ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of Power Efficient and High Speed Carry Select Adder Using Brent Kung Adder

T. Naga Praveen
M.Tech student
Department of ECE,
Dr.K V Subba Reddy Institute of Technology,
Dupadu, Kurnool, AP, India.

J. Naveen Kumar
Assistant Professor,
Department of ECE,
Dr.K V Subba Reddy Institute of Technology,
Dupadu, Kurnool, AP, India.

Abstract

The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP).In this paper Carry Select Adder (CSA)architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time.

The time critical applications use Carry Look ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. Power and delay of all these adder architectures are calculated at different input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of delay. The designs have been synthesized at Xilinx ISE 14.4 using Verilog HDL.

Keywords- ***Brent Kung (BK) adder, Ripple Carry Adder (RCA), Regular Linear Brent Kung Carry Select Adder, Modified Linear BK Carry Select Adder, Regular Square Root(SQRT) BK CSA and Modified SQRT BK CSA.***

INTRODUCTION

An adder is a digital circuit that performs addition ofnumbers. In many computers and other kinds of processors,adders are used not only in the arithmetic logic unit, but alsoin other parts of the processor, where they are used tocalculate addresses, table indices, and similar operations.Addition usually impacts widely the overall performance ofdigital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT,FIR and IIR. Millions of instructions per second are performedin microprocessors using adders. So, speed of operation is themost important constraint. Design of low power, high speeddata path logic systems are one of the most essential areas ofresearch in VLSI. In CSA, all possible values of the inputcarry i.e. 0 and 1 are defined and the result is evaluated inadvance. Once the real value of the carry is known the resultcan be easily selected with the help of a multiplexer stage.Conventional Carry Select Adder [1] is designed using dualRipple Carry Adders (RCAs) and then there is a multiplexerstage. Here, one RCA (C_{in}=l) isreplaced by brent kung adder.As, RCA (for

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

C_{in}=0) and Brent Kung adder (for C_{in}=l).consume more chip area, so an add-onescheme i.e., Binary toExcess-l converter is introduced. Also the square root adderarchitectures of CSA [2] are designed Carry select Adder using Brent Kung adder is proposed using single BK and BECinstead of dual RCAs in order to reduce the powerconsumption with small penalty in speed.

This paper is organized as follows: In section 2, parallelprefix adders are illustrated. Section 3 explains Regular LinearBK CSA and section 4 give details of Modified Linear BKCSA. In section 5, Regular Square Root BK CSA iselucidated. The structure of Modified Square Root BK CarrySelect Adder is enlightened in Section 6. Simulation Resultsand comparisons are evaluated in section 7 and section 8concludes.

PARALLEL PREFIX ADDERS

Parallel prefix adders [3] are used to speed up the binaryadditions as they are very flexible. The structure of CarryLook Ahead Adder (CLA) is used to obtain parallel prefixadders [4] . Tree structures are used to increase the speed [5] ofarithmetic operation. Parallel prefix adders are used for highperformance arithmetic circuits in industries as they increasethe speed of operation. The construction of parallel prefixadder [6] involves three stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

Pre-possessing stage:

Generate and propagate signals to each pair of inputs A andB are computed in this stage. These signals are given by thefollowing equations:

$P_i=A_i$ xor B_i(1)

$G_i=A_i$ and B_i(2)

Carry generation network:

In this stage, we compute carries equivalent to each bit.Implementation of these operations is carried out in parallel.After the computation of carries in parallel they are segmentedinto smaller pieces. Carry usingbrent kung adderin order to reduce the powerand delay of adder.

In this paper, Modified Square Root propagate and generate are used asintermediate signals which are given by the logic equations3& 4:

$CP_{i:j}=P_{i:k+1}$ and $P_{k:j}$(3)

$CG_{i:j}=_{Gi:k+1}$ or ($P_{i:k+1}$ and $G_{k:j}$)(4)

The operations involved in fig. 1 are given as:

CPO=P_i and P_j(3(i))

CG0=($P_i$and$G_{j)}$orG_i(3(ii))

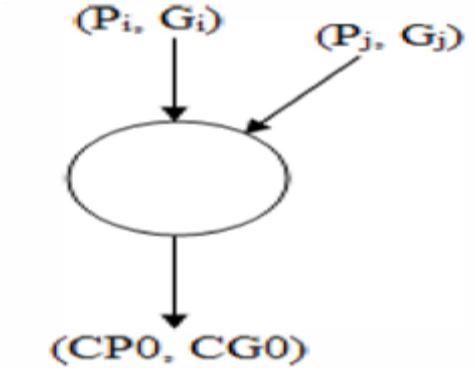

Fig 1.CarryNetwork

Post processing stage:

This is the concluding step to compute the summation ofinput bits. It is common for all the adders and the sum bits arecomputed by logic equation 5& 6:

C_{i-1}= (P_i and C_{in}) or G_i(4)

$S_i=P_i$xor $C_{i-1.}$(5)

Brent-Kung Adder:

Brent-Kung adder [7] is a very well-known logarithmicadder architecture that gives an optimal number of stages frominput to all outputs but with asymmetric loading on allintermediate stages. It is one of the parallel prefix adders.Parallel prefix adders are unique class of adders that are basedon the use of generate and propagate signals. The cost andwiring complexity is less in brent kung adders. But the gatelevel depth of Brent-Kung adders [8] is 0 ($\log_2(n)$), so thespeed is lower. The block diagram of 4-bit Brent-Kung adderis shown in Fig. 2.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

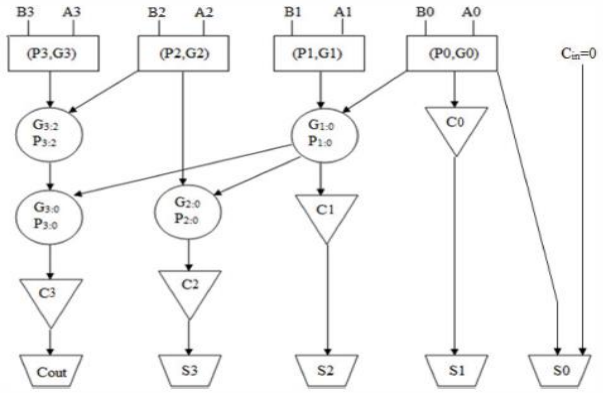

Fig.2BlockDiagramof 4BitBrentKungAdder

REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual RippleCarry Adders and a multiplexer. Brent Kung Adder [9] hasreduced delay as compared to Ripple Carry Adder. So,Regular Linear BK CSA is designed using Brent Kung Adder.Regular Linear KS CSA consists of a single Brent Kung adderfor C_{in}=0and a Ripple Carry Adder for C_{in}=1. It has fourgroups of same size. Each group consists of single Brent Kungadder, single RCA and multiplexer. We use tree structure formin Brent Kung adder to increase the speed of arithmeticoperation. The block diagram of Regular Linear BK CSA is showninFig.3.

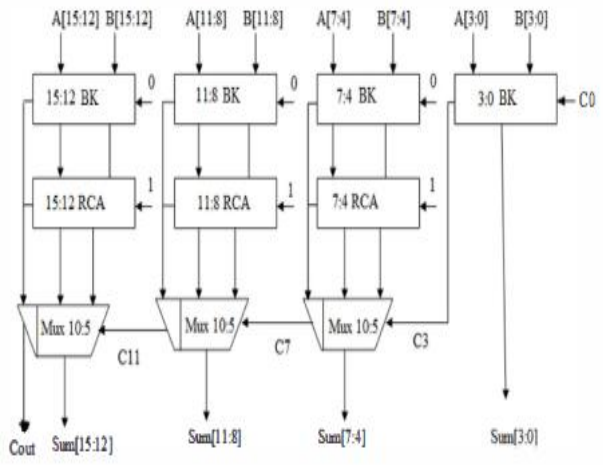

Fig. 3 Block Diagram of 16-bit Regular Linear BK Carry Select Adder

In group 2 of Regular Linear CSA, there are single BK forC_{in}=0 and single RCA for C_{in}=1. Now, the C3 tells whetherthe input carry is 0 or 1 and depending on its value the outputof particular block is selected. If C3=0 then the output of BKwith C_{in}=0 is selected using 10:5 multiplexer and if C3=1 thenoutput of RCA with C_{in}=l is selected using the MUX. A 4-bitSum [7:4] and an output carry, C7 is obtained at the output ofgroup 2. The schematic of 16-Bit Regular linear BK CSA isshown in Fig. 4. Now, power and delay of this circuit iscalculated.

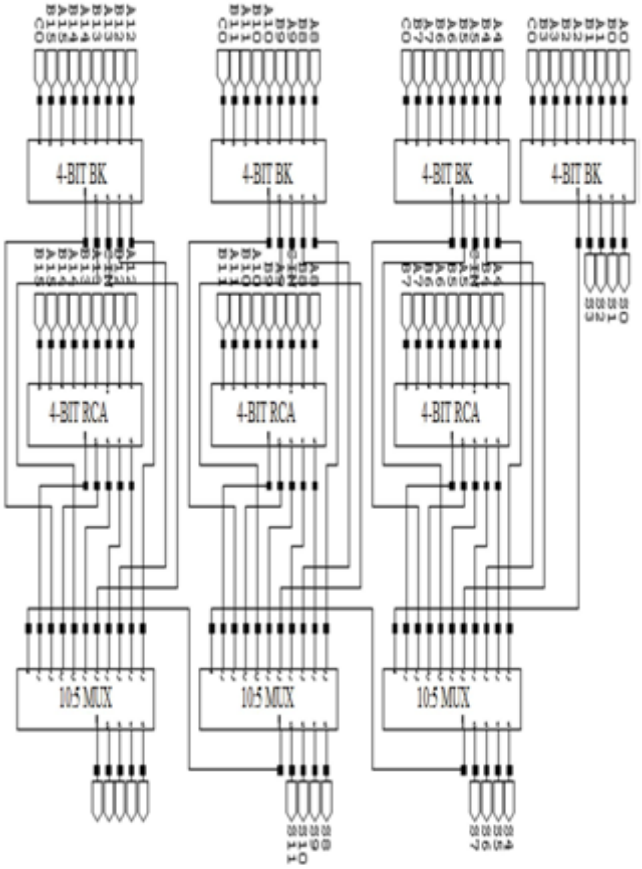

Fig. 4 Schematic of 16-Bit Regular Linear BK CSA

MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder uses singleRipple Carry Adder (RCA) for C_{in}=0 and brent kung adder forC_{in}=l and is therefore area-consuming. So, different add-oneschemes like Binary to Excess-1 Converter (BEC) have beenintroduced. Using BEC, Regular Linear BK CSA is modifiedin order to obtain a reduced area and power consumption.Binary to Excess-l converter is used to add 1 to the inputnumbers. So, here Brent Kung adder with C_{in}=1 will bereplaced by BEC because it require less number

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

of logic gatesfor its implementation so the area of circuit is less. A circuit of4-bit BEC and truth table is shown in Fig. 5 and TableIrespectively.

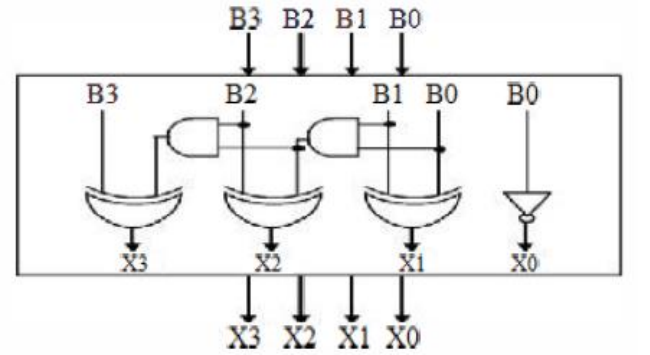

Fig. 5: 4-bit Binary to Excess-I code Converter.

The Boolean expressions of 4-bit BEC are listed below,

(Note: functional symbols, NOT, & AND, /\ XOR).

X0 = ~B0

Xl = B0 (l)/\Bl

X2 = B2 /\ (B0& Bl)

X3 = B3 /\ (B0 & B1 & B2)

TABLE I. TRUTH TABLE OF 4-BIT BINARY To EXCESS-I CONVERTER

Binary Logic B_0 B_1 B_2 B_3	Excess-l Logic X_0 X_1 X_2 X_3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Linear Modified BK CSA is designed using Brent Kungadder for Cin=O and Binary to Excess-l Converter for Cin=l inorder to reduce the area and power consumption with smallspeed penalty. Linear Modified BK CSA consists of 4 groups.Each group consists of single BK adder, BEC and multiplexer.The block diagram of Linear Modified BK CSA is shown in Fig.6.

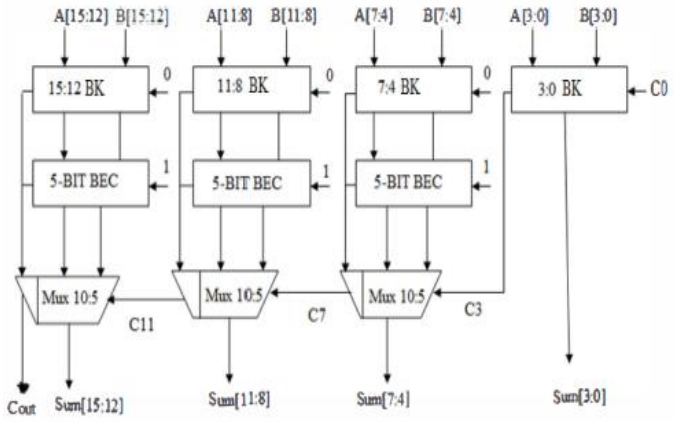

Fig.6 Block Diagram of 16-bit Linear Modified BK Carry Select Adder

To replace the N-bit Brent Kung adder, a N+l bit BEC isrequired.The importance of BEC logic comes from the largesilicon area reduction when designing Linear Modified BKCSA for large number of bits. The schematic of Linear Modified BK CSA is shown in Fig.7.

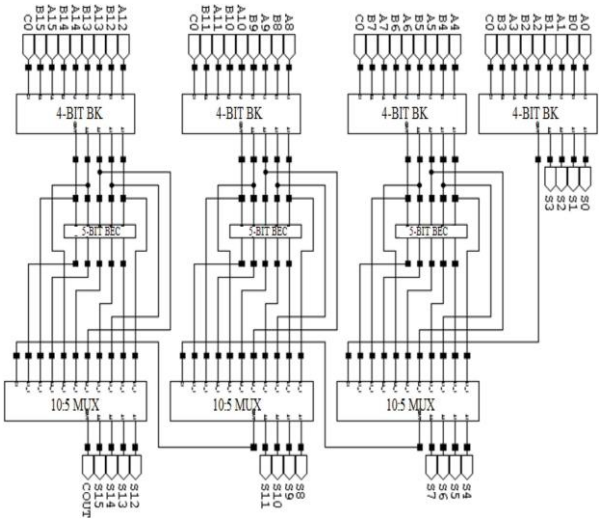

Fig. 7 Schematic of 16-Bit Linear Modified BK CSA

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder consumeslarge area and to reduce its area a new design of adder is usedi.e. Regular Square Root Brent Kung Carry Select Adder.Regular Square Root BK CSA has 5 groups of different sizebrent kung adder. Each group contains single BK for C_{in}=0,RCA for C_{in}=1 and MUX. The block diagram of the 16-bitregular SQRT BK CSA is shown in Fig. 8. High area usageand high time delay are the two main disadvantages of LinearCarry Select Adder. These disadvantages of linear carry selectadder can be rectified by SQRT CSA [10]. It is an improvedversion of linear CSA. The time delay of the linear adder candecrease, by having one more input into each set of addersthan in the previous set. This is called a Square Root CarrySelect Adder.

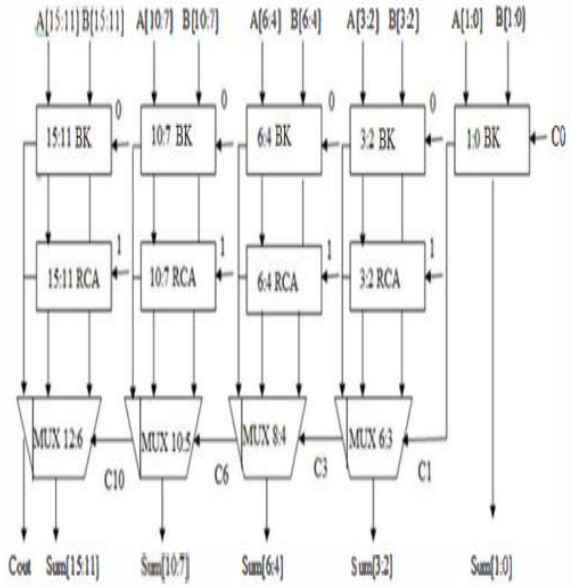

Fig. 8 Block Diagram of l6-bit Regular Square Root BK Carry Select Adder

The schematic of 16-bit Regular Square Root BK CarrySelect Adder is shown in Fig. 9. There are 5 groups in RegularSquare Root BK Carry Select Adder [11] . Here single BrentKung adder is used for C_{in}=0 and ripple carry adder is used forC_{in}=l and then there is a multiplexer stage. Due to thepresence of RCA and BK, this circuit consumes large area.

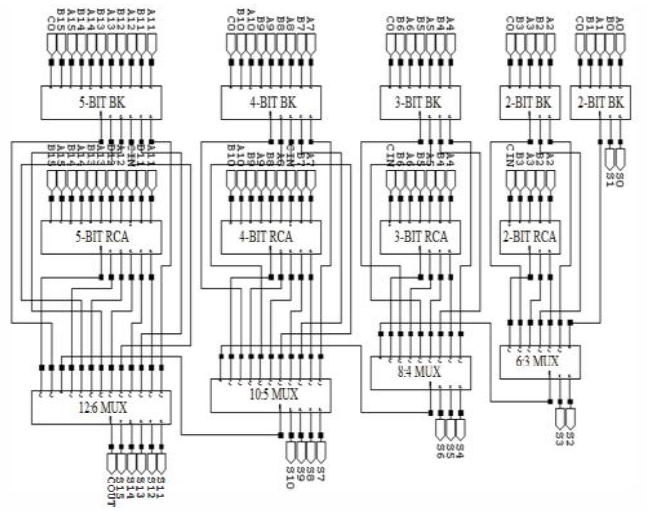

Fig. 9 Schematic of l6-Bit Regular SQRT BK CSA

MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Modified Square Root Brent Kung Carry Select Adder hasbeen designed using Brent kung adder for Cin=O and BEC forCin=l and then there is a multiplexer stage. It has 5 groups ofdifferent size brent kung adder and Binary to Excess-lConverter (BEC). BEC is used to add 1 to the input numbers.Less number of logic gates are used to design BEC ascompared to RCA therefore it consumes less area. The blockdiagram of the 16-bit modified Square Root BK Carry SelectAdder is shown in Fig.10.

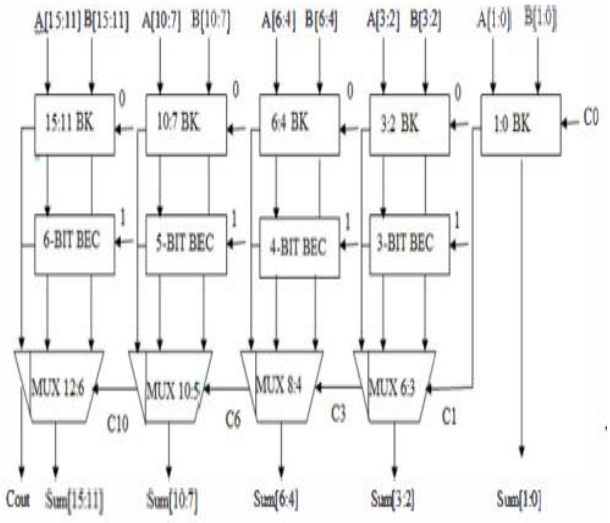

Fig. 10 Block Diagram of 16-bit Modified SQRT BK CSA

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Each group contains one BK, one BEC and MUX. For NBitBrent Kung adder, N+ 1 Bit BEC is used. Fig. 11 shows theschematic of 16-Bit Modified SQRT CSA. Powerconsumption and delay of this adder is calculated for 16-Bitword size.

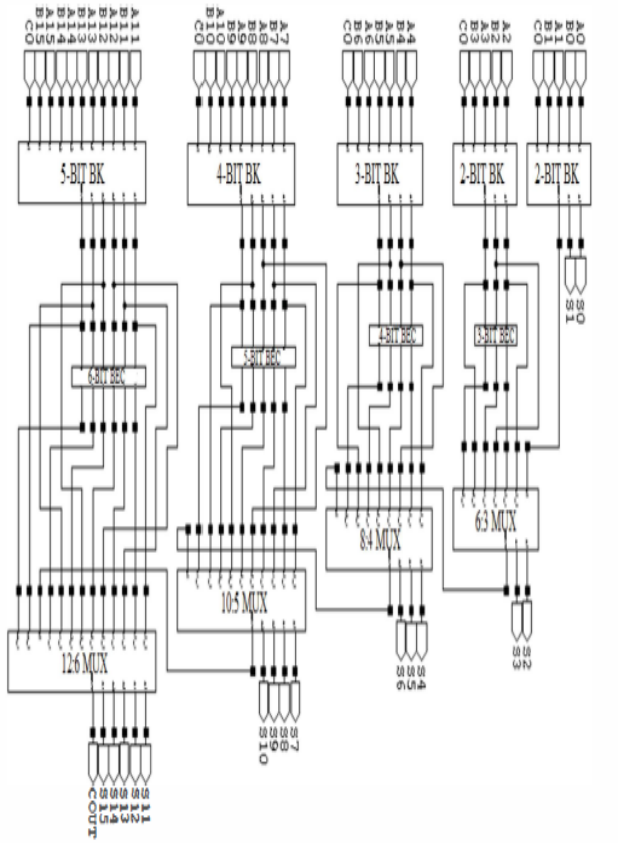

Fig. 11 Schematic of 16-Bit Modified SQRT BK CSA

SIMULATION RESULTS AND COMPARISON

Various adders were designed in Tanner EDA version 13.0tool using Predictive Model Beta Version 45nm CMOS technology. Power consumption and delay of various adderslike Regular Linear BK CSA, Regular SQRT BK CSA,Modified Linear BK CSA and Modified SQRT BK CSA hasbeen calculated for 16-Bit word size. The comparison ofvarious adders for different parameters like delay and power consumption is shown in Table II. The result analysis showsthat Modified Square Root Brent kung Carry Select Addershows better results than all the other adder architectures in terms of power consumption at different input voltages butwith a small speed penalty. The graphical representation ofcomparison of Regular Linear BK CSA and Modified Linear BK CSA for different input voltages for power consumption isshown in fig. 12. Results show that modified linear BK CSAshows better results than Regular Linear BK CSA.

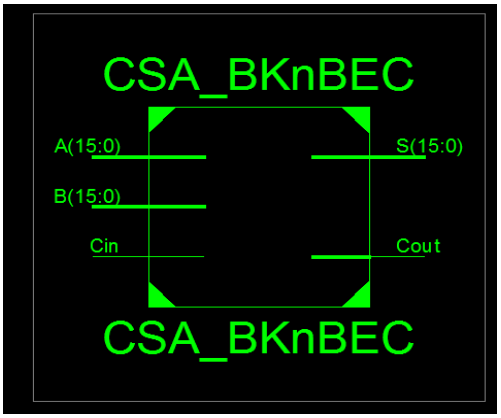

Fig12: Block diagram of 16bit-BK-BEC Carry select adder

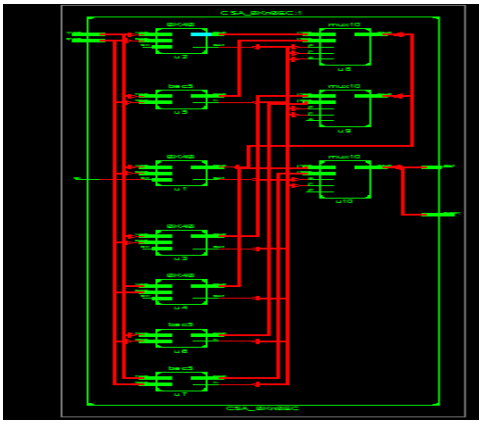

Fig13: RTL Schematic of 16bit-BK-BEC Carry select adder

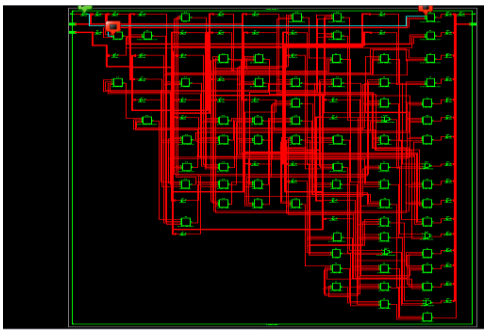

Fig14: Technology Schematic of 16bit-BK-BEC Carry select adder

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

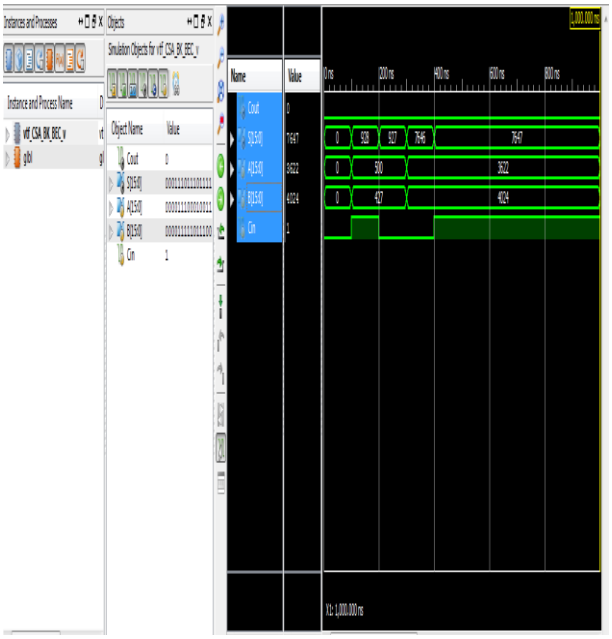

Fig15: Simulation output waveform of 16bit-BK-BEC Carry select adder

TABLE II. COMPARISON OF DIFFERENT ADDERS FOR POWER CONSUMPTION AND DELAY AT VARIOUS INPUT VOLTAGES

ADDER	Supply voltage									
	Power(w)					Delays(s)				
	0.6v	0.8v	1.0v	1.2v	1.4v	0.6v	0.8v	1.0v	1.2v	1.4 v
Regular Linear BK CSA	1.7SE-08	3.47E-08	7.37E-08	1.7SE-07	1.02E-06	1.13E-10	6.44E-11	4.63E-1 1	2.47E-11	S.7S E-12
Linear Modified BK CSA	1.24E-08	2.16E-08	4.13E-08	1.12E-07	7.43E-07	1.21E-10	1.04E-10	1.02E-10	8.27E-11	6.41 E-11
Regular Square Root BK CSA	1.23E-08	3.4SE-08	7.42E-08	1.74E-07	1.03E-06	8.08E-11	6.34E-11	4.11E-1 1	3.64E-11	3.03 E-11
Modified Square Root BK CSA	1.29E-08	2.S4E-08	4.12 E-08	1.10E-07	8.91 E-07	1.24E-10	9.16E-11	9.10E-11	8.03 E-11	6.22 E-11

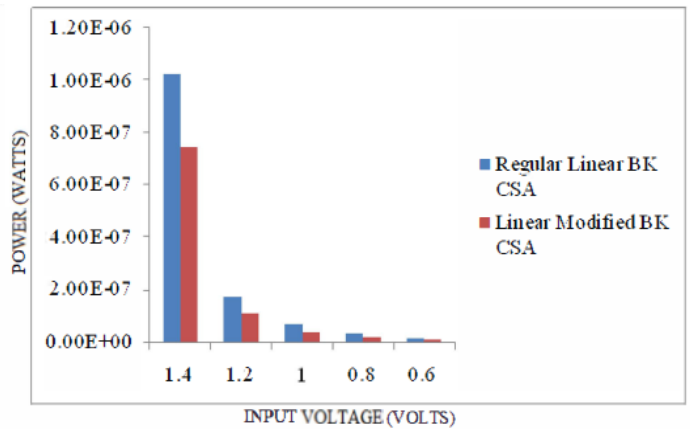

Fig. l6 Comparison of Regular Linear BK CSA and Modified Linear BKCSA for power comparison at different input voltages.

The graphical representation of comparison of RegularSQRT BK CSA and Modified SQRT BK CSA at differentinput voltages for power consumption is shown in fig. 17.Results show that modified SQRT BK CSA shows betterresults than Regular SQRT BK CSA. The graphicalrepresentation of comparison of Regular linear BK CSA andModified SQRT BK CSA for power consumption at differentinput voltages is shown in Fig. 18. The graphicalrepresentation of comparison of different adders for delay atdifferent input voltages is shown in Fig. 19.

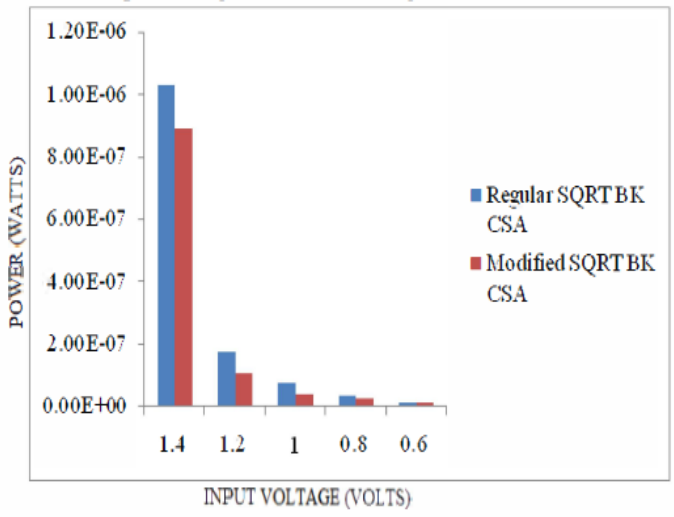

Fig. l7 Comparison of Regular SQRT BK CSA and Modified SQRT BK CSAfor power comparison at different input voltages.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

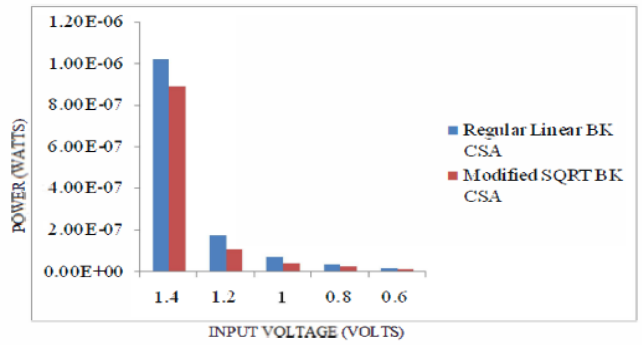

Fig. 18 Comparison of Regular Linear BK CSA andModified SQRT BK CSAfor power comparison at different input voltages.

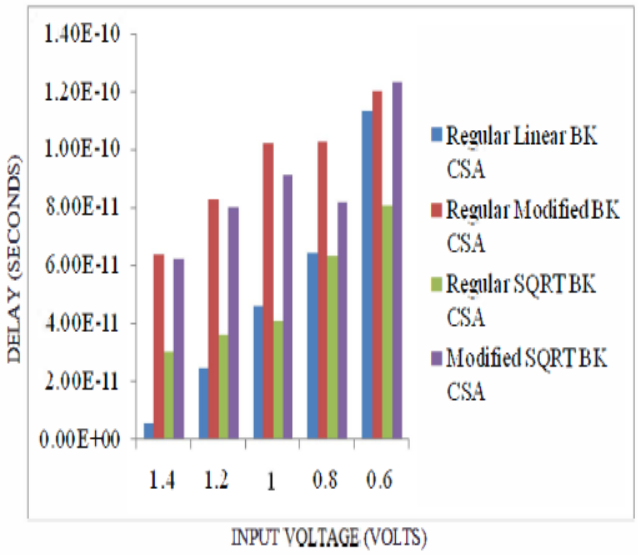

Fig. 19 Comparison of different adders for delay at different input voltages.

Fig. 20, Fig. 21 and Fig. 22 shows the power VsTemperature graphs for Regular linear BK CSA and modifiedlinear BK CSA, regular SQRT BK CSA and modified SQRTBK CSA, regular linear BK CSA and modified SQRT BKCSA respectively. From the graphical representation it is clearthat Modified Linear and Square Root BK CSA have reducedpower consumption but they have increased delay incomparison to Regular Linear and Square Root BK CSA.Modified square root brent kung carry select adder consumesless power than all the other adder architectures at differentinput voltages and as the input voltage is reduced, the powerconsumption also reduces.

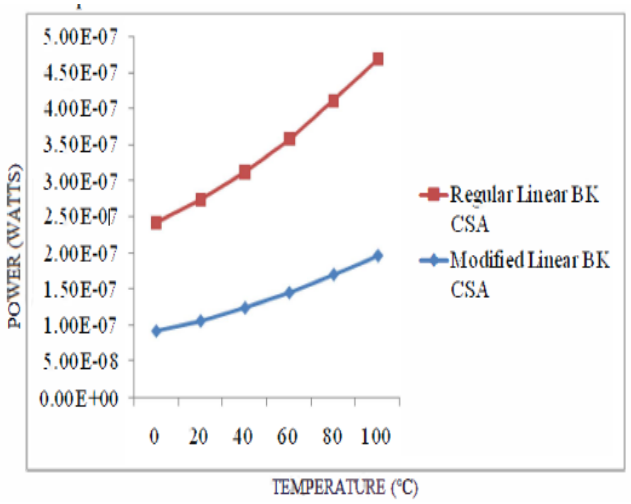

Fig. 20 Power Vs Temperature for Regular Linear BK CSA and ModifiedLinear BK CSA

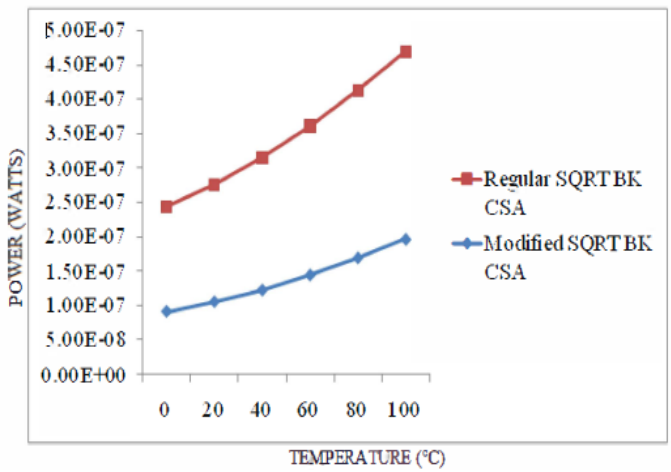

Fig. 21 Power Vs Temperature for Regular SQRT BK CSA and ModifiedSQRT BK CSA.

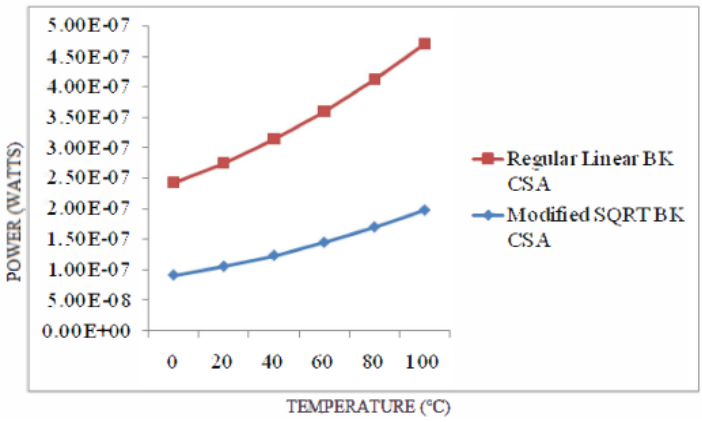

Fig. 22 Power Vs Temperature for Regular Linear BK CSA and ModifiedSQRT BK CSA

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

CONCLUSION

In this work, a Modified Square Root BK Carry SelectAdder is proposed which is designed using single Brent kungadder and Binary to Excess-l Converter instead of usingsingle brent kung adder for C_{in}=0 and Ripple Carry Adder forC_{in}=l in order to reduce the delay and power consumption ofthe circuit. Here, the adder architectures like Regular LinearBK CSA, Modified Linear BK CSA, Regular SQRT BK CSAand Modified SQRT BK CSA are designed for 16-Bit wordsize only. This work can be extended for higher number of bitsalso. By using parallel prefix adder, delay and powerconsumption of different adder architectures is reduced. As,parallel prefix adders derive fast results therefore brent kungadder is used. The synthesized results show that powerconsumption of Modified SQRT BK CSA is reduced incomparison to Regular Linear CSA.

REFERENCES

[I] Shivani Parmar and Kirat Pal Singh," Design of High Speed Hybrid CarrySelect Adder", IEEE's 3rd International Advance Computing Conference(IACC) Ghaziabad, ISBN: 978-1-4673-4527-9,22-23 February 2013.

[2] Yajaun He, Chip-Hong Chang, and Jiangmin Gu, "An area efficient 64-Bit square Root carry-select adder for low power Applications, " in Proc.IEEE International Symposium Circuits and Systems, vol. 4, pp. 4082-4085,2005.

[3] M. Snir, "Depth-Size Trade-Offs for Parallel Prefix Computation",Journal of Algorithms, Vo!.7, Issue-2, pp.185-201, June 1986.

[4] David Jeff Jackson and Sidney Joel Hannah, "Modelling and Comparisonof Adder Designs with Verilog HDL", 25th South-eastern Symposium onSystem Theory, pp.406-4tO, March 1993.

[5] Belle W.Y. Wei and Clark D. Thompson, "Area-Time Optimal AdderDesign", IEEE transactions on Computers, vo!.39, pp. 666-675,May1990.

[6] Y. Choi, "Parallel Prefix Adder Design", Proc. 17th IEEE Symposium onComputer Arithmetic, pp. 90-98, 27th June 2005.

[7] J. M. Rabaey, "Digital Integrated Circuits- A Design Perspective", NewJersey, Prentice-Hall, 2001.

[8] R. Brent and H. Kung, "A regular layout for parallel adders", IEEETransaction on Computers, vol. C-31,n o.3,p p. 260-264,M arch 1982.

[9] Adilakshmi Siliveru, M. Bharathi, "Design of Kogge-Stone and BrentKungadders using Degenerate Pass Transistor Logic", InternationalJournal of Emerging Science and Engineering, Vol.-I, Issue-4, February2013.

[10] K. Saranya, "Low Power and Area-Efficient Carry Select Adder",International Journal of Soft Computing and Engineering, Vol.-2, Issue-6,January 2013.

[11] Deepthi Obul Reddy and P. Ramesh Yadav, "Carry Select Adder withLow Power and Area Efficiency", lnlernalional Journal of EngineeringResearch and Developmenl, Vol. 3, Issue 3, pp. 29-35, August 2012.

Author Details

T.Naga Praveen received B.TECH from Kottam college of engineering and perusing M.TECH from DR.KVSRIT Kurnool, A.P, India from the university of JNTU Ananthapur in VLSI&Embedded system design.

J.Naveen Kumar received B.TECH from Sri Kottam Tulasireddy college of Engineering and M.TECH from Mallareddy Institute of Technology,JNTUH. He is working as a assistant professor in KVSRIT, Kurnool. He has interested in VLSI systems.