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A Quasi-Unipolar SPWM Full-Bridge without Transformer Renewable Grid-Inverter

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Abstract

Transformer less photovoltaic inverter with ac bypass brings low conduction loss and less leakage current. To eliminate the leakage current induced by the common mode voltage, the clamping topology can be adopted to hold the common-mode voltage on a constant value in the freewheeling period. A full-bridge inverter topology with constant common-mode voltage (FB-CCV) has been derived and proposed in this paper, two unidirectional freewheeling branches are added into the ac side of the FB-CCV, and the split structure of the proposed freewheeling branches does not lead itself to the reverse-recovery issues for the freewheeling power switches and as such superjunction MOSFETs can be utilized without any efficiency penalty. The operationmode and common-mode characteristics of the FB-CCV, Heric, and HB-ZVR topologies are analyzed and compared in detail.

*Keywords-**PWM,FBCCV,Photovoltaic,common mode voltage.***

INTRODUCTION

Transformer-less grid-connected inverters have a lot of advantages such as higher efficiency, smaller size, lighter weight, lower cost, and so on. The unipolar sinusoidal pulsewidth modulation (SPWM) full-bridge inverter has received extensive attentions owing to its excellent differential-mode characteristics such as higher dc voltage utilization, smaller current ripple in the filter inductor, and higher processing efficiency.

Topology:

- PWM pulse,
- Space vector PWM pluses
- Common-mode voltage,
- Full-bridge inverter,
- Passive clamping,
- Quasi-unipolar SPWM (qSPWM),

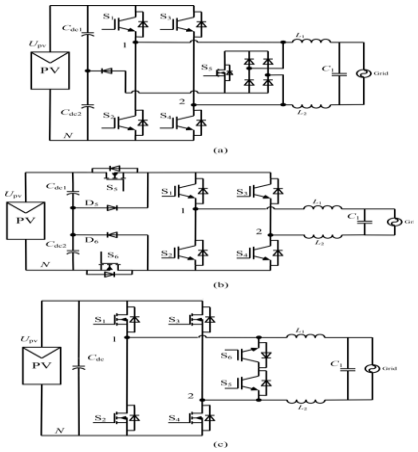

Fig. 1.Typical transformerless inverter topologies. (a) HB-ZVR topology.(b) H6 topology. (c) Heric topology.

Exciting concepts:

The power conversion systems can be classified according to the type of the input and output power

- AC to DC (rectifier)
- DC to AC (inverter)
- DC to DC (DC-to-DC converter)
- AC to AC (AC-to-AC converter)

Power electronic devices may be used as switches, or as amplifiers.[3] An ideal switch is either open or closed and so dissipates no power; it withstands an applied voltage and passes no current, or passes any amount of current with no voltage drop.

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Semiconductor devices used as switches can approximate this ideal property and so most power electronic applications rely on switching devices on and off, which makes systems very efficient as very little power is wasted in the switch. By contrast, in the case of the amplifier, the current through the device varies continuously according to a controlled input.

DC/AC converters (inverters)

DC to AC converters produce an AC output waveform from a DC source. Applications include adjustable speed drives (ASD), uninterruptable power supplies (UPS), active filters, Flexible AC transmission systems (FACTS), voltage compensators, and photovoltaic generators. Topologies for these converters can be separated into two distinct categories: voltage source inverters and current source inverters

AC/AC converters

Converting AC power to AC power allows control of the voltage, frequency, and phase of the waveform applied to a load from a supplied AC system.The two main categories that can be used to separate the types of converters are whether the frequency of the waveform is changed. AC/AC converter that don't allow the user to modify the frequencies are known as AC Voltage Controllers, or AC Regulators.

DC link converters:

DC Link Converters, also referred to as AC/DC/AC converters, convert an AC input to an AC output with the use of a DC link in the middle. Meaning that the power in the converter is converted to DC from AC with the use of a rectifier, and then it is converted back to AC from DC with the use of an inverter. The end result is an output with a lower voltage and variable (higher or lower) frequency

Construction of the FB-CCV

Implementation of common-mode voltage of the Heric is on a constant value in the freewheeling period, the procedure of deriving the freewheeling branches and passive clamping branches will be demonstrated in the following how a Heric topology, as shown in Fig. 1 (c), can be transformed to a FB-CCV topology, as shown in Fig. 3 (a).

1. First, the bidirectional freewheeling branches are extracted from the Heric topology, as shown in Fig. 2 (a). Separate the bidirectional branches to form two unidirectional branches shown in Fig. 2 (b).
2. Next, the positions of S_5 and D are exchanged in the unidirectional branch B, as shown in Fig. 2 (c).
3. Finally, find or build a clamping voltage source in the full-bridge inverter [for example, point 3 in Fig. 2 (d)], then introduce two clamping diodes D_7 and D the inverter to connect the center points of the two unidirectional branches to the clamping voltage source.

The direction of the clamping diodes can be determined using the back-to-back rule of $D_5$and D,asshown in Fig. 2 (d). 6 Remark: It should be mentioned that the freewheeling branches and passive clamping branches can be rearranged as following.

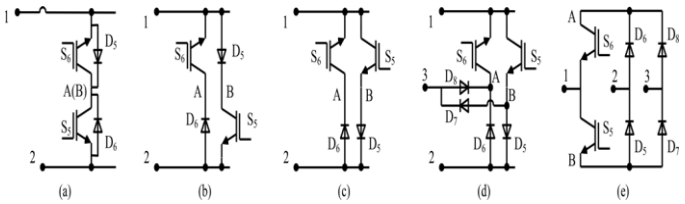

Fig. 2.Derivation of the freewheeling branches and passive clamping branches.

Operation principle:

In the QSPWM style, there are two freewheeling modes in the 2 freewheeling period. One is dead-time mode, such as the time intervals [t 2,t 3] and [t] in Fig. 3 (c); another is zero-vector mode, the time interval t 4 ,t 5], as shown in Fig. 3 (c) also. Especially, the potential of the zero-vector freewheeling path is defined as the potential of points 1 and 2 as shown in Fig. 3 (a), and the zero-vector freewheeling path can be freely clamped to the midpoint of the input voltage (it is the point 3) through

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the diodes D 7 and D 8 3 ,t 4 in the zero-vector freewheeling stage. B. 1) All active power devices are ideal switches with antiparallel diodes, and the power diodes are also ideal diodes without parasitic parameters; and 2) The capacitance C dc1 and C dc2 filter are large enough to be treated as constant voltage sources.

Modes of operation:

Stage I-1 [t 1 ,t 2]: Refer to Figs. 3(c) and 4(a). At t,themain switches S_1 and S_4 are turned ON and other switches are OFF, and the inductor current $I_L = I_L$ (t). In this stage, the power flows from the PV side of the grid through S_1, S and the filter. The inductor current I_L increases linearly until t 4 , this stage named as power mode

$$i_L(t) - I_L(t_1) = \frac{U_{pv} - u_g}{L}(t - t_1) \quad (1)$$

$$u_{12} = U_{pv}. \quad (2)$$

Stage I-2 [t 2 ,t 3]: Refer to Fig. 4 (b). At t 2 S are turned OFF, and then all switches are off. This stage s called as dead-time freewheeling mode. The inductor current I_{L1} flows into a dc bus capacitor through he antiparallel diodes D and D 3 . The inductor current I reduces linearly under the effects of the PV Voltage and the grid voltage L.

$$i_L(t) - I_L(t_2) = \frac{-U_{pv} - u_g}{L}(t - t_2) \quad (3)$$

$$u_{12} = -U_{pv}. \quad (4)$$

Stage I-3 [t3,t4]: Refer to Fig. 4 (c). At t, the freewheeling switches S5and S63are turned ON with the A same commutation order, and the other switches are OFF. This stage is called aszero-vector freewheeling ode. The inductor current I flows through the diode D6 and the switch S . The inductor current I_{L6} reduces linearly under the effect of the grid voltage L

$$i_L(t) - I_L(t_3) = \frac{-u_g}{L}(t - t_3) \quad (5)$$

$$u_{12} = 0. \quad (6)$$

At t_4 , S_5 , and S_6 are turned OFF, and then all switches are OFF, the inverter works at the dead-time freewheeling mode (likes stage I-2). In state II, the grid voltage goes into negative half period, and the rid-in current still stays at positive direction.

Stage II-1 [t1,t12]: At t 11 , the freewheeling switches S and are turned ON, and other switches are OFF. The direction of the grid voltage is reversed, and the inductor current I flows through the diode D 6 and the switch S 6 L5 , is linearly increased under the effect of the grid voltage (Fig. 4 (c) can be referred as the equivalent circuit, but the bottom of the symbol of the rid is positive direction). This stage is called as the energy storage mode.

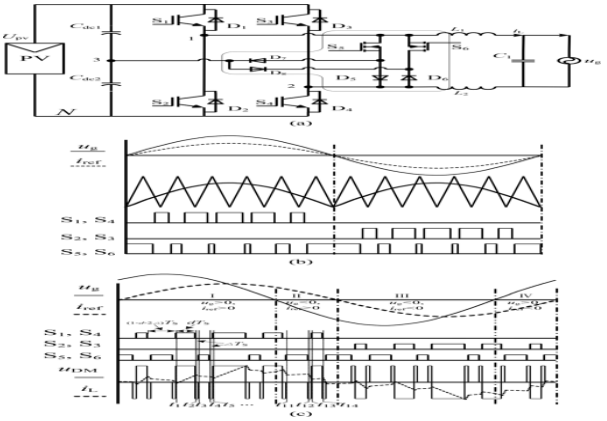

Fig. 3.Proposed transformerless PV grid-connected inverter. (a) FB-CCV topology. (b) Gate drive signal f the qSPWM with unity power factor. (c) Key operation waveforms of the FB-CCV with qSPWM.

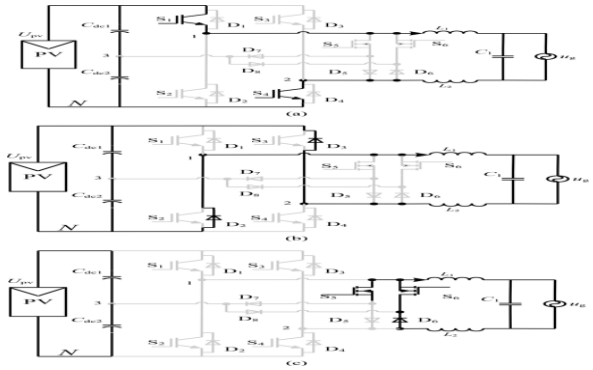

Fig. 4. Equivalent circuits in the positive half period of the grid-in current.(a) Stage 1 [t 1,t2]. (b) Stage 2 [t2,t3]. (c) Stage 3 [t3,t4] .

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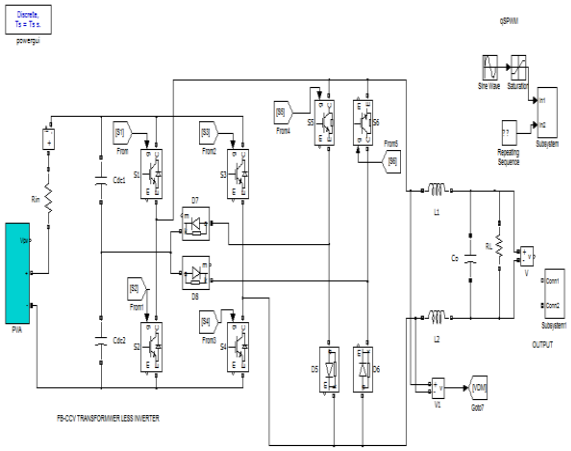
Stage II-2 [t_2]. (b) Stage 2 [t_{12} ,t_{13}]: At t,t_3. (c) Stage 3 [t , S5 , and S then all switches are OFF. The inductor current I_3,t_4].are turned OFF,

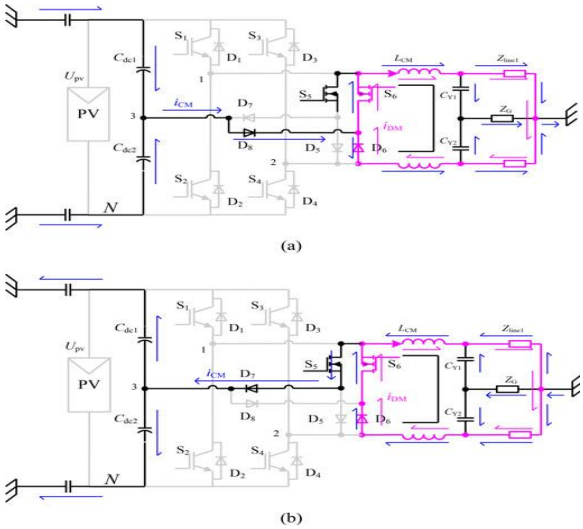
EXPERIMENTAL RESULTS:
SIMULINK RESULTS AND OUTPUTS



Stage II-3 [t_{13} ,t_{14}]: At t_{13} , the main switches S are turned ON and other switches are OFF. In this stage, the energy is stored in filter inductors through S 1 , and S4 .The inductor current I_L is increased linearly until t.

$$i_L(t) - I_L(t_{11}) = \frac{|U_g|}{L}(t - t_{11}) \quad (7)$$

$$u_{12} = 0. \quad (8)$$



Simulation modal of FB-CCV topology

Simulation outputs:

Figure: Unipolar SPWM pulses.

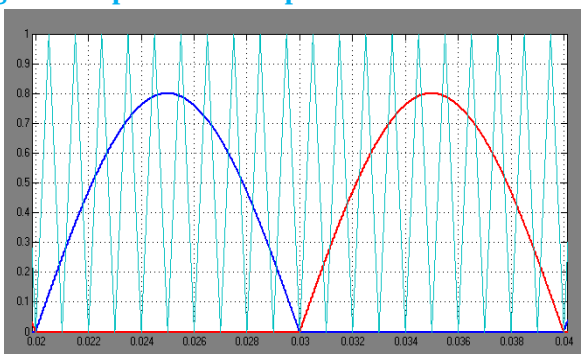


Fig. 5.Equivalent circuits in the clamped mode. (a) The potential of the zero vectorfreewheeling path falls. (b) The potential of the zero-vector freewheeling path rises.

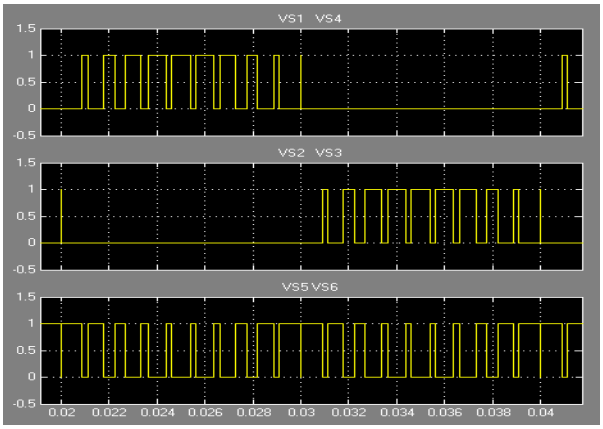


Figure: Switching pulses of the vs 1&4,2&3, 5&6.

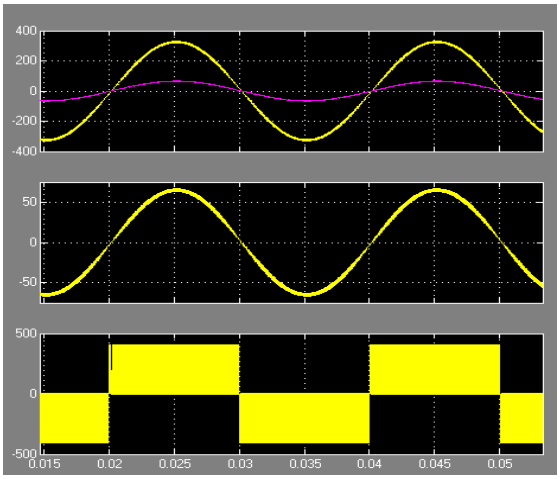


Figure: Output voltage and current

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CONCLUSION

The proposed inverter is an optimized topology with high conversion efficiency and low leakage current. These merits are verified and compared by a universal prototype. It can be concluded that the proposed topology is extremely suitable for transformer-less single-phase grid-connected inverter with lower switching frequency.

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