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Modeling of Adders using CMOS and GDI Logic for Vedic Multipliers

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Abstract:
As the days go by, the innovation in the technology is growing faster and smaller chips with more complexity in the design and implementation. Design of adders is prime importance in any given embedded application; hence the design of reliable and efficient adder on a VLSI based embedded application matters. In this paper we primarily deal with the construction of high speed adder circuits. Design and modeling of various adders like Ripple Carry Adder, Kogge Stone Adder, and Brent Kung Adder is done by using CMOS and GDI logic and comparative analysis is coated. The simulated results verify the functionality of high speed adders and performance parameters like Power, Delay and power-delay product is analyzed. With the results obtained and analysis made, gives a clear picture that KSA is the more efficient in speed and power parameters. This work is extended to designing of Vedic multiplier. A Vedic multiplier is designed by using UrdhavaTriyagbhayam sutra and the adder design is done by using CMOS and GDI logic.

Keywords:
Ripple Carry Adder (RCA), Kogge Stone Adder (KSA), Brunt Kung Adder (BKA), Vedic Multiplier using adder, Gate count, number of transistors, Power, and Delay.

I. INTRODUCTION:

In electronic, an adder is a digital circuit that performs addition of number. In many computers and other kind of processors, adders are used not only in the Arithmetic Logic unit (ALU), but also in other parts of the processors.

In this paper a different set of adders like RCA, KSA, BKA are of the adders are designed. Addition is the most fundamental operation in any digital system. A simple adder performs the addition of given two numbers and the result is sum of those two numbers. Multiplication operation greatly depends on adder operation as it is one of the key hardware block in most digital signal processing system. Its main block is Arithmetic unit. The number of multiplication operation is performed by a series or parallel addition concept. Multiplication is one of the fundamental block in almost all the arithmetic logic units. This Vedic multiplication is mainly used in the fields of the Digital Signal Processing (DSP) and also in so many applications like Fast Fourier Transform, convolution, filtering and microprocessor applications.

In most of the DSP algorithms multiplier is one of the key component and hence a high speed and area efficient multiplier is needed and multiplication time is also one of the predominant factor for DSP algorithms. The ancient mathematical techniques like Vedic mathematics used to reduce the computational time such that it can increases speed and also requires less hardware. The rest of the sections in this paper are arranged as, Section 2 gives the literature survey of various adder designs, here the adders are designed and implemented on CADENCE toolset for VLSI back-end design, Section 3 gives the methodology to design various adders like RCA, KSA and BKA, Section 4 gives the simulation results and performance analysis of the various adders, followed by conclusion and references sections.

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II. LITERATURESURVEY

Design and modeling of adders for VLSI and embedded application is a critical task to perform, the following are the few references that we have gone through that has helped us in the design of adders, In [1] the authors have designed and simulated various adders like RCA, CSA, CLA and KSA for s precession of 8-bit and have coated a comparative statement. The simulations and analysis is made on Cadence Design Suite using 45nm technology. In [2] the authors have designed and tested 1-but full adders using Cadence Design Suite at GPDK 45nm technology with unvaried width and length parameter of MOSFET used. And a comparative analysis and simulation result is coated. In [3] the FPG A implementation of 8 bit adders like RCA, CSA, CLA, and KSA is performed and its RTL is coated with its implementation details. In [4] the detail investigation of the performances of 8 bit KSA and BK Aadder in terms of computational delay and design are as are studied. In [5] the survey and brief on the design of BKA is provided. In [6] the FPGA implementation, comparison, and performance analysis of parallel prefix adders is made.

III. DESIGN OFADDERS

A. Ripple Carry Adder:

The RCA block can be constructed by cascading full adder blocks in series. It is possible to create a logical circuit using multiple full adder to add N-bit numbers. Each full adder inputs a Cin,which is the Cout of the previous adder. This kind of adder is RCA, since each carry bit "ripples" to the next full adder. For an n bit adder it requires n 1 bit full adder.

Drawbacks of Ripple Carry Adder:

The RCA is relatively slow since each full adder must wait for the carry bit to be calculated from the previous full adder. Equation of Ripple Carry Adder

Si= Ai XOR BiXORCi-1 (1)

Ci+1= (Ai AND Bi) OR (Bi AND Ci) OR(Ci ANDAi) (2)

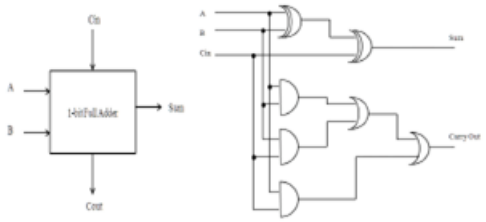

Figure1: Block diagram and Schematic of 1-bit Full Adder

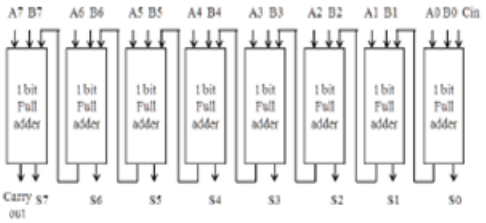

Figure 2: Block diagram of 8-bit Ripple Carry Adder

B. Kogge Stone Adder:

KSA is a parallel prefix form carry look ahead adder. It generates carry in O (log n) time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area. It has three processing stages for calculating the sum bits.

Working of KSA:

i. Pre-processing:

In this step the computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

Pi = AixorBi (3)

Gi = AiandBi (4)

ii. Carry look ahead network:

This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit.

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It uses group propagate and generate as intermediate signals which are given by the logic equations below:

Black Cell. The black cell takes two pairs of generate and propagate signals (Gi, Pi) and (Gj, Pj) as input and computes a pair of generate and propagate signals (G, P) as output

G = Gi OR (PiANDPj) (5)

P = PiANDPj (6)

Grey Cell. The gray cell takes two pairs of generate and propagate signals (Gi, Pi) and (Gj, Pj) as inputs and

Computes a generate signal G as output

G = Gi OR (PiANDPj) (7)

iii. Post processing:

This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic givenbelow:

Si = pi xor Ci-1.

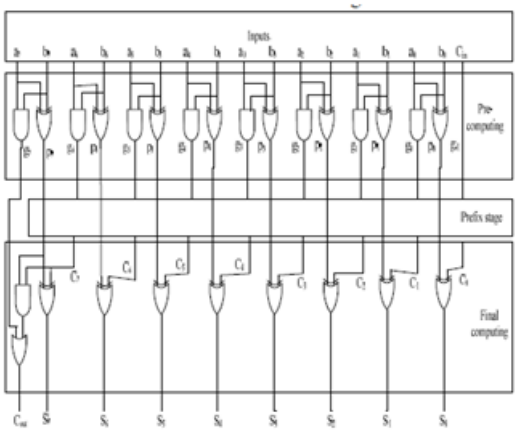

Figure 3: Computational stages of Parallel Prefix Adder.

A. Brent Kung Adder:

Brent Kung Parallel Prefix Adder has a low fan-out from each prefix cell but has a long critical path and is not capable of extremely high speed addition.

In spite of that, this adder proposed as an optimized and regular design of a parallel adder that addresses the problems of connecting gates in a way to minimize chip area. Accordingly, it considered as one of the better tree adders for minimizing wiring tracks, fan out and gate count and used as a basis for many other networks.

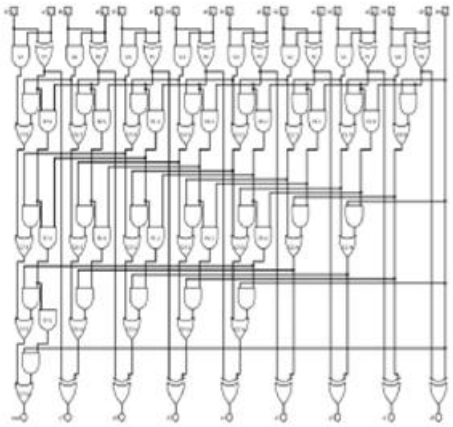

Figure 4: Schematic of 8-bit KoggeStone Adder

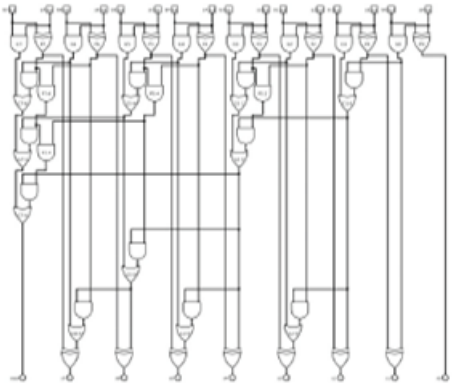

Figure 5: Schematic of 8-bit Brent Kung Adder

IV. VEDIC MULTIPLIERS

In this section we propose a Vedic multiplication technique called "Urdhva-Tiryakbhyam – Vertically and crosswise." Which can be used not only for decimal multiplication but also used for binary multiplication? This technique mainly consists of generation of partial products parallel and then we have to perform the addition operation simultaneously [3]. This algorithm can be used for 2x2, 4x4, 8x8....N×N bit multiplications.

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To illustrate this technique, let us consider two decimal numbers 252 and 846 and the multiplication of two decimal numbers 252×846 is explained by using the line diagram shown in below figure 6. First multiply the both numbers present on the two sides of the line and then first digit is stored as the first digit of the result and remaining digit is stored as pre carry for the next coming step and the process goes on and when there is more than one line then calculate the product of end digits of first line and add the result to the product obtained from the other line and finally store it as a result and carry. The obtained carry can be used a carry for the further steps and finally we will get the required result which is the final product of two decimal numbers 252x846. Take the initial carry value as the zero. For clear understanding purpose we explained the complete algorithm in the below line diagram such that each bit represents a circle and number of bits equal to the number of circles present.

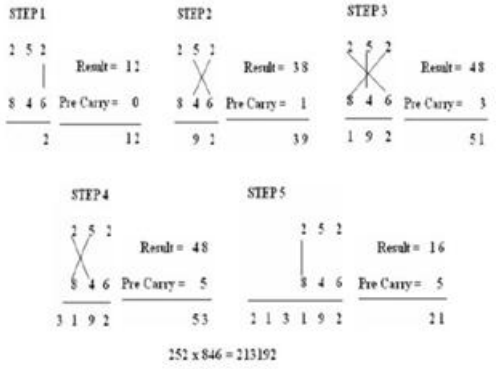

Figure 6. Multiplication of two decimal numbers

The architectures for 2×2, 4×4 bit modules are discussed in this section. In this section, the technique used is 'Urdhva-Tiryakbhyam' (Vertically and Crosswise) sutra which is a simple technique for multiplication with lesser number of steps and also in very less computational time. The main advantage of this Vedic multiplier is that we can calculate the partial products and summation to be done concurrently. Hence we are using this Vedic multiplier in almost all the ALU's.

A. 2×2 Vedic Multiplier Block

To explain this method let us consider 2 numbers with 2 bits each and the numbers are A and B where A=a0a1 and B=b0b1 as shown in the below line diagram. First the least significant bit (LSB) bit of final product (vertical) is obtained by taking the product of two least significant bit (LSB) bits of A and B is a0b0. Second step is to take the products in a crosswise manner such as the least significant bit (LSB) of the first number A (multiplicand) is multiplied with the next higher bit of the multiplicand B in a crosswise manner. The output generated is 1-Carry bit and 1bit used in the result as shown below. Next step is to take product of 2 most significant bits (MSB) and for the obtained result previously obtained carry should be added. The result obtained is used as the fourth bit of the final result and final carry is the other bit.

s0 = a0b0

c1s1 = a1b0 + a0b1

c2 s2 = c1 + a1b1 (8)

The obtained final result is given as c2s2s1s0. A 2×2 Vedic multiplier block is implemented by using two half adders and four two input and gates as shown in below Figure 7.

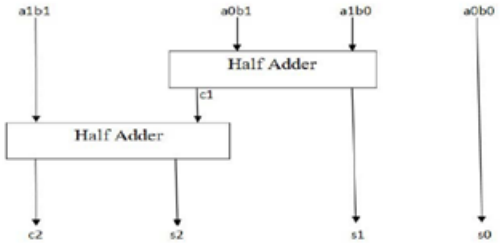

Figure 7. Block Diagram of 2×2 Vedic Multiplier

B. 4x4 Vedic Multiplier Block

In this section, now we will discuss about 4x4 bit Vedic multiplier. For explaining this multiplier let us consider two four bit numbers are A and B such that the individual bits can be represented as the A3A2A1A0 and B3B2B1B0. The procedure for multiplication can be explained in terms of line diagram shown in below figure. The final output can be obtained as the C6S6S5S4S3S2S1S0.

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The partial products are calculated in parallel and hence delay obtained is decreased enormously for the increase in the number of bits. The Least Significant Bit (LSB) S0 is obtained easily by multiplying the LSBs of the multiplier and the multiplicand. Here the multiplication is followed according to the steps shown in the line diagram in figure 6. After performing all the steps the result (Sn) and Carry(Cn) is obtained and in the same way at each step the previous stage carry is forwarded to the next stage and the process goes on.

S0 = A0B0
C1S1 = A1B0 + A0B1
C2S2 = C1 + A0B2 + A2B0 + A1B1
C3S3 = C2 + A0B3 + A3B0 + A1B2 + A2B1
C4S4 = C3 + A1B3 + A3B1 + A2B2
C5S5 = C4 + A3B2 + A2B3
C6S6 = C5 + A3B3 (9)

For clear understanding, observe the block diagrams for 4x4 as shown below figure 7 and within the block diagram 4x4 totally there are four 2x2 Vedic multiplier modules, and three ripple carry adders which are of four bit size are used. The four bit ripple carry adders are used for addition of two four bits and likewise totally four are use at intermediate stages 3 of multiplier. The carry generated from the first ripple carry adder is passed on to the next ripple carry adder and there are two zero inputs for second ripple carry adder. The arrangement of the ripple carry adders are shown in below block diagram which can reduces the computational time such that the delay can be decrease.

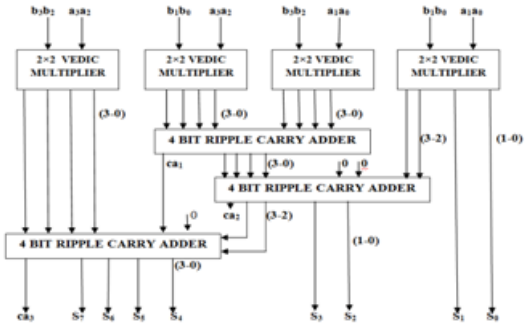

Figure 9. Block Diagram of 4x4 bit Vedic Multiplier

IV.RESULTS ANDDISCUSSIONS

The following are the simulation results and performance analysis of various adders with precession of 4 bit and 8 bit. The design is done using CMOS and GDI logic using using DSCH and Microwind 120nm technology. The part A shows schematic and simulation results of the same and part B shows comparative analysis with performance measure as power, Delay and Number of Transistor.

A.SIMULATION RESULTS

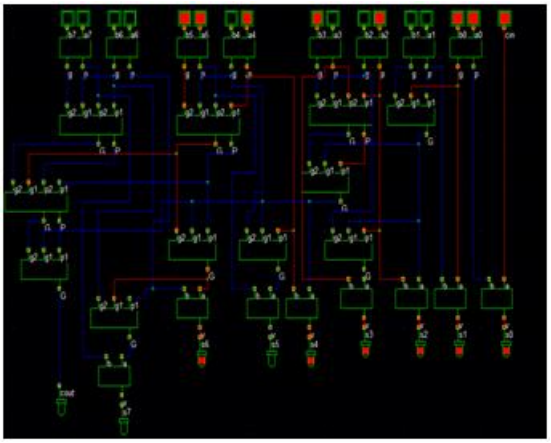

Fig 10: Schematic of 8bit Brent Kung Adder using CMOS

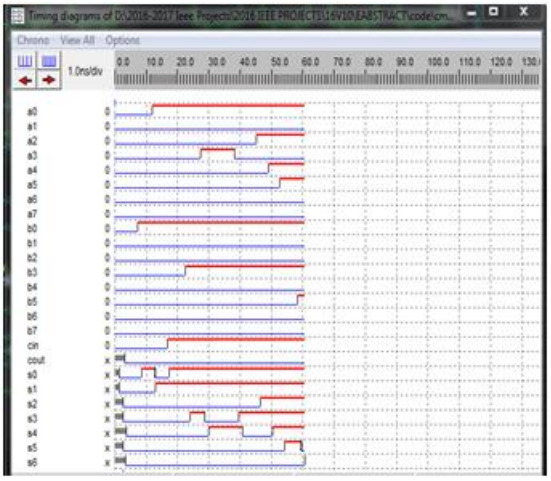

Fig 11: Timing Diagram of 8bit Brent Kung Adder using CMOS

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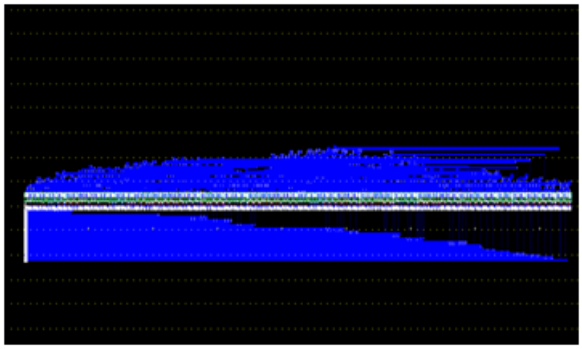

Fig 12: Layout of 8bit Brent Kung Adder using CMOS

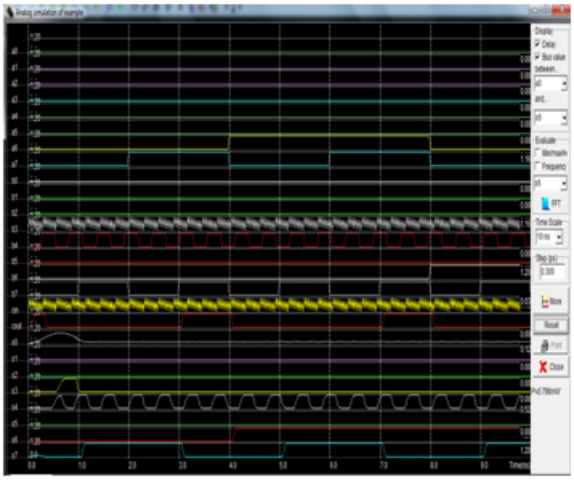

Fig 13: Simulation of Layout of 8bit Brent Kung Adder using CMOS

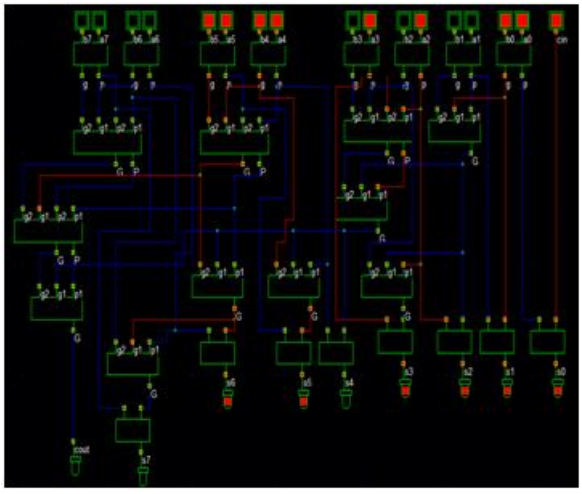

Fig 14: Schematic of 8bit Brent Kung Adder using GDI

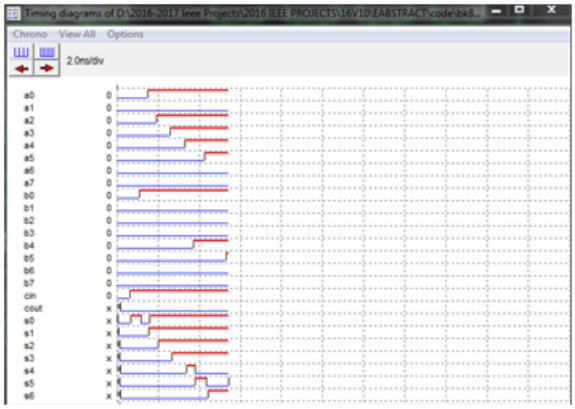

Fig 15: Timing Diagram of 8bit Brent Kung Adder using GDI

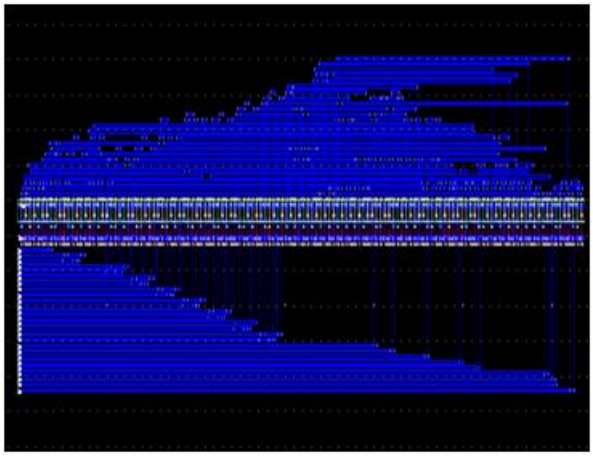

Fig 16: Layout of 8bit Brent Kung Adder using GDI

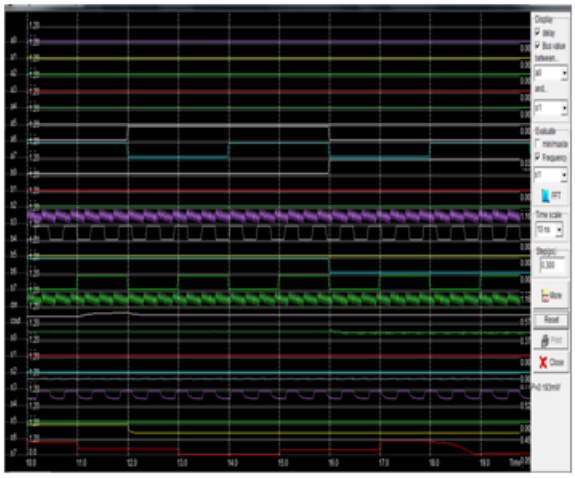

Fig 17: Simulation of Layout of 8bit Brent Kung Adder using GDI

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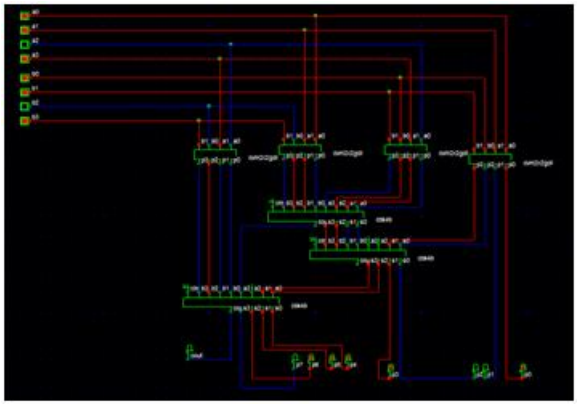

Fig 18: Schematic of 4bit Vedic Multiplier using Brent Kung Adder GDI

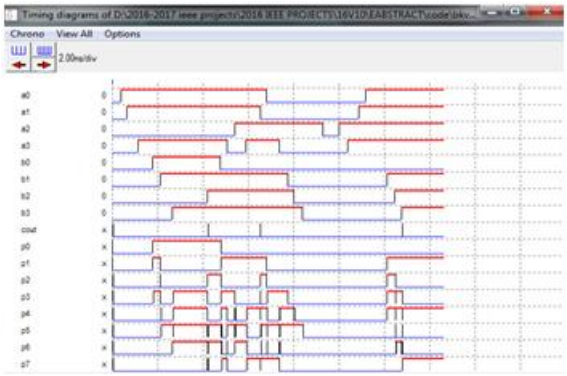

Fig 19: Timing Diagram of 4bit Vedic Multiplier using Brent Kung Adder GDI

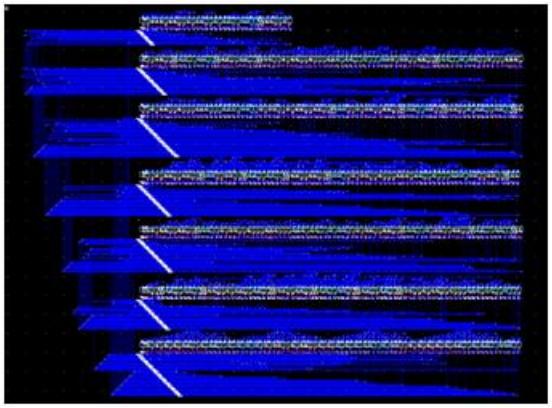

Fig 20: Layout of 4bit Vedic Multiplier using Brent Kung Adder GDI

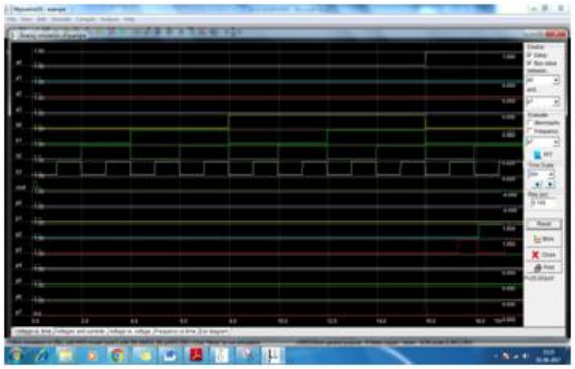

Fig 21: Simulation of Layout of 4bit Vedic Multiplier usingBrent Kung Adder GDI

B. COMPARATIVE ANALYSIS The comparative analysis of the various adders with performance measure as Number of transistor, Power and Delay is coated here. Form the comparative analysis it is clear that the CMOS design gives a less power consumption compared to GDI design style, and the GDI design gives less delay and consumes less number of transistor compared to CMOS design style.

Table:1 Comparisons results of 8Bit Brunt Kung Adder Using CMOS and GDI

	PARAMETERS		
DESIGN	Area	DEALY	Power
CMOS	511x28uw	0.50ns	0.789mW
GDI	192x29	0.33ns	0.194mW

V.CONCLUSION

Adders are core and essential block in many modules which involves computation and adders play a vital role in the design of multipliers using adder based logic, hence the design and implementation of the adders is a prime concern, In this paper we have designed, modeled the different adders like RCA, KSA, BKA used in Vedic Multiplier design and coated comparative results obtained. From the results it is clear that the adders designed using GDI design style give less delay and consumes less number of gate count, CMOS design style give less power consumption, as these the performance parameters are prime concerned while designing a module.

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Hence the choice has to be made and as per the desire of the designer and the prime concern of performance measure needed at that point intime.design of multiplier employing adder can use adders coated here, at the initial stages the GDI based adder can be used to optimize area and delay, where as the CMOS design based adder can be used at the final stage to balance on the power state. The highlighted part of the design coats the parameter which is best in the given design style, based on this the designer can select adder as per the requirement.

REFERENCES

[1]Mr. Kunjan D. Shinde, Mrs. Jayashree C. N."Modeling, Design and Performance Analysis of Various 8-bit Adders for Embedded Applications", Proceedings of the ELSEVIER in International Conference onEmerging Research in Computing, Information, Communication and Applications (ERCICA-14)" at NitteMeenakshi Institute of Technology, Bangalore, Karnataka, India. 01st and 02nd August 2014, ISBN 9789351072621, pp. 823 to 831.

[2]Mr. Kunjan D. Shinde, Mrs. Jayashree C. N. "Design of Fast and Efficient 1-bit Full Adder and its Performance Analysis",Proceedings of the IEEE International Conference on "Control, Instrumentation, Communication and Computational Technologies (ICCICCT-2014) " at Noorul Islam University, Kumaracoil, Kanyakumari, Tamilnadu, India. 10th and 11th July 2014, IEEE Digital Xplore ISBN 978-1-4799-4191-9, pp. 1275 to 1279.

[3]Mr. Kunjan D. Shinde, Mrs. Jayashree C. N. "Comparative Analysis of 8-bit Adders for Embedded Applications", Proceedings of the IJERT in National Conference on "Real Time System (NCRTS-14)" at City Engineering College Bangalore, Karnataka, India. 9th and 10th May 2014, ISSN- 2278-0181 pp. 682 to 687, NCRTS'14 Conference Proceedings, IJERT publication

[4]Mr.Nurdiani Zamhari, Mr. Peter Voon, Miss/Mrs.Kuryati Kipli, Mr.Kho Lee Chin, Mr.Maimun Huja Husin, "Comparison of Parallel Prefix Adder (PPA)",proceedings of the World Congress on Engineering 2012 Vol IIWCE 2012, July 4 - 6, 2012, London, U.K.

[5]Anas Zainal Abidin, Syed Abdul Mutalid Al Junid, Khairul Khaizi Mohd Sharif, "A survey on 4 bit Brent kung PPA simulation study using silvaco EDA Tools".

[6]Avinashshrivastava, Chandrahas Sahu, "Performance Analysis of PPA based on FPGA, International Journal of engineering trends and techonology (IJETT)-volume 21,number 6-march 2015.