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A Review on Primitive Components of Reversible Logic Gates for Synthesis

M.Ranjith Reddy, M.Tech
Assistant Professor,
Siddartha Institute of Technology & Science.

Siri Chandana.G
M.Tech,
Siddartha Institute of Technology & Science.

Abstract:
In this paper a primitive components of reversible logic gates are synthesized. The development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. On the other hand, reversible logic circuits can decrease energy dissipation theoretically to zero. Thus power consumption is a prime target now days. Needless to say, researchers will now look at reversible logic in this vein. Primitive component of reversible logic synthesis are reversible logic gates. Thus it is very important for a new researcher to look into extensive literature survey of reversible logic gates. Many papers have been reported with review of reversible logic gates. This paper aims on updates in reversible logic gates which are stepping stones in design and synthesis of any complex reversible logic based synthesis.

Keywords:
Reversible; Power consumption; Primitive component; Optimization metrics.

I. INTRODUCTION:

The growing technologies have increased the demand of high performance computing. According to G. Moore's low [1], number of transistor counts to be integrated per unit area in devices will almost double in one and half year. To achieve high speed computation, high packaging density in the logic circuits is required which results in more heat dissipation.

The conventional computing is found unable to deal with low power, high compaction and heat dissipation issues of the current computing environment. Recently, it has been applied to cryptography [2-10]. A circuit (gate) is called reversible if there is a one-to-one correspondence between its inputs and outputs. Research on reversible logic circuits is motivated by advances in quantum computing, nanotechnology and low-power design. Therefore, reversible logic synthesis has been intensively studied recently. The attention is focused mainly on the synthesis of circuits built from the NCT library of gates, i.e. NOT, CNOT and Toffoli gates. Classical gates like two input AND, OR, NAND, NOR, XOR and XNOR are irreversible as we can't uniquely reconstruct input states from output states. Here two bit input state is mapped to one bit output state leads to erasure of one bit and consequently loss of energy. We can avoid this energy loss by mapping n bit input states to n bit output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible.

II. BASIC PREMILIRIES :

Quantum gates or reversible gates differ from Classical gates in a way that a) quantum gates work on qubits rather than bits b) feedbacks are not permitted in reversible logic circuits made with reversible logic gates so called acyclic and c) there is no fan out allowed means several copies of qubits are not allowed. It is very important to know that out of four 1*1 one qubit gates; only two are reversible i.e. trivial gate and not gate. Similarly out of 256 possible 2*2 two qubit gates; only 24 are reversible as shown in table 1.

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Table 1: Representation of all possible existing 24 2*2 reversible logic gates

Reversible gate	P	Q	Reversible gate	P	Q	Reversible gate	P	Q	Reversible gate	P	Q
1	A	B	7	$A \oplus B$	B	13(Feynman Gate)	A	$A \oplus B$	18	$\overline{A \oplus B}$	$\overline{B}$
2(Swap Gate)	B	A	8	B	$\overline{A}$	14	B	$A \oplus B$	20	$\overline{A \oplus B}$	$\overline{A}$
3	$A \oplus B$	B	9	$\overline{A}$	$\overline{A \oplus B}$	15	$A \oplus B$	A	21	$\overline{A}$	B
4	A	$A \oplus B$	10	$\overline{B}$	$\overline{A}$	16	$\overline{B}$	$A \oplus B$	22	$\overline{A}$	$\overline{B}$
5	$\overline{A \oplus B}$	A	11	$A \oplus B$	$\overline{B}$	17	A	$\overline{B}$	23	$A \oplus B$	$\overline{A}$

III. NCV GATE LIBRARY:

NCV gate library contains following set of quantum gates i.e. NOT gate, CNOT gate and controlled V and controlled V+ gates. Controlled V and controlled V+ gates are basically types of controlled square root of NOT gates. In both of these gates, when control input is 0 then second input is propagated as it is to output, Two V gates in series operation becomes CNOT gate or inverter. Similarly two V+ gates activated in series operation becomes CNOT or inverter gate and one V and another V+ gate in series operation become an Identity gate or buffer. Here block diagram of a 2*2 reversible gate is presented in Fig.1.1 with A and B as input and P and Q as output. Here quantum implementation of NOT gate, CNOT gate and Controlled V and controlled V+ gates is given in Fig 1.2, Fig 1.3, Fig 1.4 and Fig 1.5 respectively .Quantum implementation of integrated qubit gates can be implemented by cascading quantum implementation of CNOT gate with controlled V gate or with controlled V+ gate.

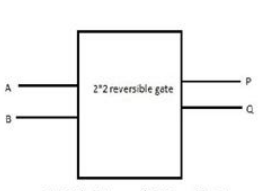


Fig 1.1:Block Diagram of 2*2 Reversible Gate

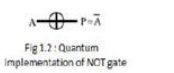


Fig 1.2 : Quantum Implementation of NOT gate

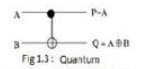


Fig 1.3 : Quantum Implementation of CNOT gate

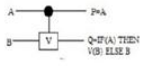


Fig 1.4 : Quantum Implementation of controlled V gate

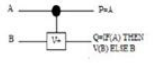


Fig 1.5: Quantum Implementation of controlled v+ gate

IV. PREMITIVE REVERSIBLE LOGIC GATES

There exist 16777216 different 3*3 three qubit gates however number of reversible 3*3 gates is much smaller i.e.40320.

Here fundamental 3*3 Reversible logic gates and other popular 3*3 reversible logic gates are described in Table 2 and Table 3 respectively with their logic expression, quantum cost, special feature respectively.

Table 2: Fundamental 3*3 Reversible Logic gates

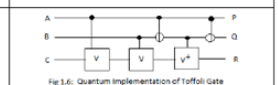
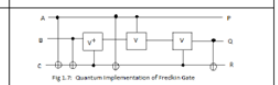
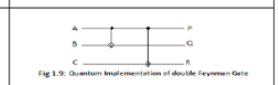
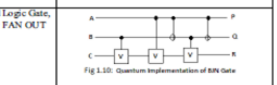
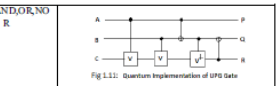
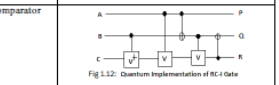
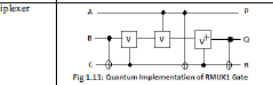
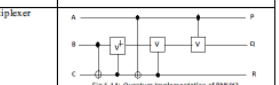
Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*	*Quantum Implementation*
Toffoli/CCNOT Gate[3]	3*3	P = A Q = B $R = AB \oplus C$	5	Universal Reversible Logic Gate	 Fig 1.6: Quantum implementation of Toffoli Gate
Fredkin Gate/CSWAP Gate[4]	3*3	P = A $Q = \bar{A}B \oplus AC$ $R = \bar{A}C \oplus AB$	5	Universal Reversible Logic Gate, Parity Preserving Reversible Logic Gate	 Fig 1.7: Quantum Implementation of Fredkin Gate
Peres Gate/NTG[5]	3*3	P = A $Q = A \oplus B$ $R = AB \oplus C$	4	Lowest Quantum Cost	 Fig 1.8: Quantum Implementation of Peres Gate
Double Feynman Gate[6]	3*3	P = A $Q = A \oplus B$ $R = A \oplus C$	2	Parity Preserving Reversible Logic Gate	 Fig 1.9: Quantum Implementation of double Feynman Gate

Table 3: Other popular 3*3 Reversible Logic Gates

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*	
BJN/MTG Gate[7]	3*3	P = A Q = B $R = (A + B) \oplus C$	5	Universal Logic Gate, Used for FAN OUT	 Fig 1.10: Quantum Implementation of BJN Gate
YAG/UPG Gate[8]	3*3	P = A $Q = (A \oplus B) \oplus (AB \oplus C)$ $R = AB \oplus C$	4	AND,NAND,OR,NOR	 Fig 1.11: Quantum Implementation of UPG Gate
RC-1 Gate[9]	3*3	P = A $Q = \bar{A}B \oplus C$ $R = A\bar{B} \oplus C$	4	1 bit comparator	 Fig 1.12: Quantum Implementation of RC-1 Gate
RMUX1 Gate[10]	3*3	P = A $Q = \bar{A}B + AC$ $R = \bar{A}C + A\bar{B}$	4	Multiplexer	 Fig 1.13: Quantum Implementation of RMUX1 Gate
RMUX2 Gate[10]	3*3	P = A $Q = \bar{A}B + AC$ $R = (A \oplus B) \oplus C$	4	Multiplexer	 Fig 1.14: Quantum Implementation of RMUX2
BR Gate(TRG)[11]	3*3	P = A $Q = A \oplus B$ $R = AB \oplus C$	4	Subtractor	 Fig 1.15: Quantum Implementation of TR Gate
MRG Gate[12]	3*3	P = A $Q = A\bar{B} \oplus A\bar{C}$ $R = A\bar{C} \oplus AB$	4	Universal Logic Gate with reduced quantum cost	 Fig 1.16: Quantum Implementation of MRG Gate

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To justify quantum cost; Quantum implementation of logic gates is also given. Table 4 describes all popular 4*4 reversible logic gates and to justify quantum cost, quantum implementation is also given. Table 5 describes 5*5 reversible logic gates and to justify quantum cost, quantum implementation is also given.

Table 4: Popular 4*4 Reversible Logic Gates

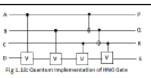
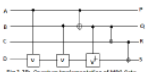
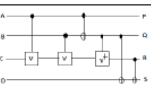
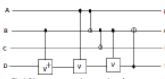
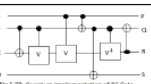
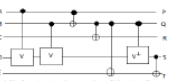
Reversible Logic Gate	Specification	Expression	Quantum Cost	Feature	
Double Peres/MTSG Gate/DPG/PFAG[13]	4*4	P = A Q = A⊕B R = A⊕B⊕C S = [A ⊕ B)C ⊕ AB ⊕ D	6	Reversible Full Adder Gate	
HNG Gate[14]	4*4	P = A Q = B R = (A⊕B)⊕C S = (A⊕B)C ⊕AB ⊕D	6	Reversible Adder	
MRG Gate [15]	4*4	P = A Q = A ⊕ B R = A⊕B⊕C S = (AB⊕D)⊕ ((A⊕B)⊕C)	6	OR,NOR,XOR,XNOR	
PAOG Gate[15]	4*4	P = A Q = A ⊕ B R = AB⊕C S = (AB⊕C)⊕((A⊕B)⊕D)	6	OR,NOR,AND,NAND	
RC-II Gate [9]	4*4	P = A Q = AB⊕D R = A⊕B⊕C S = AB⊕D	5	Reversible 4x4 comparator	
RC Gate[15]	4*4	P = A Q = (A⊕B)⊕(B⊕AB) R = B⊕C⊕AB S = A⊕B⊕D	5	Comparator	

Table 5: 5*5 Reversible Logic Gate

Reversible Logic Gate	Specification	Expression	Quantum Cost	Feature	
Morrison Gate[15]	5*5	P = A Q = A ⊕ B R = (A⊕B)⊕C S = AB ⊕D T = ((A⊕B) ⊕E)⊕(AB⊕D)	7	OR,AND	

V. SIMULATION RESULTS

All the synthesis and simulation results of the proposed 5x5(Morrison) Reversible Logic Gates are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.7. The corresponding simulation results of the proposed 5x5(Morrison) Reversible Logic Gates are shown below.

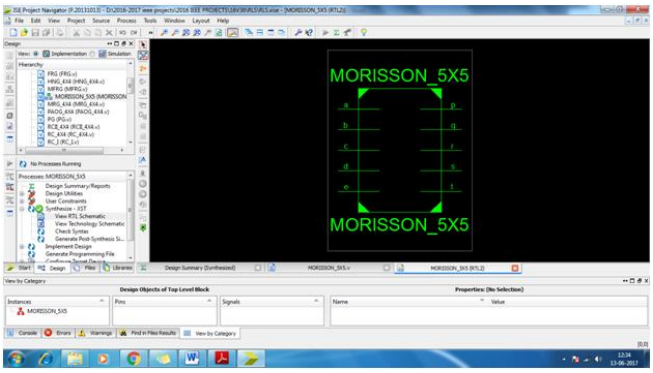


Figure 2: RTL schematic of Top-level of proposed 5x5(Morrison) Reversible Logic Gate

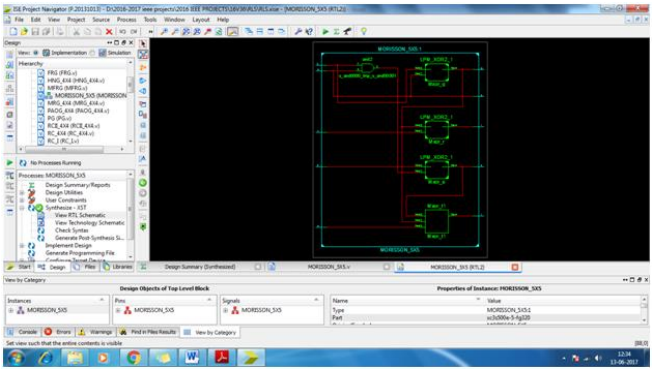


Figure 3: RTL schematic of Internal block of proposed 5x5(Morrison) Reversible Logic Gate

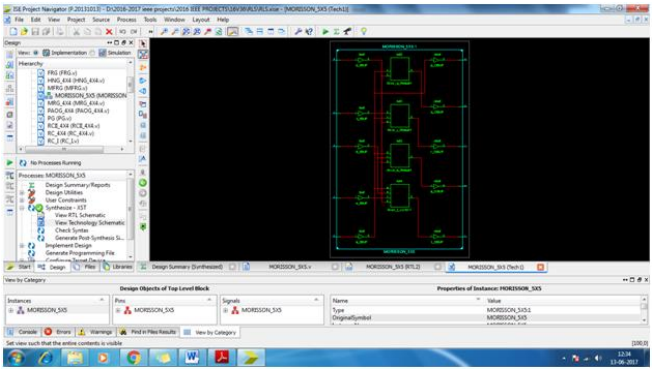


Figure 4: Technology schematic of Internal block of proposed 5x5(Morrison) Reversible Logic Gate

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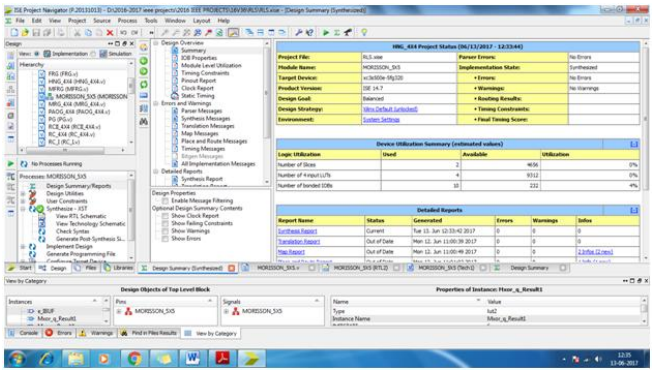

Figure 5: Synthesis report of proposed 5x5(Morrison) Reversible Logic Gate

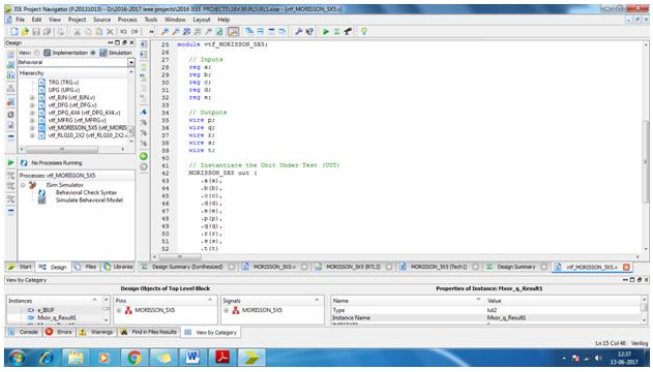

Figure 6: Test Bench for proposed 5x5(Morrison) Reversible Logic Gate

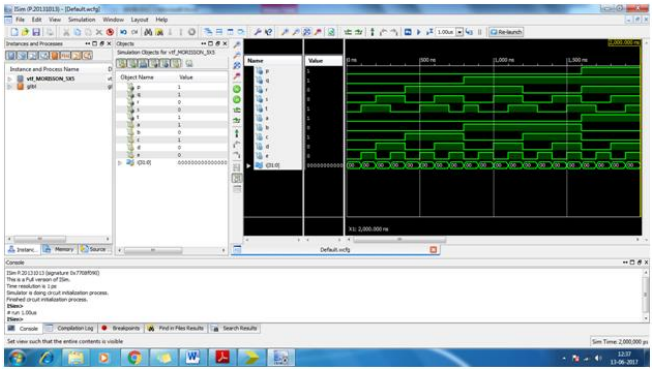

Figure 7: simulated outputs for proposed 5x5(Morrison) Reversible Logic Gate

VI. CONCLUSION:

In this paper all the 2x2, 3x3, 4x4 and 5x5 reversible logic gates for synthesis coded in Verilog HDL. All the synthesis and simulations are evaluated on Xilinx ISE 14.7.

This paper aims not only on updates in reversible logic gates with their expressions, special features and quantum cost but also on their quantum implementation to justify quantum cost which are stepping stones in design and synthesis of any complex reversible logic based synthesis. A new researcher may begin with basics of reversible logic gates and implement optimum reversible logic circuit based on various optimization metrics like ancillary inputs, garbage outputs, quantum cost.

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