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Transistor Level Implementation of Vedic Multiplier by Using GDI Method

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ABSTRACT

Low power design has significant importance in digital VLSI circuits. Speed and power efficient implementations of multipliers are very challenging. The increase in complexity of VLSI systems and minimizing power consumption has clearly become a priority. The processor performance depends upon the power and delay, as we get less the effective processor. The proposed paper consists of the transistor level implementation of Vedic multiplier using Urdhva Tiryakbhayam (uv) sutra. This low power Vedic multiplier designed by using the GDI technique. So, these GDI based design of multipliers may reduce power consumption compared to that of design in CMOS. These low power designs are realized in MICROWIND TOOL schematic tool.

INTRODUCTION

The primary semiconductor device held one transistor each. The consequent advances included an ever increasing the transistor count, as consequences, more individual functions or systems were integrated over time. The ICs held not only some gadgets many gadgets like ten diodes, transistors, resistors and capacitors, are fabricated on a unmarried device. In "small-scale integration" (SSI), improvements a technique to gadgets with hundreds of good judgment gates, referred to as massive-scale integration (LSI), i.e. system does contain the thousand logic gates. Current innovation has moved far past this stamp and present chip have many gates and millions of individual transistors.

At one time, there has been an effort to name and regulate exceptional degrees of large-scale integration above VLSI. phrases like extremely-massive-scale Integration were applied. Terms like Ultra-large-scale Integration (ULSI) were utilized. Gigantic number of gates and transistors are accessible on regular devices has rendered such refinements are disputable.

Terms proposing more noteworthy than VLSI levels of joining are no longer in far reaching use. Indeed, even VLSI is presently to some degree interesting, given the regular suspicion that all microchips are VLSI or better.

Began at mid 2008, billion-transistors are monetarily available, a case of which is Intel's Montecito Itanium chip. this is relied upon to turn out to be rather more normal as semiconductor creation moves from the present era of sixty five nm methods to the subsequent forty five nm eras (while encountering new difficulties, for example, expanded variety crosswise over process corners). Another remarkable case is NVIDIA¨s 280 arrangement GPU.

The chip is one of a kind in the way that its 1.4 Billion transistor count, able to a teraflop of execution, is absolutely committed to good judgment (Itanium's transistor depend is essentially because of the 24MB L3 cache). cutting-edge designs, as disagreed to the earliest devices, use substantial design automation and automatic common sense synthesis to lay out the transistors, enabling higher stages of complexity within the good judgment resulting capability. Certain superior rationale squares like the SRAM cell, in any case, are as yet composed by hand to guarantee the most noteworthy proficiency (now and again by bowing or breaking built up configuration standards to acquire the last piece of execution by exchanging security).

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VLSI DESIGN

The complexity of VLSIs being composed and utilized now a days makes the guide way to format impractical. Layout automation is the order of the day. With the quick innovative advancements in the past two decades, the status of VLSI technology is characterized by the following:

- A enduring increment in the size and as a result the functionality of the ICs.
- A regular discount in characteristic length and ultimately increase in the pace of operation as well as gate or transistor density.
- A consistent change in the consistency of circuit conduct.
- A consistent increment in the assortment and size of software tools for VLSI design.

The above improvements have brought about an expansion of ways to deal VLSI design. We briefly describe the procedure of automated design flow [Rabaey, Smith MJ]. The main point more to draw out the part of a Hardware Description Language (HDL) in the design process. An abstraction based model is the basis of the automated design.

Abstraction Model

The model partitions the entire outline cycle into different areas. With such a reflection through a division procedure the outline is done in various layers. The planner at only one layer may work without making a big deal about the layers above or underneath. The thick level lines isolating the layers in the figure imply the compartmentalization. For instance, let us examine the outline at the gate level. The circuit to be planned would be portrayed regarding truth tables and state tables. With these as accessible sources of info, he needs to express them as Boolean rationale conditions and acknowledge them as far as doors and flip-flops. Thusly, these shape the contributions to the layer instantly beneath. Compartmentalization of the way to deal with plan in the way portrayed here is the embodiment of reflection; it is the reason for advancement and utilization of CAD devices in VLSI outline at different levels. The plan techniques at various levels utilize the individual guides, for example, Boolean conditions, truth tables, state move table, and so on. Be that as it may, the guides assume just a little part all the while. To finish an outline, one may need to change starting with one device then onto the next, raising the issues of hardware similarity and adapting new situations.

ASIC DESIGN FLOW

Some other specialized technique, development of an ASIC begins with an thought and takes substantial shape through the stages of development. The initial step in the process is to grow an idea in terms of behavior of the target circuit. Through stages of programming, the same is fully advanced into a design description in terms of well described trendy constructs and conventions.

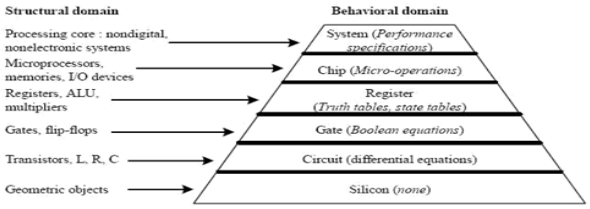
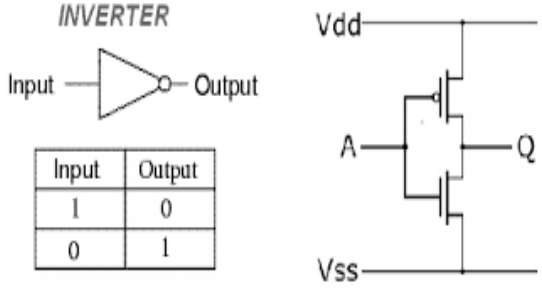


Fig: Design Domain and Level of Abstraction

EXISTED SYSTEM:

CMOS Full Adder:

The inverter is generally accepted as the most essential logic gate doing a Boolean operation on a single input variable. The representation of CMOS inverter and its truth table shown below, the CMOS inverter is a combination of both PMOS and NMOS.



Input	Output
1	0
0	1

Fig: Cmos Inverter Symbol and Truth Table

Complementary metal oxide semiconductor (CMOS) is a era for building integrated circuits. CMOS era is used in microcontroller, microprocessor, recollections and other

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digital circuits. Many styles of verbal exchange CMOS era is also utilized in analog circuits which include picture sensors (CMOS sensors), data converters, and relatively integrated transceivers. The CMOS inverter sometimes referred to as COS-MOS. The phrases "complementary-symmetry" refers that the digital layout fashion of CMOS inverter use as a complementary and symmetrical pairs of each p-type and n-type metal oxide field effect transistors (MOSFETs) for logic functions. CMOS inverter having the characteristics of high noise immunity and low static power consumption. CMOS circuits are built in such a way that each one PMOS transistors must have either an enter from the voltage source or from every other PMOS transistor.

Inverter Dynamic Characteristics:

The dynamic traits of a CMOS inverter. The accompanying are a few formal definitions of temporal parameters of digital circuits. All percentages are of the regular nation values.

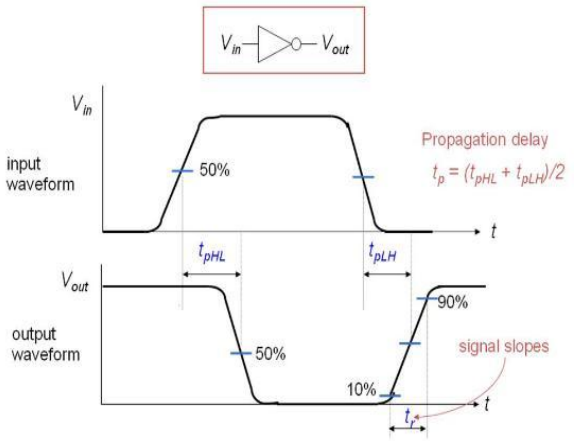

Fig : Dynamic Characteristics Of Cmos Inverter

PSEUDO Transmission Gate Full Adder:

It operates on pseudo reason, that is referred to as an ratioed fashion. This complete adder cellular makes use of 19 transistors to understand the terrible addition characteristic. The advantages of pseudo nMOS adder cellular is its higher velocity (in comparison to traditional full adder) and less transistor be counted. The downside of pseudo nMOS mobile is the static power usage of the PMOS transistor as well as the reduces the output voltage swing, which makes this adder cell more susceptible to noise. To increase the output voltage swing, CMOS inverter is added to this circuit.

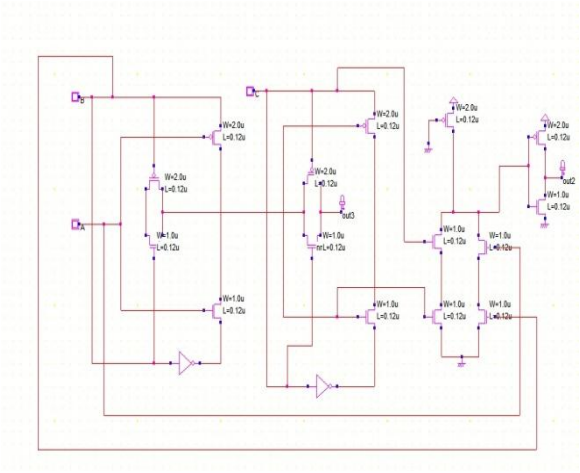

Fig : Pseudo Transmission Gate Fa

PROPOSED SYSTEM:

In the proposed design iam implementing a GDI full adder. As compared to existed system it consumes less area, it requires less number of transistors. By using this implementing a 2-bit and 4-bit Vedic multiplier by using GDI technique.

Basic GDI cell:

A new technique of low-strength virtual combinational circuit layout. GDI method can allows lowering strength intake, propagation put off, and region of digital circuits whilst designing a low complexity of common sense layout. Pass-transistor good judgment has been exhibited for NMOS. They are primarily based on the version, in which a hard and fast of manipulate indicators is implemented to the gates of NMOS transistors. Another arrangement set of information signals are applied to the sources of the n-transistors. A number of the main blessings of PTL over standard GDI layout are excessive pace, due to the small node capacitances.

- Low strength dissipation, due to the reduced range of transistors.
- Decrease interconnection because of a small vicinity.

However, a large portion of the PTL usage have two basically issues:

They are:

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Since the "high input voltage level at the regenerative inverters is not VDD, the PMOS device within the inverter isn't always fully turned off, and consequently Direct-route static energy dissipation may be big.

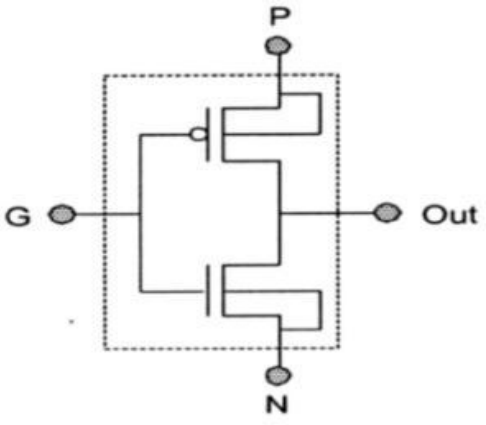

Fig: GDI Cell

Simulation and Result:

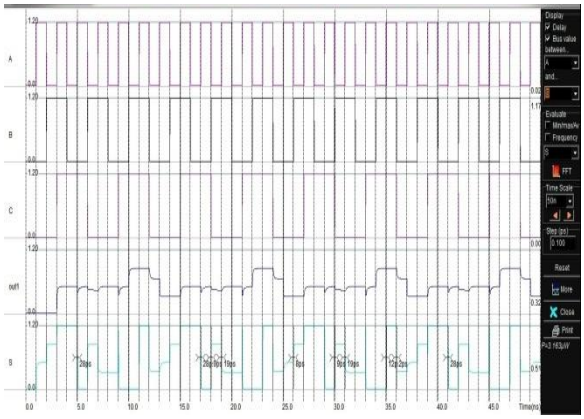

Fig: GDI Full Adder Simulation

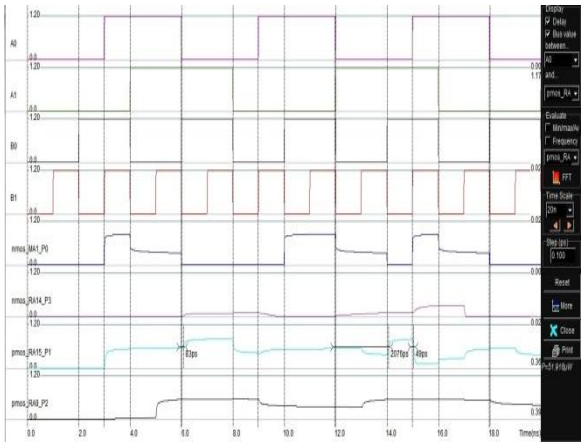

Fig: 2-Bit Vedic Multiplier Simulation

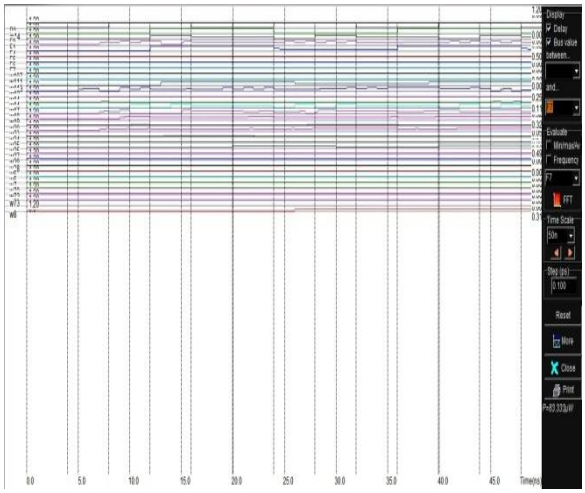

Fig: 4-Bit Vedic Multiplier Simulation

RESULT

The existed system is compared with the GDI full adder. It requires less area, power dissipation, delay and it required less number of transistors.

PARAMETER	EXISTED SYSTEM			PROPOSED SYSTEM
	CMOS FA	TG FA	TG PSUEDO FA	GDI
AREA (µm2)	544	280	273	98
POWER DISSIPATION (µw)	45.35	33.56	19.33	3.16
NO.OF TRANSISTORS	28	16	19	14
DELAY(ns)	1.76	4.28	1.15	0.6

TABLE: Comparison between the Existed and Proposed Design

By using the GDI full adder designing a 2-bit and 4-bit vedic multiplier.

PARAMETER	AREA(µm2)	POWERDISSIPATION(µw)	DELAY(ns)
GDI FULL ADDER	98	3.16	0.6
2-BIT VEDIC MULTIPLIER	286	51.83	1.23
4-BIT VEDIC MULTIPLIER	3366	83.33	4.370

TABLE: Proposed Design Outputs

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CONCLUSION

Multiplication plays important role in the processors. A Multiplier is designed by using the adder circuit. In this paper CMOS full adder, Transmission gate, Pseudo transmission gate full adder and GDI full adder circuits can be implemented. By comparing all adder circuits GDI full adder is most efficient as compared to all the designs. For the further design GDI full adder is used. In this paper 2-bit and 4-bit Vedic multiplier is proposed using Urdhva Tiryakbhayam sutra by using the GDI full adder method.

In this project for simulation and for synthesis MICROWIND tool is used using target technology and performing placing & routing operation for system verification.

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