

Design of an Efficient Full Adder for Low power Applications

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ABSTRACT:

Adders are the key building blocks of the ALU circuit. Arithmetic and logical unit plays a very important role in any of the systems. Any changes to adder circuit directly affect on the processor. By using proposed system it gives low power dissipation, more accuracy and at the same time it gives the fast of operation because we are reducing the transistors. The proposed system gives high speed with low area consumption. So compare to existed method the proposed method gives the better performance in terms of power delay and area. Instead of utilizing the more transistors here, we are using less transistors for the same work then we get the less area and at the same time concentrating on power dissipation and performance.

Keywords: Full adder, Adiabatic, GDI, and PTL logic.

INTRODUCTION:

Modern System-on-Chip demand for more power in both logic and memory, Static power is growing really fast and Dynamic power kind of grows. Overall power is dramatically increasing. If the semiconductor integration continues to follow Moore's Law, the power density inside the chips will reach far higher than the rocket nozzle. Power dissipation is the main constrain when it comes to Portability. The mobile device consumer demands more features and extended battery life at a lower cost. About 70% of users demand longer talk and stand-by time as primary mobile phone feature. Top 3G requirement for operators is power efficiency. Customers want smaller & sleeker mobile devices. This requires high levels of Silicon integration in advanced processes, but advanced processes have inherently higher leakage current. So there is a need to bother more on reducing leakage current to reduce power consumption.

In order to reduce the power consumption of a circuit in this paper I am designing a Full Adder using Pass Transistor Logic. This PTL logic full adder is compared with CMOS full adder, Adiabatic Full Adder and GDI based full adder. From the outcomes of these circuits PTL logic Full Adder consumes less power and require less area.

EXISTED SYSTEM

In existed system, a basic CMOS full adder is used to design a carry skip adder which contains 28 transistors in a single full adder. Four full adders, one multiplexer and one AND gate is used to design a CSKA in previous method. Using a CMOS full adder a CSKA is created with 28 transistors for each full adder. It makes a circuit more complex, more delay and area also more. The below figure 2.1 shows the basic diagram of a full adder.

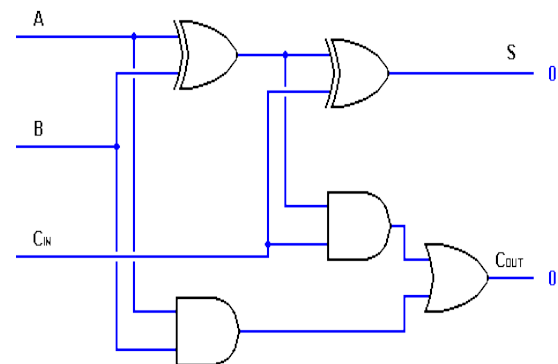


Figure: 2.1 A basic full adder diagram

A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers.

The full adder produces a sum of the two inputs and carries value. It can be combined with other full adders or work on its own. The below table 2.1 shows the truth table of a Full Adder.

INPUT			OUTPUT	
CIN	A	B	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2.1 Full Adder truth table

Note that the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. This is because the only difference between OR and XOR gates occurs when both inputs are 1; for the adder shown here, this is never possible. Using only two types of gates is convenient if one desires to implement the adder directly using common IC chips.

However, they are absolutely valuable in working up bigger circuits; for example, various piece input adders and multipliers. The adder is a champion among the most essential fragments of a processor, as it is used as a piece of Arithmetic Logic Unit. An adder is a digital circuit that performs addition of numbers.

In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

The operation of CMOS full adder is same as the basic full adder circuit. It contains 28 transistors for a single full adder.

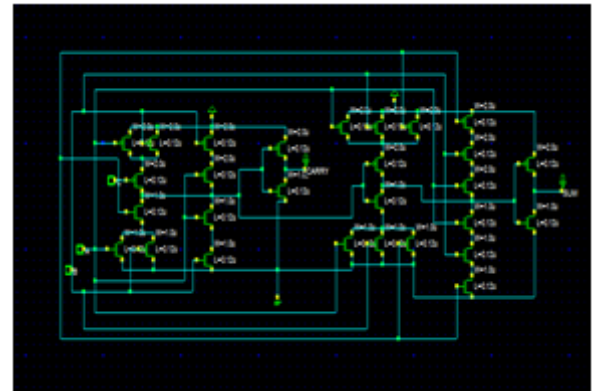


Figure: 2.2 A CMOS full adder

Schematic diagram of a CMOS full adder is shown in the figure 2.2. Given the three 1-bit inputs A, B, and C_{in} , it is desired to calculate the two 1-bit outputs Sum and Carry, where

$$\text{Sum} = (A \text{ XOR } B) \text{ XOR } C_{in}$$

$$\text{Carry} = A \text{ AND } B + C_{in} (A \text{ XOR } B)$$

The above table shows the possible combinations of inputs and their outputs of a Full Adder. In order to reduce power dissipation and delay mainly I am concentrating to reduce the number of transistors.

ANALYSIS OF DIFFERENT LOGIC STYLES TO DESIGN FULL ADDER

Adiabatic Logic

The process of adiabatic logic gate is classified into two distinct stages: one stage is used for logic evaluation; and the other stage is used to reset the gate output logic value.

Conventional Switching

There are three noteworthy wellsprings of energy dispersal in computerized CMOS circuits: those are dynamic, short out and spillage control scattering. The prevailing part is dynamic power scattering and is because of charging, releasing of load capacitance.

Adiabatic Switching

Adiabatic exchanging can be accomplished by guaranteeing that the potential over the exchanging gadgets is kept subjectively little. This can be accomplished by charging the capacitor from time

shifting voltage source or consistent current source. In writing, adiabatic rationale circuits arranged into two sorts: full adiabatic and semi or halfway adiabatic circuits. By using the adiabatic logic a full adder is implemented and the figure 3.1 shows the schematic digarm of a adiabatic full adder.

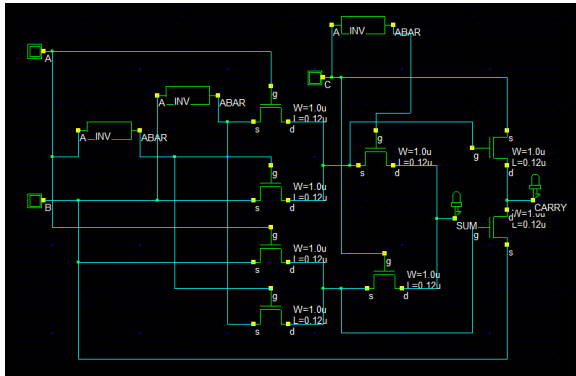


Figure 3.1 Adiabatic Full Adder

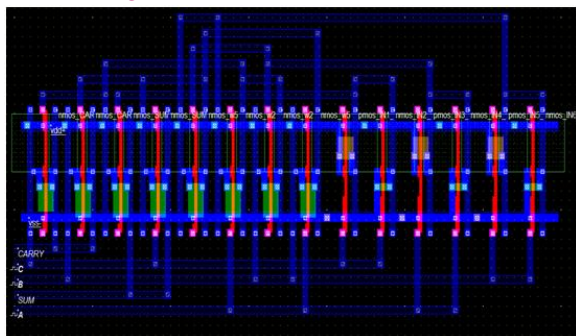


Figure 3.2 Layout diagram of adiabatic logic full adder

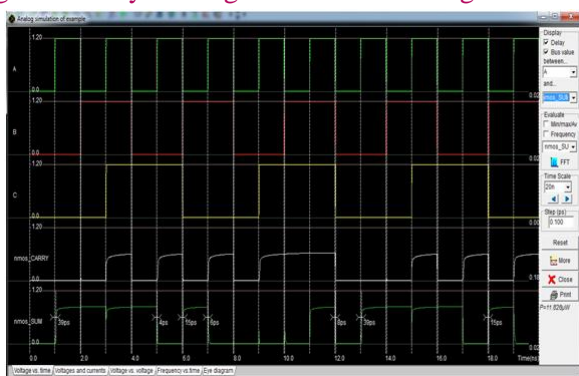


Figure 3.3 Timing diagram of a adiabatic logic full adder and 3.2 shows the layout diagram of adiabatic fulladder.

The above figure 3.3 shows the timing diagram of a Adiabatic full adder circuit, Which contains three inverters and eight n mos transistors so, totally 14 transistors are used in this adiabatic logic to implement a

full adder, by using this I have reduced a area insteaded of 28 transistors i.e nothing but a cmos full adder. Compare to CMOS full adder it gives less power dissipation and less delay.

GDI Logic

Gate diffusion input (GDI) a replacement technique of low-power digital combinatorial circuit style is delineated. This system The Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in Figure7. One may be think of the CMOS inverter in the first look of this circuit, but there are some major differences in the two: (1) The GDI cell contains three inputs—G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast to CMOS inverter.

N	P	G	Out	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	\bar{A}	NOT

Table 3.1: Basic GDI cell Operation

The above table Shows that simple configuration changes in the inputs G, P, and N of the basic GDI cell can lead to very different Boolean functions at the output out. Most of these functions are complex (usually consume 6-12 transistors) in CMOS, while very simple (only 2 transistors per function) in the GDI design methodology. Meanwhile, multiple-input gates can be implemented by combining several GDI cells. The figure 3.4 shows the schematic diagram of a GDI based full adder, figure 3.5 shows the layout diagram of GDI full adder and figure 3.6 shows the GDI based full adder timing diagram.

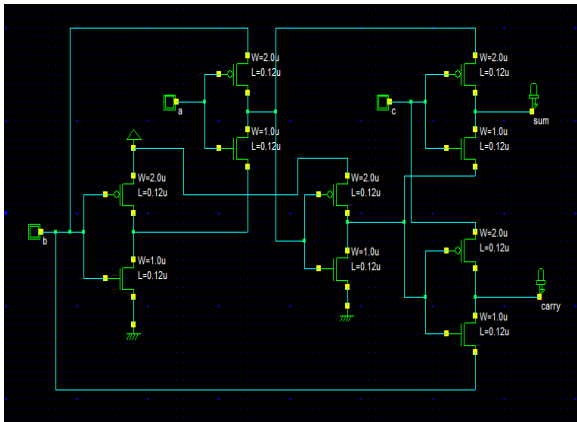


Figure: 3.4 Full adder using GDI technique

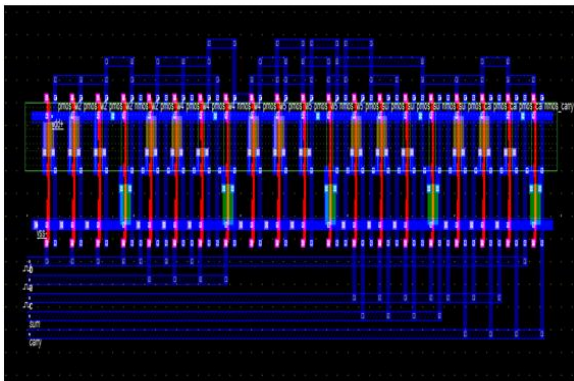


Figure 3.5 Layout diagram of a GDI full adder

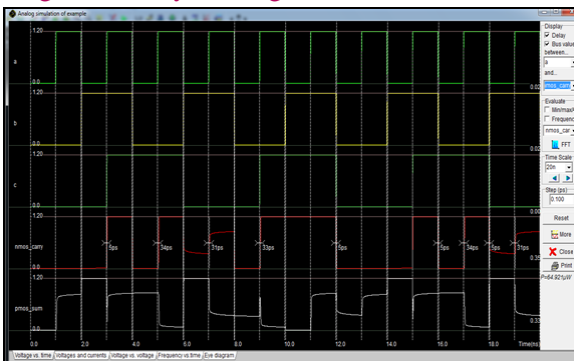


Figure: 3.6 Timing diagram of a Full Adder

**PROPOSED METHOD
 PASS TRANSISTOR LOGIC**

Pass Transistor Logic In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the number of transistors to make different logic diagrams, by neglecting redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply

voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance

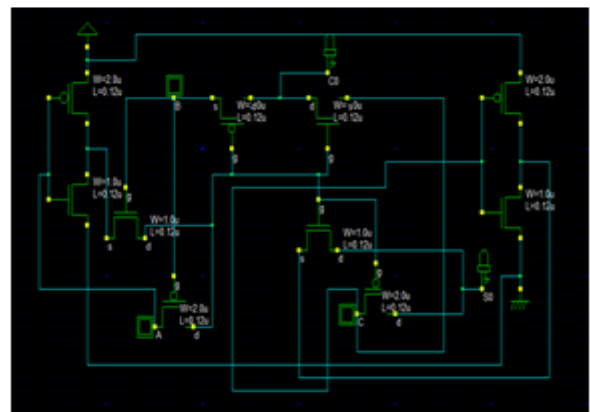


Figure: 4.1 PTL full adder

The schematic diagram of a FULL ADDER is shown in the above figure 4.1 in which Pass Transistor Logic is used so, compare to all the above technologies Pass Transistor Logic is better in terms of power dissipation, area and critical path delay.

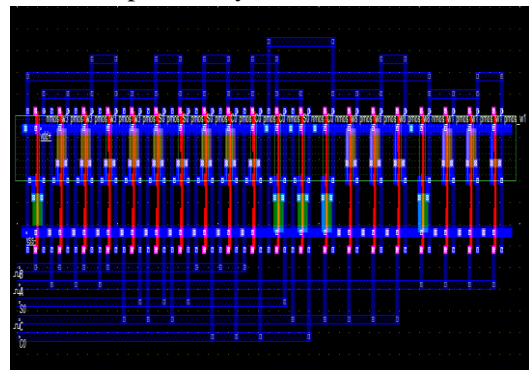


Figure: 4.2. The layout diagram of a PTL full adder

The above figure 4.2 shows the layout diagram of a PTL logic full adder.

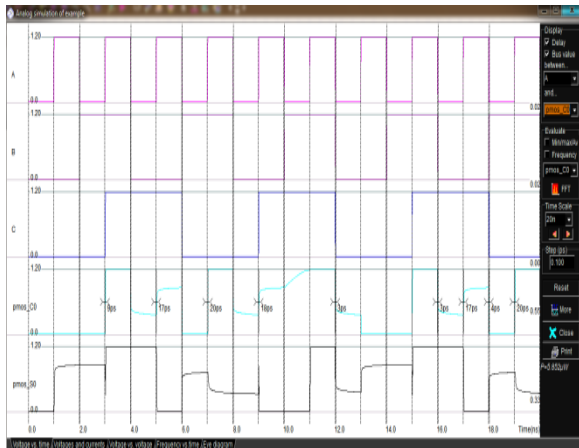


Figure: 4.3 The Timing Diagram of a PTL Full adder

The above figure 4.3 shows the timing diagram of a PTL full adder.

COMPARISON TABLE:

The below Table shows the comparisons of different logic designs in terms of power delay and number of transistors of a Full Adder.

DESIGN STYLE	NO.OF TRANSISTOR	POWER DISSIPATION	CRITICAL PATH DELAY
CMOS	28T	45.458uW	1.76nS
ADIABATIC	14T	10.24uW	0.410nS
GDI	10T	64.92uW	0.960nS
PTL	10T	5.852uW	0.550nS

Table 3.2 Comparison of different logic styles for a Full Adder

CONCLUSION

In This paper we have given a brief explanation about the different types of logic styles that are used to design VLSI circuits and also we have studied about the design of Full Adder using different logic styles, their pros and cons. Our proposed design has shown a remarkable improvement in delay, area and power whereas less

distortion has been observed than the previously designed adders. Further enhancements can be made to reduce these also. In this project we compare a different types of logic designs like Adiabatic logic and Gate diffusion Inputs logic and finally Pass Transistor Logic to the CMOS logic which is nothing but an existing method, So compare to all these logic designs Our proposed system gives the better performance and better delay and number of transistors are also reduced, but here we are mainly concentrating on the power dissipation. So, from the above analysis, we came to know that Pass Transistor logic is the best technique. So we design carry skip adder using the PTL technique because it consumes less power. So compare to previous or existed method the proposed method is better in terms of Power delay and are or the number of transistors used.

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