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Dual Threshold Voltage Design for Low Power VLSI Circuits

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ABSTRACT:
The high growth of the semiconductor trade over the past twenty years had placed VLSI in demand throughout the globe. Low power designs in VLSI have emerged as a principal theme in today's electronics industry. So, the main aim of this paper is to reduce the power consumption of a circuit. In order to reduce the power consumption of a circuit one of the low power design technique named Dual-threshold voltage technique is used. The dual-vth method profits by the characteristics of low and high threshold voltage. Low threshold voltage is assigned for critical paths and high threshold voltage for non-critical paths. Different circuits are designed using dual-threshold voltage design and there power consumption values are compared with the single threshold voltage values.

Keywords:
Low power, single-threshold voltage, Dual-threshold voltage.

INTRODUCTION:

Low power design in VLSI had evolved as the prime factor in present electronic industry. Reduction of power dissipation in the circuit had become as important as consideration as performance and area. In past, VLSI designers were thinking of parameters like performance, area, cost and reliability but power has given secondary importance. Later, this has started to change and increasingly power is being given comparable importance that has been given to area and speed considerations. Several factors had contributed to this trend. The important factor was the outstanding success and growth of PC's and wireless systems for communication which needs high-speed calculations and difficult functions with low power consumption. In these applications, average power consumed depends upon circuit design.

If there are no low-power designing techniques then, present and future movable devices will be suffered from either with less battery life or with very high battery pack. There also exists a strong pressure for producers of high-end products to reduce their power consumption. The price of packaging and cooling such devices cannot be prevented. If the power consumed by a chip is high then the expensive packaging and cooling strategies are required. Consequently, cost of production also reduces as the consumed power in high performance systems is reduced. In this paper to reduce the power consumption of a circuit Dual-threshold voltage technique is used.

Maintaining high and low threshold voltages together in a single functional unit is called Dual-threshold voltage (DUAL-Vth) Technology. Low threshold voltage value is assigned to the transistors in the critical path and high threshold voltage value for transistors in non-critical paths. Different circuits are designed using dual-threshold voltage design and there power consumption values are compared with the single threshold voltage values. From the simulation results I am going to show that dual-threshold voltage design gives better power consumption values compared to the single threshold voltage values.

THRESHOLD VOLTAGE:

The threshold voltage (vth) is generally defined as a gate voltage where at the interface an interchanging layer is formed in between the insulating layer (oxide) and the substrate of the transistor. The reason for the forming interchanging layer is by forming this layer free flow of electrons through the gate-source junction is achieved.

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FULL ADDER DESIGN USING SINGLE-THRESHOLD VOLTAGE:

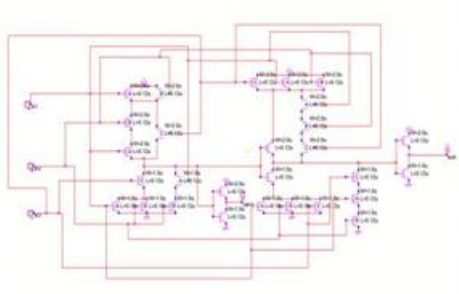

Fig.1 full adder with single threshold voltage value

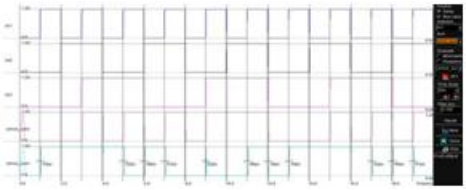

Fig.2 output waveform of the single-vth full adder

FULL SUBTRACTOR DESIGN USING XOR GATES WITH SINGLE-VTH:

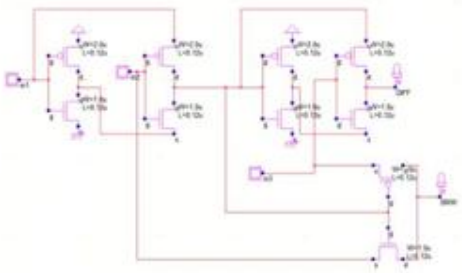

Fig.3 full subtractor design using xor gates with single-vth

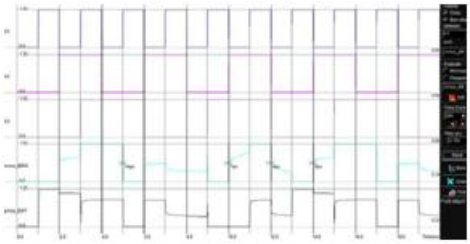

Fig.4 simulation result for full subtractor design using xor gates with single-vth

FULL SUBTRACTOR DESIGN USING XNOR GATES WITH SINGLE-VTH:

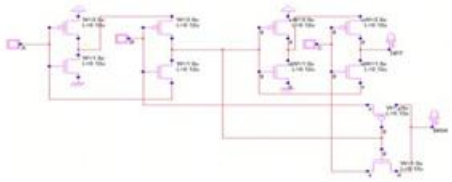

Fig.5 full subtractor design using xnor gate with single-vth

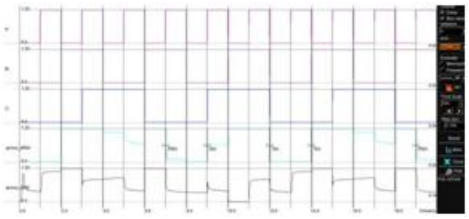

Fig.6 Simulation result for full subtractor design using xnor gates with single-vth

DUAL-THRESHOLD VOLTAGE DESIGN:

Threshold voltage (vth) denotes the value of the gate-source voltage when the charge in a MOS transistor begins to rise since the conduction layer just begins to appear. However, a transistor can likewise work effectively when a input voltage lower is applied less than its threshold voltage (Vth), which is known as sub-threshold operation or weak-inversion of a transistor. A circuit which works beneath the input voltage in the sub-threshold range is named as sub-threshold circuit. The increasing development of power-constrained electronic devices, it is more critical to suppress energy consumption in order to achieve a longer battery life. Therefore the need for design methods of low power is high. The dual-vth method profits by the characteristics of low and high vth. Higher vth results in low leakage current, thereby low leakage power consumption is achieved with the some delay. On the other hand, lower vth brings high power consumption while maintaining the speed. Dual-vth design is a common method for reducing power consumption. The vth changes with application of different source-bulk bias voltages.

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The vth when bias voltage is present can be summarized in the following equation.

$$V_{th}=V_{th}(0)+\gamma(\sqrt{|-2\phi F + Vsb|} - \sqrt{|} - 2\phi F|)$$

Where

- Vth0 is the (vth) with zero source-bulk bias voltage (V), which means that the bulk terminal is connected to ground in NMOS transistors and the bulk terminal is connected to supply voltage in PMOS transistors,
- VSB is the source-bulk bias voltage (V),
- 2ϕF is the surface potential parameter (V),
- γ is the body effect parameter($\sqrt{V}$).

DESIGNING OF FULL ADDER USING DUAL-VTH DESIGN:

The dual-vth is applied to the circuit by the following process. For a logic circuit, a higher vth is assigned to the transistors in non-critical paths and low-vth for critical paths so as to reduce the power consumption and maintain the speed. Therefore, many studies apply the dual-V_{th} technology with gate size to reduce the leakage power. Full adder using Dual- vth is shown below

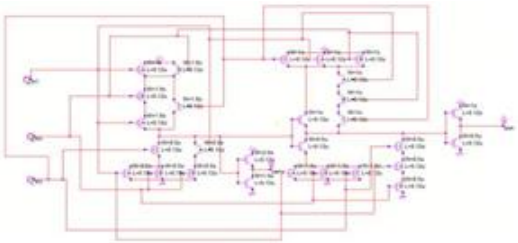

Fig.7 Full adder using Dual-vth design

In the above full adder circuit dual-vth is assigned by assigning low-vth to the transistors that are present in the critical path and high-vth to the transistors in the off-critical path. Low threshold is implemented by varying the width of the pmos and nmos transistors in the critical path. For the above circuit the width of the pmos transistors in the critical path is given as w=1 and the width of the nmos transistors in the critical path is given as w=0.5.The transistors present in the off-critical path are assigned with high-vth.

The width of pmos and nmos in off-critical path are given as w=2 and w=1. By performing this process the power consumption of the circuit can be reduced while maintaining the speed.

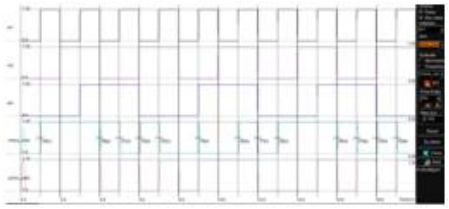

Fig.8 output waveform for the dual-vth full adder circuit

DUAL-VTH DESIGN FOR FULL SUBTRACTOR DESIGNED USING XOR GATES:

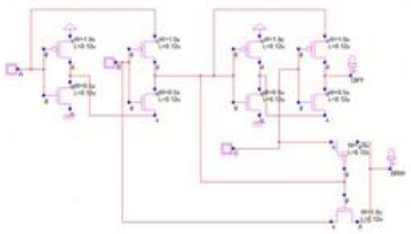

Fig.9 dual-vth design for full subtractor designed using xor gates

Full subtractor is also developed similar to the full adder. In full substractor, the transistors in the critical path are assigned with low-vth and high-vth to the off-critical path transistors. For the above circuit the width of the pmos transistors in the critical path is given as w=1 and the width of the nmos transistors in the critical path is given as w=0.5.The transistors present in the off-critical path are assigned with high-vth. The width of pmos and nmos in off-critical path are given as w=2 and w=1. By performing this process the power consumption of the circuit can be reduced while maintaining the speed.

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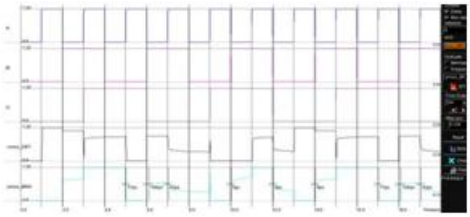

Fig.10 Simulation result for full substractor design using xor gates

DUAL-VTH DESIGN FOR FULL SUBTRACTOR DESIGNED USING XNOR GATES:

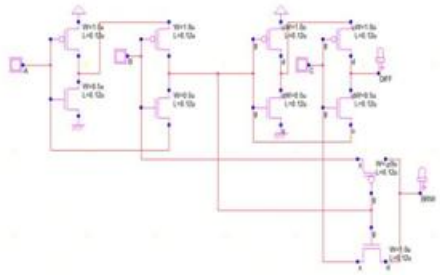

Fig.11 dual-vth design for full subtractor designed using xnor gates

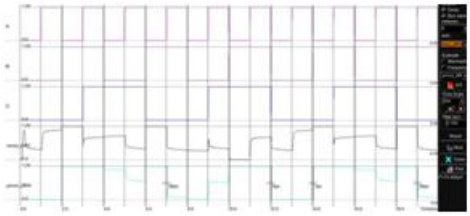

Fig.12 Output waveform for Full subtractor designed using dual-vth voltage design

COMPARISON:

Comparison of values of power for single and dual-vth voltage for full adder, full subtractor, xor and xnor circuits are listed below.

circuit	Single threshold voltage(µw)	Dual threshold voltage(µw)
Full adder	45.458	28.869
Xor	3.642	2.016
Xnor	4.234	1.934
Full subtractor using xor gate	25.296	8.643
Full subtractor using xnor gate	140	74.309

Table.1 Comparisons of values of power for single and dual threshold voltage

From the above tabular column we can see that the power consumption of circuits designed using dual-threshold voltage consumes less power when compared to the single threshold voltage.

Comparison of area:

area	Single threshold voltage(µm)	Dual threshold voltage(µm)
Full adder	759	380
Xor	99	54
Xnor	99	54
Full subtractor using xor	260	160
Full subtractor using xnor	260	160

Table.2 Comparison of area for single and dual threshold voltage design

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The above tabular column shows that by using dual-threshold voltage design not only the power consumption reduces but also area of the circuit is reduced.

CONCLUSION:

The high growth of the semiconductor trade in the course of recent years has put Very Large Scale Integration in demand throughout the globe. Previously, the chief significance's given by the designers were device size, cost of production, speed and quality. The sector of power was mostly thought of entirely inferior importance. Later it had changed and power is given more importance. Thus, the fundamental point is to diminish the power utilization of a circuit in VLSI design. In this project to decrease the power utilization of a circuit Dual-vth design technique is used. This dual-threshold voltage technique is compared with the single threshold voltage design method. To comprehend this, circuits like full adder, full subtractor, xor, xnor gates were designed. The results of these circuits are compared and from the tabular columns, we can show that dual-threshold voltage technique reduces the power consumption when compared with the single threshold voltage design.

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