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Design of 64-Bit Reversible BCD Add-Subtract Unit using Parallel and Pipelined Method

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Abstract:
In order to continue the revolution in the computer hardware performance, we need to reduce the energy dissipated in each logic operation. Energy dissipation can be reduced by preventing information loss. This is achieved by designing the circuits using reversible logic gates. Reversible logic computing is a rapidly developing research area. This paper proposes the design of 64-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 64 -bit BCD addition unit is designed using the reversible gates and propagation adder. The reversible 64-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. The reversible 64- bit BCD addition and subtraction unit is designed based on the parallel pipelined unit to enhance the speed of operation. All the synthesis and simulation results of the Proposed Reversible 64 bit BCD adder Unit and subtract Unit are performed using Verilog HDL on Xilinx ISE 14.7.

Index Terms:
Reversible logic gates; BCD adder; BCD subtractor, Reversible add-subtract unit.

INTRODUCTION:

Reversible logic is the successful option in the design of low power arithmetic unit. The reversible logic gate, which has one to one mapping innovation furnish output with zero loss of information. According to Bennett, no vitality would disseminate from a framework in the event that it is ready to come back to its underlying state from its last state paying little heed to what happened in the middle of [1].

In reversible logic gates, input vectors can be recovered from the output vectors with precision and low power dissipation. BCD utilized on different digital processors diminishes the deferral of control. BCD circuit may open new application ranges of a fund, business, arrive administration and Internet-based systems. BCD digit dispenses with the truncation error and in this way decreases the calculation delay. In this paper, BCD addition and subtraction unit has been actualized utilizing the reversible logic gates. The addition and subtraction unit is designed for 64-bit input information utilizing reversible logic gates. BCD adder and subtraction requires error correction unit which gives correct BCD output. The reversible logic gates, for example, Toffoli gate, Feynman gate, TNORG gate and URG gate are utilized as a part of the design of reversible 64-bit BCD addition unit; SBV gate, TNORG gate, URG gate, Feynman gate, Toffoli gate and COG gate are utilized as a part of the design of 64-bit reversible BCD subtraction unit.

This proposed strategy will adequately decrease the postponement, error and garbage esteem. Reversible logic gates are designed to address the issues, for example, rapid, no loss of information as warmth vitality [2]. These gates have extended its application over the wide range, for example, low power optical figuring, nanotechnology and quantum registering. One to one mapping of input and output vectors of reversible logic gates keeps the gate from loss of information as warmth vitality. Reversible logic gates diminish the loss of information while repossessing the input vectors from output vector. Input vectors of the reversible logic gates are 1‟s; the output vectors include output values and the garbage values.

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These garbage values alongside output values help in recovering the input vectors with no misfortune in information. Reversible logic gates are more powerful in executing the Boolean expressions with high exactness. Reversible logic gates don't permit fan-out while falling of reversible logic gates is conceivable [3]. This paper proposes the design of BCD adder and subtraction for 64-bit input data using reversible logic gates.

II. LITERATURE SURVEY:

In the current design, X. Susan Christina, M.Sangeetha Justine, K.Rekha, U.Subha, and R.Sumathi designed BCD addition and subtraction unit is designed using the reversible logic gates. A 4-Bit Reversible BCD addition unit is designed as the ripple carry adder, carry skip adder, carry select adder and carry look-ahead adder using reversible logic gate named NEW gate, Feynman gate, TSG gate, Toffoli gate, Fredkin gate. The similar result of reversible 4-bit BCD adder is furnished with the postponement of control. From the current module of examination carry, look-ahead adder has the most minimal deferral of control of around 456.774ns with the garbage values of 48 [4]. V. Rajmohan, V. Ranganathan, and M. Rajmohan proposed a 4-bit BCD Subtraction unit is acknowledged by getting nine's complement of one of the 4-bit input vectors and is included using the 4-bit BCD adder unit.

The reversible logic gates, for example, TKS gate, SCL gate, HNG gate, Peres gate, BVF gate have been utilized as a part of the design of 4-bit reversible BCD subtraction unit. The deferral of control of reversible 4-bit subtraction unit is evaluated in the current work is around 36ns with the garbage estimation of 37 [5]. Robert D. Kenney and Michael J. Schulte proposed the design of BCD using twofold error correction unit for addition. The addition is performed using the Carry Save Adder and Carry Propagate Adder as a tree structure with twofold error correction unit to decrease the error of control [6].

III. REVERSIBLE LOGIC GATES:

The reversible logic gates will be having n-input and n-output i.e. the meet number of input and equivalent number of output. In reversible logic, inputs can be remarkably recouped from the output. In the event that a reversible gate has k inputs, and therefore k outputs, at that point it is a k*k reversible gate. In reversible gates, fan out is not allowed, if there it must not surpass more than one. No criticism ways are permitted i.e. circuit is noncyclic. Some important factors in reversible logic are Garbage output, consistent input, quantum cost and so on [3, 4].

Gate Count (GC): It is the number of reversible gates used to understand the system.

Garbage Output (GO): It is the unutilized output from the reversible gate, it is especially basic to accomplish reversibility and it must be not utilized for facilitating calculation.

Consistent Input (CI): Constant inputs are those inputs that are utilized to create a given logical expression using the reversible logic gates. Steady inputs are kept up at either a consistent 0 or steady 1.

Quantum Cost (QC): Each reversible gate has a cost related with it called quantum cost [5, 6]. The quantum cost of a reversible gate is the number of 2*2 reversible gates or quantum logic gates required in designing it. The quantum cost of all reversible 2*2 gates is taken as unity. The cost of all the 1*1 reversible gates, for example, the NOT gate is thought to be zero [5].

An effective design in reversible logic ought to have the accompanying highlights:

- Use the least number of reversible logic gates
- Should have less number of garbage outputs
- Less number of consistent inputs and
- Minimization of quantum cost.

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The essential reversible logic gates exist in the writing is Feynman Gate [4], Peres Gate [5], Toffoli Gate [6] and Fredkin Gate [7].

A. Feynman Gate:

The most surely understood (2, 2) reversible gate is the Feynman gate[4]. The logical functions performed by a Feynman gate with input vector (A, B) and output vector (P, Q) appear in Fig.1.

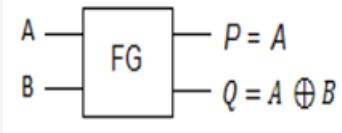

Fig.1:Feynman gate.

B. Toffoli Gate:

Toffoligate [5] is one of the cases for (3, 3) reversible gates. Fig.2 demonstrates the Toffoli gate. This gate is two through gate since two of its outputs are indistinguishable with its inputs. Along these lines, Toffoli gate is otherwise called two controlled NOT (2-CNOT).

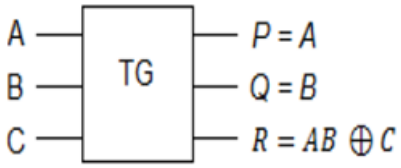

Fig.2: Toffoli gate.

C. URG Gate:

The 3*3 Reversible gate with three inputs and three outputs. URG remains for Universal Reversible Gate. The inputs (A, B, C) mapped to the outputs is as appeared in Fig.3.

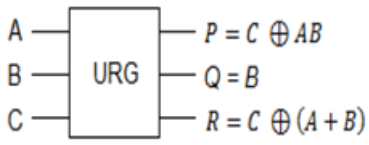

Fig.3: URG gate

D. Machine gear-piece Reversible Logic Gates:

A 3×3 reversible gate COG (Controlled Operation Gate) as of now had been proposed [14] appeared in Fig. 4.

The nearer taking a gander at reality table uncovers that the input design corresponding to a particular output example can be interestingly decided and in this way be kept up that there is a one-to-one correspondence between the input vectors and the output vectors. In this gate the input vector is given by IV = (A, B, C) and the corresponding output vector is OV = (P, Q, R).

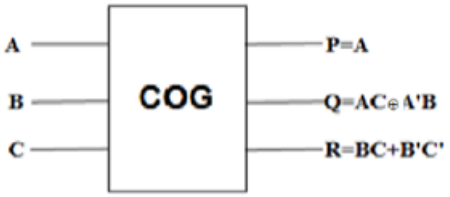

Fig.4: COG reversible gate

E. SBV Gate:

SBV gate is a 5 x 5 reversible gate whose fact table is as appeared in Fig.5. The Fig.6 demonstrates the proposed reversible logic gate which can exclusively work as a nine‟s complementary with one garbage output.

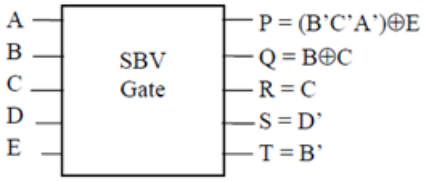

Fig.5: SBV gate.

The proposed SBV gate can be utilized to acquire nine‟s complement of a number with E = 0. On the off chance that input number is B3, B2, B1, B0 whose 9‟s complement is to be acquired then the outputs of SBV gate are as appeared in Fig.6.

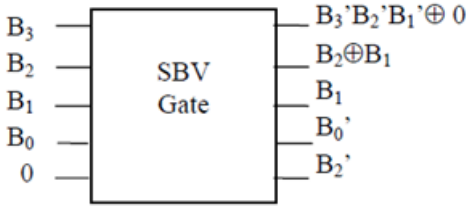

Fig.6: SBV gate implemented as Nine's Complemented gate, where "B2" is a garbage output.

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IV. PROPOSED DESIGN:

In this paper, reversible logic gates are utilized to understand the 64-bit BCD addition and subtraction units. Reversible logic gates are utilized in order to diminish the deferral and power dissipation in the BCD arithmetic unit. BCD adder includes two input data and produces the total as the result. By virtue of any error in the aggregate esteem like the output data so created is not a BCD number at that point there needs a correction hinder for the error output so delivered [7]. Reversible BCD subtraction unit subtracts the two input values and produces the distinction esteem as the output. In the proposed design, subtraction is acknowledged by taking the nine‟s complement and including the complemented an incentive alongside the other input data [8].

A. Reversible 64-bit BCD Addition:

Reversible BCD addition design comprises of two modules, for example, 4-bit addition unit and an error correcting unit. Reversible 64-bit BCD addition unit is acknowledged by falling eight 4-bit BCD adder alongside the error correction unit designed exclusively in the Carry Propagate Adder (CPA) form. Reversible logic gates utilized as a part of this designing are Feynman gate and URG gate for around 4-bit input vectors. Fig.7 demonstrates the design of proposed 4-bit BCD addition unit using reversible logic gates.

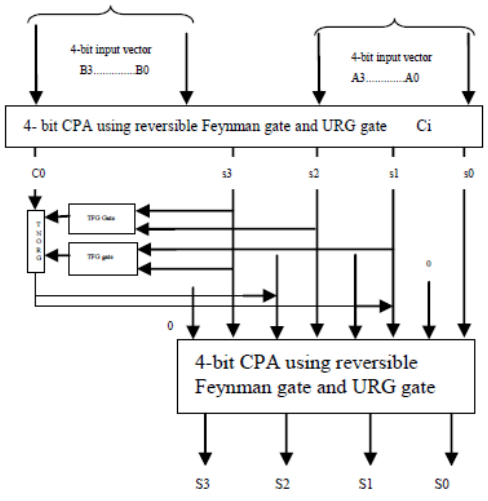

Fig.7: Proposed 4-bit reversible BCD Addition unit

The produced output from 4-bit adder unit is checked for error using error correction unit. Error correction piece is designed by (4x1) MUX using Toffoli gate and TNORG gate. On the off chance that the output of (4x1) MUX is „1‟ then the estimation of binary „0110‟ is added to the output of stage 1 of reversible 4-bit BCD adder; else the output is produced with no correction. By falling 16 reversible 4-bit BCD adder alongside the error correction piece, 64-bit reversible BCD addition can be acknowledged as appeared in Fig.8.

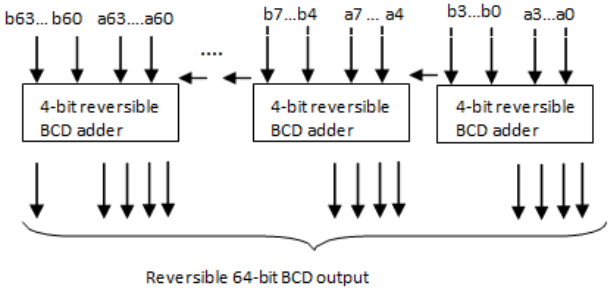

Fig.8: Proposed reversible 64-bit BCD adder

B. Reversible 64-bit BCD Subtractor:

Reversible 64-bit BCD subtraction unit is designed based on the addition of nine's complement of one of the two 4-bit inputs and is included with the other 4-bit input esteem.

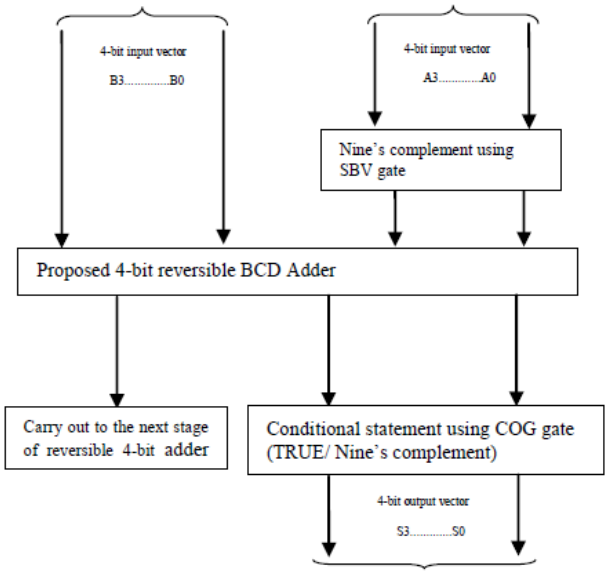

Fig.9: Proposed 4-bit reversible BCD Subtract unit

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Fig.9: the error correction square is designed for singular 4-bit BCD addition pieces. Reversible 4-bit addition unit is designed based on CPA mold using the reversible logic gates, for example, Feynman gate and URG gate; error correcting unit is designed using the reversible logic gates, for example, Toffoli gate and TNORG gate. Nine's complement of one of the 4-bit input vectors is designed using reversible SBV gate. If there should arise an occurrence of the output of 4-bit BCD adder design gives the carry of "1" the output of the specific square is sustained into the nine‟s complement; else if the carry is "0" the output of 4-bit BCD adder is produced at the output vector with no correction made at the error correction unit. If there should be an occurrence of any error correction required for the output of reversible 4-bit BCD subtraction unit the reversible COG gate assumes the part conditional proclamation; if no correction is required then the output of reversible 4-bit subtraction unit is produced with no correction.

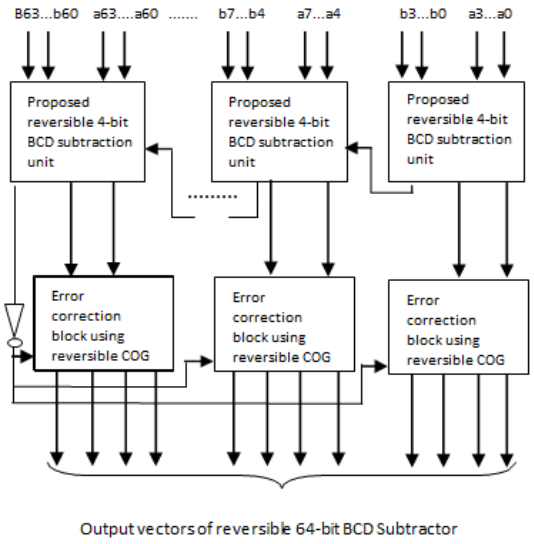

Fig.10: Proposed 64-bit reversible BCD Subtract unit

From Fig.10, it is induced that the 64-bit BCD subtraction is acknowledged by falling of sixteen 4-bit reversible BCD subtraction units alongside the error correction piece controlled for singular reversible 4-bit BCD subtraction.

V. SIMULATION RESULT AND DISCUSSION:

All the amalgamation and reenactment results of the proposed 64 bit BCD adders and subtractor units are performed using Verilog HDL. The combination and recreation are performed on Xilinx ISE 14.7. The corresponding recreation results of the proposed 64 bit BCD adders are demonstrated as follows. Here in this Spartan 3E family, a wide range of gadgets was accessible in the Xilinx ISE apparatus. In order to orchestrate this design the gadget named as "XC3S500E" has been picked and the bundle as "FG320".

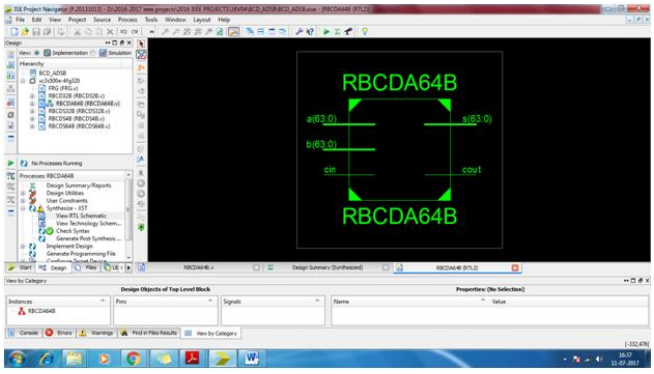

Fig.11: RTL schematic of Top-level of Proposed Reversible 64 bit BCD adder Unit

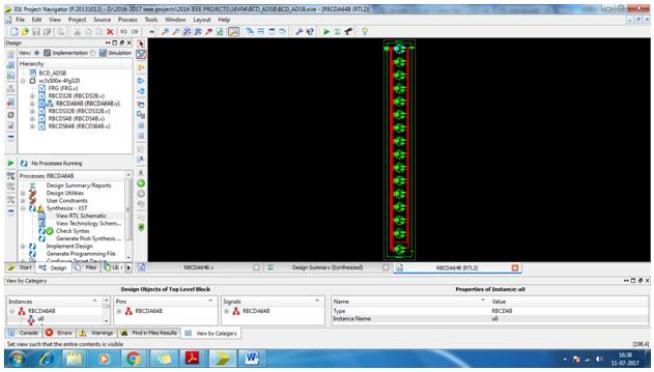

Fig.12: RTL schematic of internal block of Proposed Reversible 64 bit BCD adder Unit

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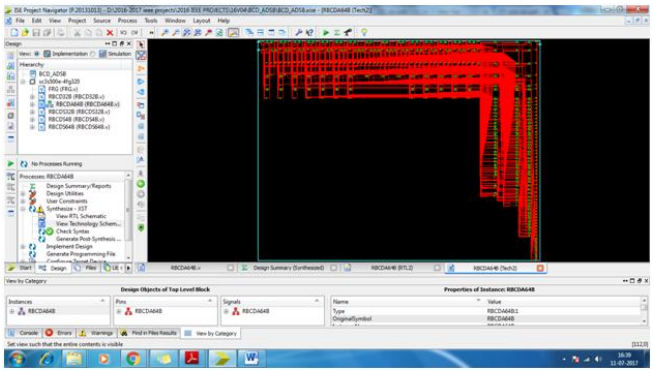

Fig.13: Technology schematic of Proposed Reversible 64 bit BCD adder Unit

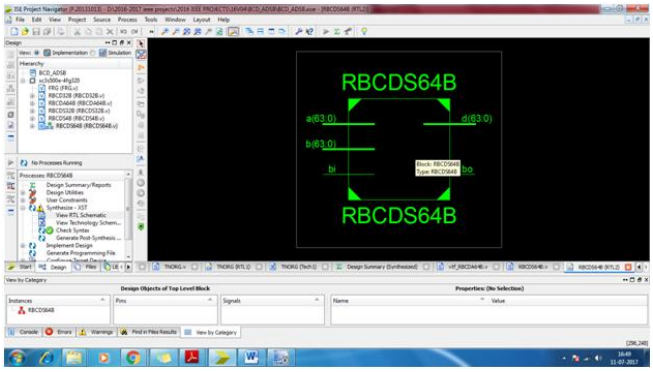

Fig.14: RTL schematic of Top-level of Proposed Reversible 64 bit BCD subtract Unit

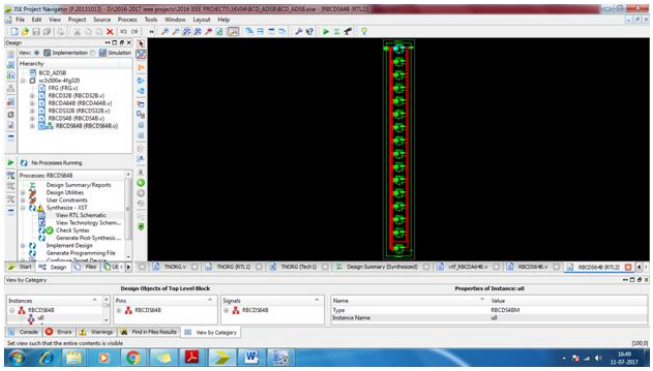

Fig.15: RTL schematic of internal block of Proposed Reversible 64 bit BCD subtract Unit

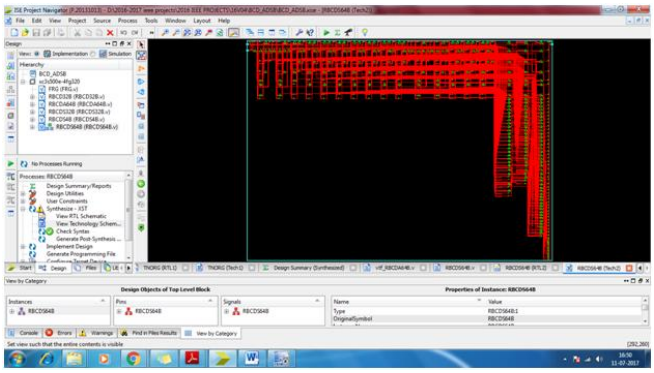

Fig.16: Technology schematic of Proposed Reversible 64 bit BCD subtract Unit

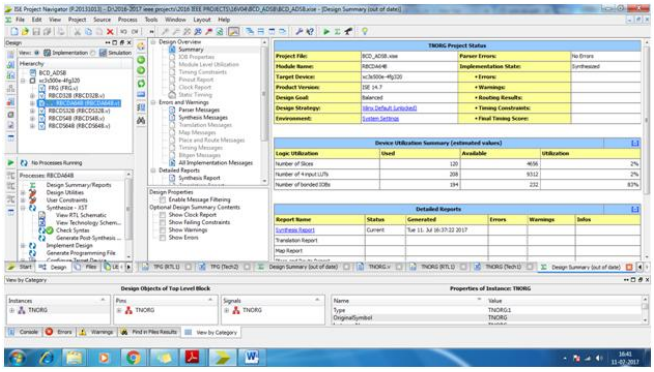

Fig.17: Synthesis report of Proposed Reversible 64 bit BCD adder Unit

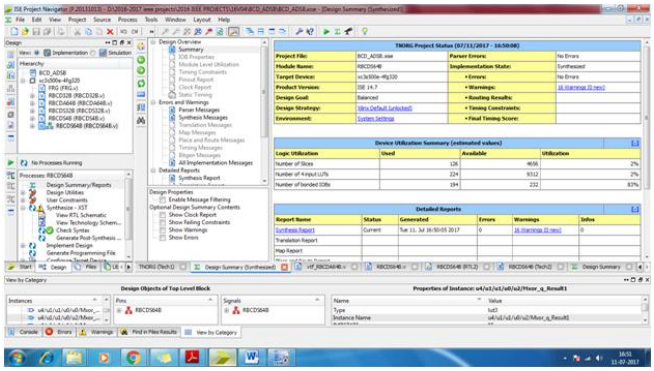

Fig.18: Synthesis report of Proposed Reversible 64 bit BCD subtract Unit

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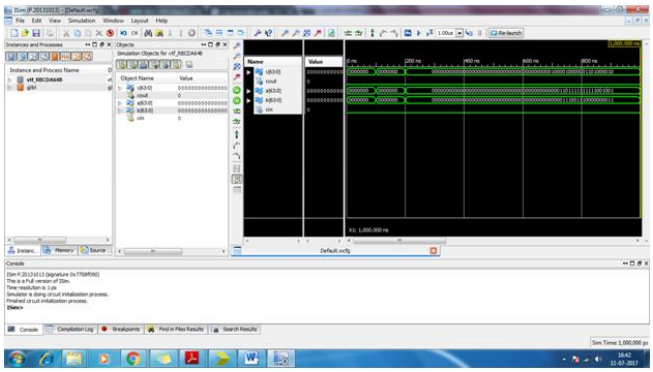

Fig.19: simulated outputs for Proposed Reversible 64 bit BCD adder Unit

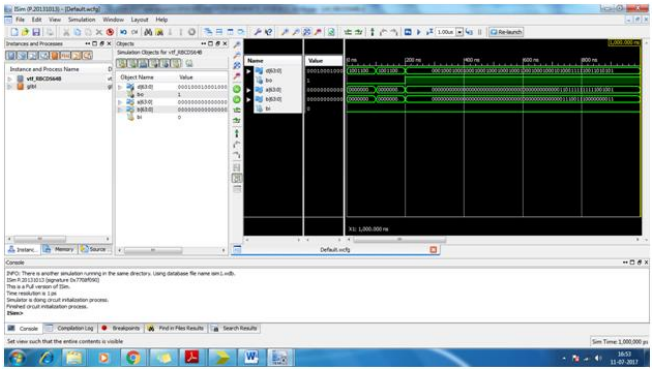

Fig.20: simulated outputs for Proposed Reversible 64 bit BCD subtract Unit

Table I Synthesis Report For Reversible 64 Bit Bcd Add Unit

Reversible 64-bit BCD adderunit	Used	Available	Utilization
No. of slices	120	4656	2%
No. of 4 input LUTs	208	9312	2%
No. of bonded IOB"s	194	232	83%

Table II Synthesis Report For Reversible 64 Bit Bcd Subtract Unit

Reversible 64-bit BCD subtract unit	Used	Available	Utilization
No. of slices	126	4656	2%
No. of 4 input LUTs	224	9312	2%
No. of bonded IOB"s	194	232	83%

VI. CONCLUSION:

In this paper, the design of 64-bit BCD includes subtracting unit have been actualized using reversible logic gates. Modules, for example, 4-bit BCD addition, error correction unit, (4x1) MUX, conditional articulations, 4-bit nine"s complement unit have been designed using the reversible logic gates. BCD arithmetic units are rapid control with the lessened territory. The four piece BCD addition is designed in the CPA mold to additionally upgrade the speed of 64-bit BCD arithmetic design for include subtract units. 64-bit subtraction unit has been designed using 4-bit nine"s complement and 4-bit BCD addition unit. The proposed module has an extensive variety of use in digital signal handling. The assessed parameters for reversible 64-bit BCD addition unit are around 832 garbage values with the basic way deferral of 108 ns; reversible 64-bit BCD subtraction module is around 580 garbage values with the basic way postponement of around 115.6 ns.

REFERENCES:

[1] C.H.Bennett, "Logical Reversibility of Computation," IBM J.Research and Development, pp.525-532, November 1973.

[2] R.Landauer, "Irreversibility and Heat Generation in the Computational Process," IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[3] Dmitri Maslov, "Reversible logic synthesis," University of New Brunswick, September 2003.

[4] X. Susan Christina, M.Sangeetha Justine, K.Rekha, U.Subha, and R.Sumathi, "Realization of BCD adder using reversible logic," International Journal of Computer Theory and Engineering, vol. 2, no. 3, pp 1793-8201, June 2010.

[5] V. Rajmohan, V. Ranganathan, and M. Rajmohan, "A novel reversible design of unified single digit BCD Adder-Subtractor," International journal of

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International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

computer theory and engineering, vol. 3, no. 5, October 2011.

[6] Robert D. Kenney and Michael J. Schulte, "High-Speed Multioperand decimal adders," IEEE transaction on computers, vol. 54, no. 8, August 2015.

[7] Hafiz Md. HasanBabu and Ahsan Raja Chowdhury, "Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit parallel Adder," Proceedings of the 18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design, 2005.

[8] H. Thapliyal, H.R. Arabnia, and M.B. Srinivas, "Efficient Reversible Logic Design of BCD Subtractors," Springer-Verlag Berlin Heidelberg, LNCS 5300, 2009, pp. 99–121.