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Controlling Method of MMC HVDC Based on ARM Current Under Unbalanced Condition

Yarrabotula Koti Reddy
Department of Electrical and Electronics Engineering
Malineni Lakshmaiah Engineering College
Kanumalla (Vill), Singarayakonda -523101,
PrakaSam (Dist.), A.P.

K. Thirumaleswara Rao, M.Tech
Department of Electrical and Electronics Engineering
Malineni Lakshmaiah Engineering College
Kanumalla (Vill), Singarayakonda -523101,
PrakaSam (Dist.), A.P.

ABSTRACT

This project proposes an enhanced control method for a high-voltage direct-current (HVDC) modular multilevel converter (MMC). To control an MMC-HVDC system properly, the ac current, circulating current, and sub module (SM) capacitor voltage are considered. The ac-side current is a fundamental frequency component, and the circulating current is a double-line frequency component. Existing control methods control the ac current and circulating current by separating each component. However, the existing methods have a disadvantage in that the ac-side current must be separated into the positive and negative sequences for control under an unbalanced voltage condition. The circulating current consists of not only negative-sequence components but also positive- and zero-sequence components under an unbalanced voltage condition. Therefore, an additional control method is necessary to consider the positive- and zero-sequence components of the circulating current. The proposed control method has the advantage of controlling not only the ac-side current of the MMC but also the circulating current without separating each of the current components to control each arm current of the MMC. In addition, it can stably control the positive and zero-sequence components of the circulating current under the unbalanced voltage condition.

INTRODUCTION

The voltage-source converter (VSC) high-voltage direct-current (HVDC) system has the advantage of independent control of the active and reactive power, fast transient response characteristics owing to pulse-width modulation(PWM) method, and reduced size of the ac- side filter. It also does not require a transformer to assist in the commutation process. For these reasons, many investigations related to this subject have been carried. Presently the modular multilevel converter (MMC) is widely used to constitute a VSC-HVDC system. The MMC has the advantage of expanding into hundreds of levels because of its simple circuit structure and modularity. Therefore, it is currently under consideration as the most appropriate structure for the configuration of VSC-HVDC systems.

BASIC STRUCTURE OF MMC AND CONTROLLING

Fig. 1.1 shows the structure of a three-phase MMC composed of six arms. Each arm constitutes a converter by connecting a half-bridge module in series. The MMC has the disadvantage of circulating current, which exists because of the presence of different voltages between the dc –link voltage and the entire sub module (SM) capacitor voltage in the arm.

Therefore, a separate control method is required to control the circulating current in the MMC. A control method for voltage balancing among the SM capacitors is also needed because un balanced voltage exists in the SM capacitor voltage. Therefore, to control the MMC, an ac-side power and current controller, a circulating current controller, and a controller for voltage balancing among the SM capacitors are required.

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When the inductance and capacitance increase, the amplitude of the circulating current decreases. However, the increase in the inductance and capacitance cannot completely eliminate the circulating current. This is also inefficient in terms of cost. There-fore, a separate control method to control the circulating cur-rents is needed, a circulating current control method was proposed. The circulating current is a double-line-frequency negative-sequence component under the balanced voltage condition. Accordingly, the circulating current control method was pro-posed to control the circulating current in the synchronous reference frame by performing a coordinate transformation using the double-line-frequency negative sequence. However, the ac-side current and the circulating current controllers were constructed in a cascaded form, and the control method has a disadvantage in that the structure of the controller became complicated. In addition, the double-line-frequency ripple was included in the ac-side active power under the unbalanced voltage condition because the unbalanced voltage condition was not considered. Further, under the unbalanced voltage conditions, the double-line-frequency positive and zero sequence of the circulating current could not be controlled.

The MMC control method using model predictive control (MPC) was proposed. The proposed method constituted a cost function to control the ac-side current, the circulating current, and the SM capacitor voltage balancing by the MPC method. However, the drawback of the proposed control method was that the switching status of $C(2N\,N)$ must be determined in the case where $C\,(N\,N)$ is a combination of N from a set of $2N$, and N is the SM number of each arm; thus, the computational complexity of the processor increased as the level of the MMC increased.

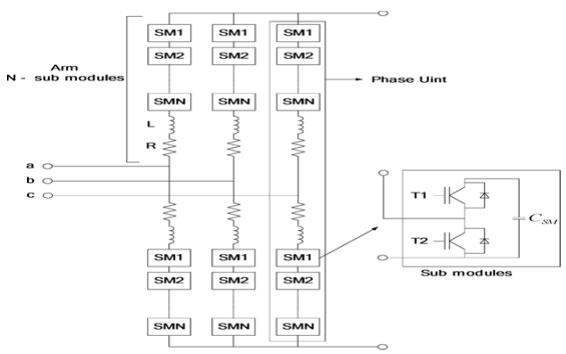

Fig: 1.1 Basic structure of MMC

In the conventional MMC control method, the controller for the ac-side current and another controller for the circulating currents are provided. In addition, the ac -side current controller is configured with a dual vector current control (DVCC) to consider the occurrence of unbalanced voltage. In case the ac-side current controller is configured with DVCC, a notch filter is required to separate the positive and negative-sequence components, and respective proportional -integral (PI) controllers are needed to control the positive and negative d–q axis currents. In addition, negative, positive, and zero-sequence circulating current controllers are correspondingly needed. Thus, controlling the MMC by considering each component makes the control system complex.

An enhanced control method is proposed to control the MMC, without separating the ac-side positive and negative-sequence current and the positive, negative, and zero-sequence components of the circulating current in a three -phase stationary reference frame. The ac-side current reference is calculated according to the active and reactive power references. In current reference is calculated. The calculation of the arm current reference is performed by considering the grid-side ac component and the dc component of the inner unbalanced current. The current that flows in each arm includes the idck component, ac-side current and circulating current. Further, the circulating current should be eliminated. Here, idck is a dc component. The ac-side current is a fundamental frequency component, and the circulating current is a double -line frequency component. Even the frequency characteristics do change under an unbalanced voltage condition. Accordingly, the controller is configured to control each component using a proportional-resonant (PR) controller.

HVDC TRANSMISSION SYSTEM

The decision for the installation of HVDC over HVAC involves capital investments and losses. A DC line with two conductors can carry the same amount of power as an AC line with three conductors of the same

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size and insulation parameters. This results in smaller footprint and simpler design of towers, reduced conductor and insulation costs. Moreover, line investments are reduced by absence of compensation devices, since DC lines do not consume reactive power. Power losses are reduced due to 30% reduction in conduction losses, minimized corona effect and smaller dielectric losses in case of a cable. The breakeven distance, where DC system tends to be more economic than AC for the overhead lines can vary within 400-700 km, while for the cable systems it is around 25-50 km, depending on particular requirements.

The HVDC transmission technology based on high-power electronic devices is widely used nowadays in electrical systems for the transmission of large amounts of power over long distances.

The transformation from AC to DC and vice versa is realized by two converter types:

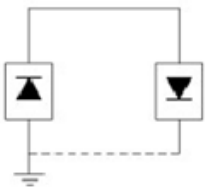
- Current-Source Converters (CSC);
- Voltage-Source Converters (VSC).

CONFIGURATION OF HVDC TRANSMISSON

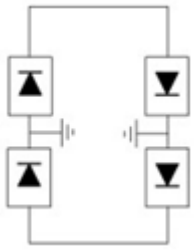
Depending on functional aspects, three main HVDC configurations shown in Figure 2.1 are used.

Mono polar configuration (a) - interconnects two converter stations via a single line, with the possibility to operate at both DC polarities. Ground, sea or metallic conductor can be used for return path.

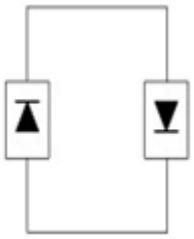
Bipolar configuration (b) - involves two conductors, operating at opposite polarities. This results in two independent DC circuits, rated at half capacity each. During outages of one pole, a mono polar operation can be used. This is the most common configuration for modern HVDC transmission.



(a)



(b)



(c)

Fig 2.1 - HVDC system configurations. (a) Mono polar. (b) Bipolar. (c) Back-to-back

In Back-to-Back configuration (c) - the DC sides of two converters are directly connected, having no DC transmission line. This arrangement is used for the interconnection of asynchronous AC systems.

The typical configuration of modern VSC-HVDC transmission system is shown in Figure 2.3. Two DC conductors of opposite polarity interconnect two converter stations. The polarity of the DC-link voltage remains the same while the DC current is reversed when the direction of the power transfer has to be changed

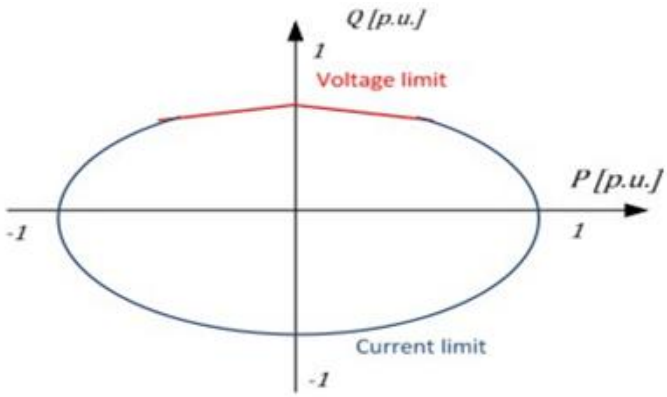


Fig 2.2 - Active-reactive locus diagram of VSC-HVDC transmission

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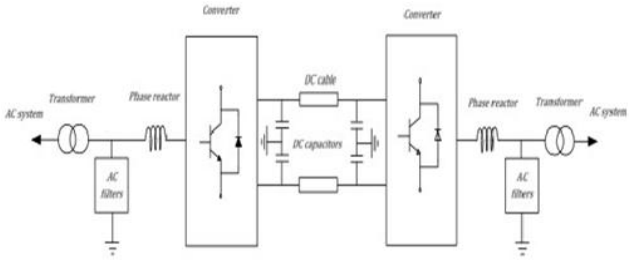

Fig 2.3 - VSC-HVDC system configuration

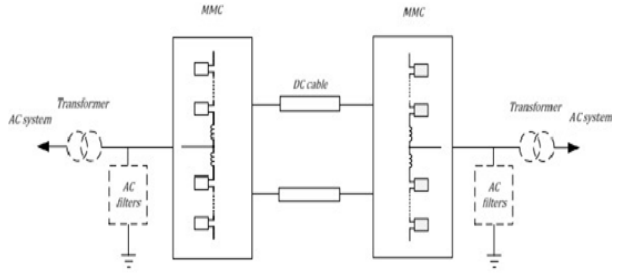

Fig 2.4 - MMC-HVDC system configuration

The DC side capacitors ensure support and filtering of the DC voltage. The converter AC terminals are connected with phase reactors and harmonic filters. The phase reactors ensure control of power exchange between the converter and AC system, the limitation of fault currents and blocking of current harmonics appearing due to PWM. The AC filters reduce harmonics content on the AC bus voltage. Power transformers are used to interface the AC system, adapting converter and AC system voltages as well as participate in power regulation by means of tap changers.

MODULATION TECHNIQUES OF MMC

Multilevel modulation methods can be split into two main categories:

Space Vector Modulation (SVM) and Voltage level Based Modulation; i.e. Carrier PWM (CPWM) and Nearest Level Modulation.

Space vector modulation

The Space Vector Modulation theory is well established nowadays. Due to its advantages, such as easy digital implementation and the possibility of optimizing the switching sequences, it is an attractive modulation technique for multilevel converters. The principle applied for the calculation of the voltage vectors in two or three level converters can be extended to multilevel converters. However, the complexity of the algorithms for the calculation of the state vectors and computational costs increase with the number of levels. Recent publications have presented strategies where simpler algorithms are used; accordingly the computational efforts are significantly reduced, comparing with conventional SVM techniques.

Multi carrier modulation

The Carrier-based Pulse-Width Modulation concept is based on comparison of a reference (modulating) signal with a high-frequency triangular waveform (the carrier). The carrier can have a periodic bipolar or unipolar waveform. The switching instants are determined by the intersections of the modulating and carrier signals. When the reference is sampled through the number of carrier waveforms, the PWM technique is considered as a multicarrier PWM. The multicarrier PWM implementation in multi-cell converter topologies is especially advantageous because each carrier can be assigned to a particular cell which allows independent cell modulation and control.

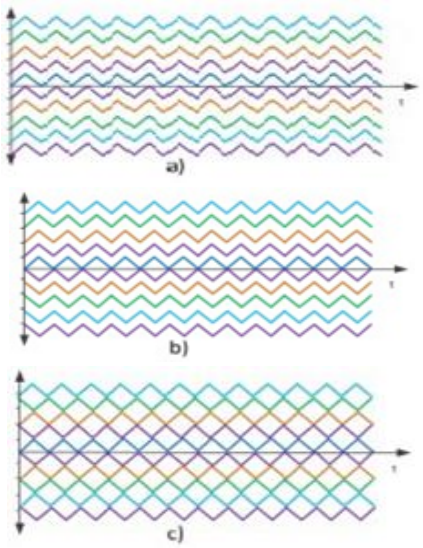

Fig3.4 - Level shifted PMW carriers. (a) Phase Disposition (PD) (b) phase opposition disposition (POD) (c) alternate phase opposition disposition (APOD)

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The carriers can be displaced within levels (Level-shifted PWM), have phase shifts (phase-shifted PWM) or have a combination of them. The level-shifted PWM (LS-PWM) has N-1 carrier signals with the same amplitude and frequency, relating each carrier with the possible output voltage level generated. Depending on the way the carriers are located, they can be in phase disposition (PD-PWM), phase opposition disposition (POD-PWM), or alternate phase opposition disposition (APOD-PWM) as shown in Figure3.4.

The LS-PWM methods produce an unequal duty and power distribution among the sub-modules since the vertical shifts relate each carrier and output level to a particular cell. These can be corrected by implementing carrier rotation and signal distribution techniques. The Carrier phase shifted method (PS-PWM) has N-1 carrier signals with the same amplitude and frequency. To achieve a staircase multilevel output waveform, the phase shift between the carriers is calculated as φ = 3605/'N − 1. The multicarrier PS-PWM process is shown in Figure 3.5.

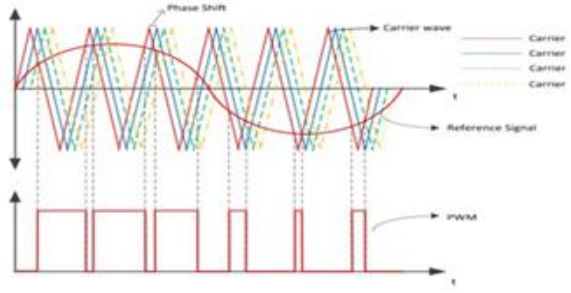

Fig 3.5 - Phase Shifted PWM

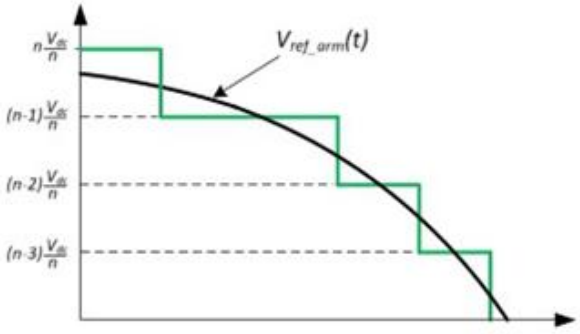

Fig 3.6 -Nearest Level Modulation, arm voltage waveform

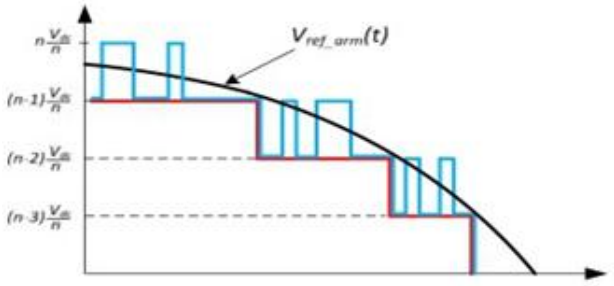

Fig 3.7 - Nearest Level Modulation, arm voltage waveform with SM modulation.

This approach provides equal duty and power distribution between the cells and, by selecting an adequate carrier frequency, capacitor voltage balancing can be achieved. A comprehensive analysis of the Multicarrier PWM techniques was performed in where the mentioned methods were extended and analysed particularly for MMC applications.

MMC – HVDC MODEL DELOPMENT

In this chapter a model of MMC-HVDC transmission system is developed and tested. First, the inner control techniques for the MMC are discussed and proven through simulations. Then, the outer control loops for the VSC-HVDC transmission systems are presented.

In this project, the MMC Inner Control shall be referred to the control of the sub-module capacitor voltages and the circulating current. The outer controls denote the control loops implemented for the regulation of the output parameters of the converter; e.g. current control, DC voltage control and PQ control.

Energy Control

In this method the arm capacitor voltages are kept to a reference through the control of the total stored energy m[in the phase leg and the difference between the energy stored in the upper and lower arms. An open loop approach using the estimation of the stored energy is proposed with the intention of increasing the stability of the system and avoiding the need of a continuous measurement of the capacitors voltage to calculate the converter stored energy.

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Distributed control

In this the cell capacitor voltages are controlled independently. The control is implemented in two parts.

- Averaging part, implemented per phase-leg
- Balancing part, implemented in each sub-module

In Figure 4.1 the block diagram of the distributed control method is presented. As it can be observed, the averaging control is implemented in two loops, outer voltage loop and inner current loop. The voltage loop is responsible of controlling the mean value of the capacitor voltages in the leg by influencing each cell individually. The error signal is processed in the controller, resulting in the reference signal for the difference current loop. Under the balanced conditions, the DC component of the difference current is equal to 1/3 of the DC-link current, therefore a feed-forward term is added to increase the response of the controller as highlighted in Figure 4.1.

If the average voltage is lower than the desired value, a positive current reference is obtained. The current reference is subtracted from the measured value, reducing the control command. By this means, the DC component of the difference current is increased, rising the charge in the capacitors.

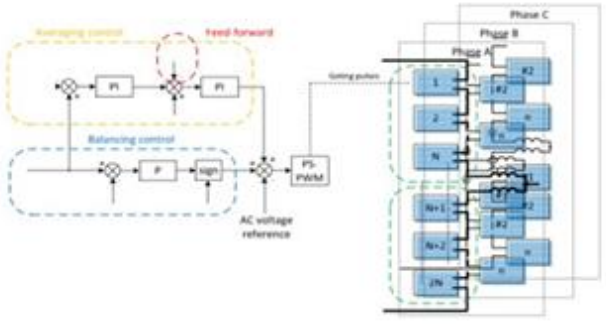

Fig 4.1 - Distributed Control, block diagram

The average charge of the capacitors depends on the DC component of the difference current. If only an integral compensator is used, the DC value of the difference current is controlled, making in no effect on the circulating current. The compensator in the current loop acts on the AC component of the difference current. The Balancing control is implemented in each sub-module individually. The control signal is generated based on the capacitor voltage and the direction of the corresponding arm current. The final sub-module voltage reference is obtained by adding both averaging and balancing control signals to the voltage reference.

HVDC CONTROLS

In HVDC transmission system the outer control regulates the power transfer between the AC and DC systems. The active and reactive power is regulated by the phase and the amplitude of the converter line currents with respect to the PCC voltage. The control structure for conventional VSC-HVDC systems consists of a fast inner current control loop and outer control loops, depending on the application requirements HVDC controls are shown in figure 4.2.

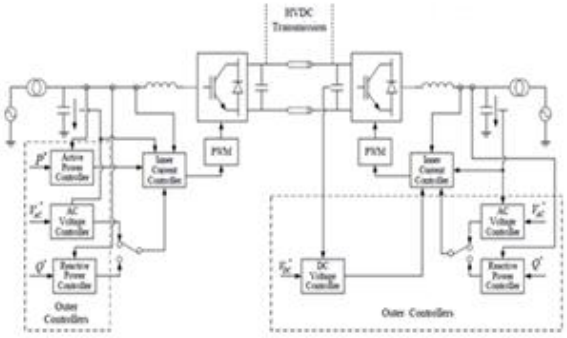

Fig 4.2 Overall control structure of the VSC-HVDC transmission system

The current loop is responsible for fast tracking of references generated in the power controller, DC or AC voltage controllers. When operating in inverter mode, the converter controls the DC-link voltage at predefined value. To achieve this, the DC voltage controller adjusts the active current reference in such a way, that the net imbalance of power exchange between the DC and AC systems is kept to zero .In rectifier mode the converter tracks active power references directly. The reactive power at both sides

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can be controlled independently. It can be regulated to track a reference, thus regulating power factor at the PCC or to control of the AC grid voltage at the PCC. A phase locked loop (PLL) is used for the synchronisation with the grid voltage. The PLL mechanism is able to detect phase angle and the magnitude of the grid voltage, to be later used in the controls. The grid frequency can also be obtained from PLL.

Phase Locked Loop

The grid synchronization is a very important and necessary feature of grid side converter control. The synchronization algorithm is able to detect the phase angle of grid voltage in order to synchronize the delivered power. Moreover, the phase angle plays an important role in control, being used in different transformation modules, as Park's transformation.

There are several methods capable to detect the phase angle: the zero crossing detection, the filtering of grid voltages and the phase locked loop (PLL) technique.PLL is a phase tracking algorithm, which is able to provide an output synchronized with its reference input in both frequency and phase. The purposed of this method is to synchronize the inverter output current with the grid voltage, in order to obtain a unitary power factor.

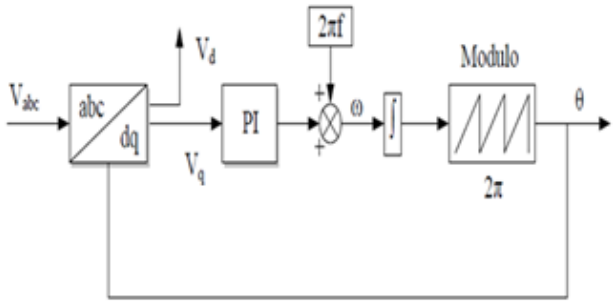

Fig 4.3 Block diagram of PLL

The block diagram of the PLL algorithm implemented in the synchronous reference frame is presented in Figure 4.3. The inputs of the PLL model are the three phase voltages measured on the grid side as well as source side and the output is the tracked phase angle. The PLL model is implemented in d-q synchronous reference frame, which means that a Park transformation is needed. The phase locking of this system is realized by controlling the q-axis voltage to zero. Normally, a PI controller is used for this purpose. By integrating the sum between the PI output and the reference frequency the phase angle is obtained.

Current Control Loop

The inner current controller is implemented in the d-q synchronous reference frame. Usually, the d-q control structures are associated with PI controllers due to their good behavior when regulating DC variables. However the PI current controllers have no satisfactory tracking performances. Therefore, in order to improve the performances of the PI current controllers in such systems, cross-coupling terms and voltage feed forward is usually used

The structure of the inner current controller implemented in the synchronous reference frame is presented in Figure 4.4.

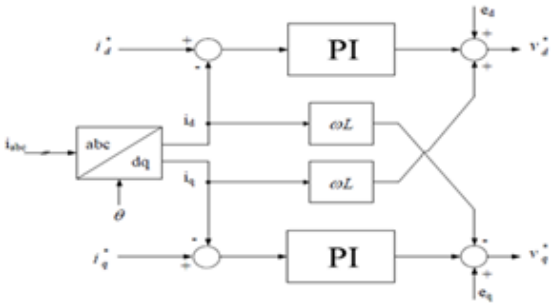

Fig 4.4 The Inner current controller implemented in synchronous reference frame

CONVERTER CURRENT LIMITATION

The described control strategies have shown an increase in the AC currents due to change in grid conditions. Depending on the particular conditions of the grid unbalance, these currents may exceed the limits of the converter devices, thus tripping the over current protection. A current-limiting mechanism should be implemented in order to ensure stable and continuous converter operation during faults.

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- Calculation of AC current limits
- Validation of current limitation strategy
- Maximum active power injection
- Maximum reactive power injection

The arm currents fall into the imposed limits within 3 fundamental cycles, because of the ramped change of power references. However, after stabilization, the limits for the arm and AC currents are not exceeded. With the injection of reactive power, the grid voltage is raised. Thus the converter provides grid voltage support with maximum allowed reactive current injection.

BASIC STRUCTURE OF THE MODULAR MULTILEVEL CONVERTER

Fig.1 shows the single-phase equivalent circuit of a three-phase MMC. Here is the ac-side voltage is the ac-side current and represent the current in the upper and lower arms, respectively represents the inner unbalanced current is the converter output voltage of the phase and represent the voltage of the upper and lower arms, respectively. Subscripts and represent the upper and lower arms, respectively and subscript represents and as shown in Fig. 1. The ac-side voltage equation of the MMC is given as follows.

$$V_k = e_k - \frac{L}{2}\frac{di_k}{dt} - \frac{R}{2}i_k \quad \text{..... (1)}$$

$$L\frac{di_{diffk}}{dt} + Ri_{diffk} = \frac{V_{dc}}{2} - \frac{e_{pk}+e_{nk}}{2} \quad \text{..... (2)}$$

$$e_k = \frac{e_{nk}-e_{pk}}{2} \quad \text{..... (3)}$$

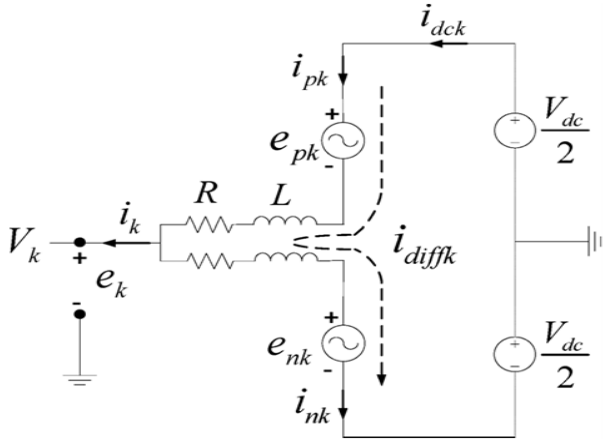

Figure 5.1 single- phase equivalent circuit of the three - phase MMC

The voltage equations of the upper and lower arms shown in Fig. 2 are expressed

$$e_{pk} = \left(\frac{V_{dc}}{2} - V_k\right) - Ri_{pk} - L\frac{di_{pk}}{dt} \quad \text{..... (4)}$$

$$e_{nk} = \left(\frac{V_{dc}}{2} + V_k\right) - Ri_{nk} - L\frac{di_{nk}}{dt} \quad \text{..... (5)}$$

Here, the currents in the upper and lower arms are expressed by (6) and (7), and the inner unbalanced current is expressed by (8) represents the circulating current

$$i_{pk} = i_{diffk} + \frac{i_k}{2} \quad \text{..... (6)}$$

$$i_{nk} = i_{diffk} - \frac{i_k}{2} \quad \text{..... (7)}$$

$$i_{diffk} = \frac{i_{pk}+i_{nk}}{2} = i_{dck} + i_{zk} \quad \text{..... (8)}$$

ARM CURRENT REFERENCE

Under the balanced voltage condition, the ac-side active power and reactive power relative to the ac-side current are expressed by (9) and (10), respectively, because the negative-sequence component does not exist. Subscripts and represent the d-q axes of the synchronous reference frame and superscripts and represent the positive and negative sequences, respectively

$$P_{AC} = \frac{3}{2}\left(V_d^p i_d^p + V_q^p i_q^p\right) \quad \text{..... (9)}$$

$$Q_{AC} = \frac{2}{3}\left(V_q^p i_d^p - V_d^p i_q^p\right) \quad \text{..... (10)}$$

If theta is determined such that using a phase-locked loop (PLL) [22], the ac-side current references relative to the active and reactive power references are expressed by (11) and(12) under the balanced voltage condition.

$$i_q^{p*} = \frac{2}{3}\frac{P_g^*}{V_q^p} \quad \text{..... (11)}$$

$$i_d^{p*} = \frac{2}{3}\frac{Q_g^*}{V_q^p} \quad \text{..... (12)}$$

However, the ac-side active power has a double-line-frequency ripple under the unbalanced voltage condition. Equation (13) shows the ac-side active power under unbalanced voltage conditions. Here, is the dc component of the active power, and are the

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double-line-frequency ripple components of the active power as expressed in (14)-(16).

$$P_{AC} = P_{AC_0} + P_{AC_{\sin 2}} \sin 2\omega t + P_{AC_{\cos 2}} \cos 2\omega t \quad \text{..... (13)}$$

$$P_{AC0} = \frac{3}{2}\left(V_d^p i_d^p + V_q^p i_q^p + V_d^n i_d^n + V_q^n i_q^n\right) \quad \text{..... (14)}$$

$$P_{AC\sin 2} = \frac{3}{2}\left(V_d^p i_d^p - V_q^p i_q^p - V_d^n i_d^n + V_q^n i_q^n\right) \quad \text{..... (15)}$$

$$P_{AC\cos 2} = \frac{3}{2}\left(V_d^p i_d^p + V_q^p i_q^p + V_d^n i_d^n + V_q^n i_q^n\right) \quad \text{..... (16)}$$

Accordingly, to eliminate the ripples of the ac-side active power, it is necessary to reduce the ripples by controlling and to zero. To control the and to zero, according to (15), (16) and taking into account

$P_{ACsin2}=0$, $P_{AC\cos 2}=0$ and $V_d{}^p=0$, the negative current reference can be obtained as

$$i_d^{n*} = \frac{V_q^n}{V_q^p} i_q^p - \frac{V_q^n}{V_q^p} i_q^p \quad \text{..... (17)}$$

$$i_q^{n*} = -\frac{V_q^n}{V_q^p} i_d^p - \frac{V_q^n}{V_q^p} i_q^p \quad \text{..... (18)}$$

The ac-side current reference of each phase can be obtained through a coordinate transformation of (11), (12), (17), and (18). The transformations are given as

$$i_{\alpha\beta}^* = i_{dq}^{p\,*} e^{j\omega t} + i_d^{n\,*} e^{-j\omega t} \quad \text{..... (19)}$$

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \quad \text{..... (20)}$$

In(6)-(8),(8)is inserted into(6)and(7),and the upper arm and lower arm current can be represented as (21) and (22),where needs to be eliminated as the circulating current

$$i_{pk} = i_{dck} + \frac{i_k}{2} + i_{zk} \quad \text{..... (21)}$$

$$i_{nk} = i_{dck} - \frac{i_k}{2} + i_{zk} \quad \text{..... (22)}$$

Accordingly, the current references of the upper and lower arms can be obtained

$$i_{pk}^* = i_{dck}^* + \frac{i_k^*}{2} \quad \text{..... (23)}$$

$$i_{nk}^* = i_{dck}^* + \frac{i_k^*}{2} \quad \text{..... (24)}$$

If three-phase active power is the same, the dc component of the inner unbalance current is of the same magnitude. However, if three-phase active power has a different magnitude, the dc component of the inner un balance current of each phase has a different magnitude depending on the phase active power.

$$P_{ACk} = P_{dck} = V_{dc} i_{dck} \quad \text{..... (25)}$$

$$P_{ACk} = \frac{1}{2} V_{mk} i_{mk} \cos\theta \quad \text{..... (26)}$$

$$P_{ACk} = V_k i_k$$

$$= V_{mk} \sin\omega t * I_{mk} \sin(\omega t - \theta)$$

$$= \frac{1}{2} V_{mk} i_{mk} (\cos\theta - \cos(2\omega t - \theta)) \quad \text{..... (27)}$$

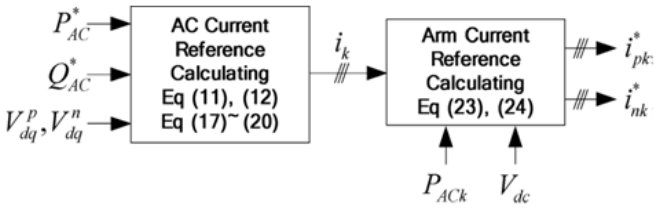

Fig: 5.2 control scheme of the proposed arm current reference calculation

The arm resistor is a small value as an internal resistance of the inductor. Accordingly, if it is assumed that there is no loss in the MMC, the ac- and dc-side phase active powers of the MMC should be equivalent. Thus, the ac- and dc-side active powers relative to are expressed by (25), where the ac-side phase active power is defined by (26). Here, is the peak value of phase voltage, is the peak value of phase current, and is the phase-angle difference. Therefore, in order to measure the phase active power, and should be known. In the control system, phase voltage and current are measured. How-ever, in order to measure the extra control method is required Phase active power is determined by using the instantaneous power. The ac-side phase instantaneous power is defined by where and are measured by the sensor. The instantaneous power and active power are the same value, except for double-line frequency harmonic components. So the double-line frequency component of the instantaneous power removed by the double-line frequency notch filter and this is used as the phase active power. The dc component is defined by (28) because the ac-side active power and the dc-link voltage are known. Fig. 1 shows the proposed control block diagram to calculate the current references of the upper and lower arms.

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$$i^*_{dck} = \frac{P_{ACk}}{V_{dc}} \quad \text{..... (28)}$$

ARM CURRENT CONTROL

As shown in (23) and (24), the reference of the arm current is composed of the dc and the ac components with the fundamental frequency component. However, the current that flows in the arm includes the dc and fundamental frequency components, as well as the double-line-frequency circulating current component, as shown in equation (21) and (22).

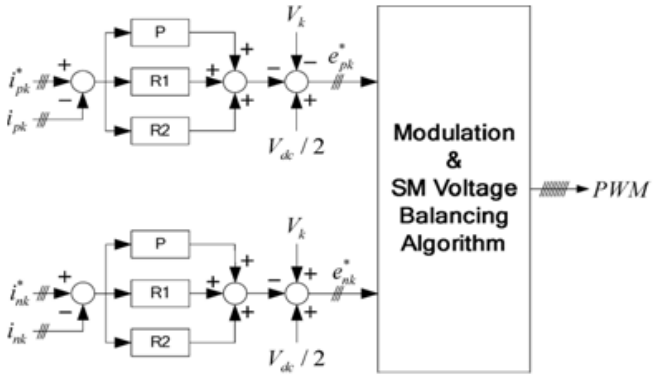

Fig 5.3 proposed arm current control

Under the balanced Voltage condition, the circulating current is a double-line-frequency negative-sequence component. However, under the un-balanced voltage condition, not only are the double-line-frequency negative-sequence components included in the circulating current, but also the double.

PROPOSED MODEL AND SIMULATION ANALYSIS

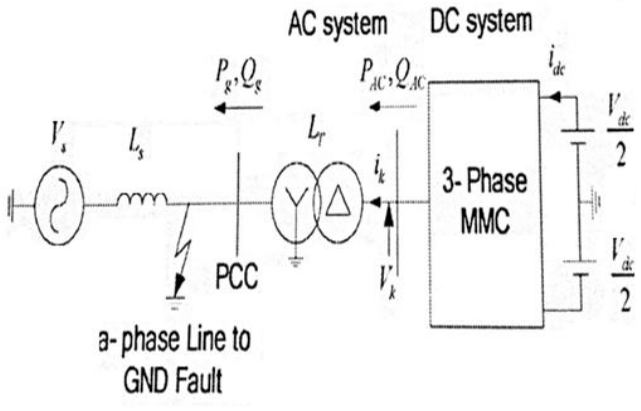

Fig5.4 system structure of simulations

Figure.5.4 shows the proposed arm current control block diagram. The current controller for the ac current and the circulating current is constructed by two PR controllers in this way, the structure of the current controller is simplified. Simulation was carried out using the PSCAD/EMTDC, as shown in Fig.5.5, and the parameters used in the simulation are listed in Table I. The voltage-balancing algorithm and the PWM method used the modified PSC-PWM method of [8] for the SM capacitor.

Fig.5.5 shows the simulation results of the proposed control method based on the load changes. The zero-power control is maintained until 0.5 s, where a load of 4 MW is applied to the ramp at t=0.05sec In addition, a load of -4MWis applied at 0.7 s to analyze the characteristics of the proposed control method depending on the load change.

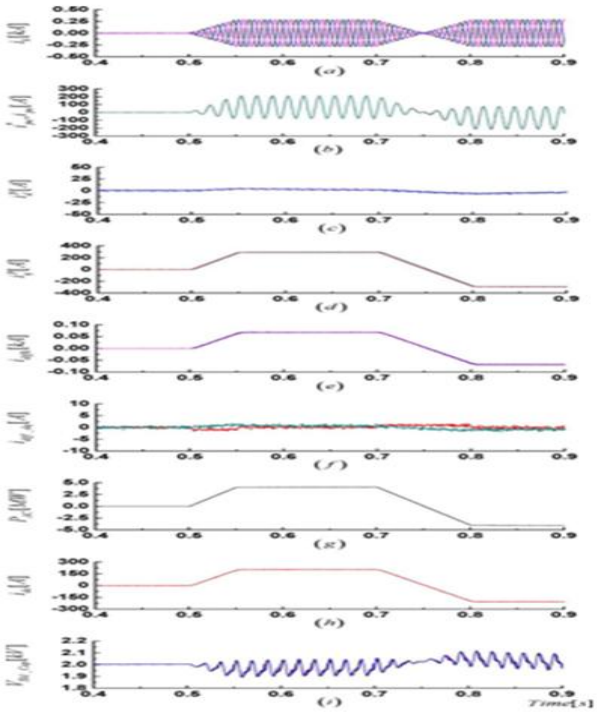

Figure.5.5 Simulation results of an active power reversal demand: (a) AC-side current. (b) a-phase upper arm current. (c)AC side d-q axis current. (d) AC- side d-q current. (e) Inner unbalance current idiffk. (f) d- q axis circulating cur-rent. (g) AC-side active power. (h) DC-link current. (i) SM capacitor voltage.

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Fig.5.5 (a) shows the ac-side current of the MMC, and Fig.5.5 (b) shows the a-phase upper arm current and the current reference. The arm current is controlled in accordance with the arm current reference without the error. Fig.5.5 (c) and (d) shows the ac-side positive – axis currents. The controls are stably achieved without overshoot and under-shoot relative to the current reference. Fig.5.5 (e) and (f) shows the inner unbalance current idiffk and the d-q axis circulating current. As the load increases and decreases, the inner unbalance current is maintained as the same magnitude and is stably controlled without ripple. The d-q axis circulating current is also controlled to zero, regardless of the increase or decrease in the load. Fig.5.5 (g) shows the ac-side active power, and Fig.5.5 (h) shows the dc-link current. Although the load reference is changed to 4 MW in 0.05 s, the ac-side active power and dc-link current are stably controlled without transient characteristics. Fig.5.5 (i) shows the SM capacitor voltage of the a-phase upper arm. Each SM voltage is controlled to the same magnitude regardless of the changes in the load.

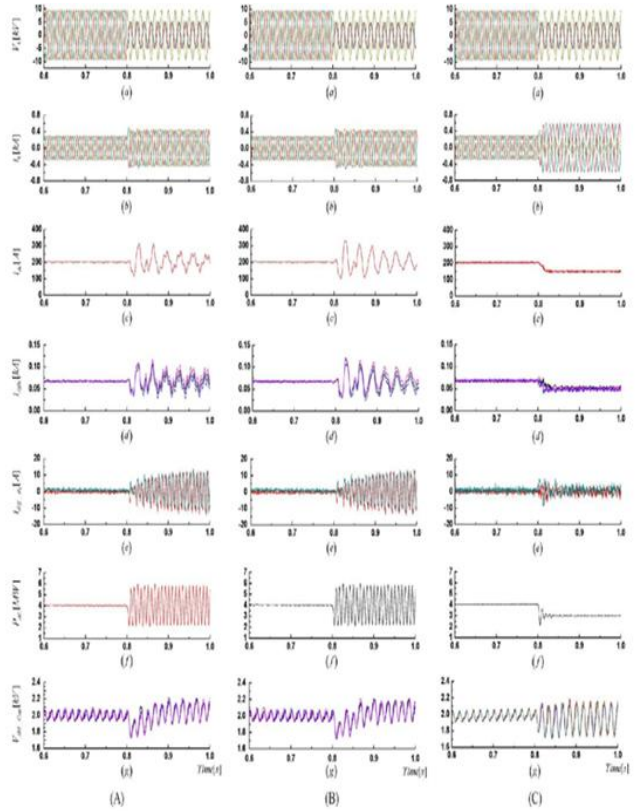

Fig 5.6. Simulation results under the unbalanced voltage condition. (a) MMC-side ac voltage. (b) MMC-side ac current. (c) DC-link current. (d) Inner unbalances current idiffk. (e) - axis circulating current. (f) AC-side active power. (g) SM capacitor voltage. (A) Conventional control method1. (B) Conventional control method2. (C) Proposed control method.

Fig.5.6 shows the simulation results under the unbalanced voltage condition. To apply the unbalanced voltage conditions, the a-phase line-to-ground fault is applied at 0.8 s. Fig.5.6 (A) and (B) show the conventional control method, and Fig.5.6(C) shows the proposed control method. Conventional control method 1 only considered the double-line-frequency negative-sequence circulating currents.

The positive and negative-sequence circulating current and unbalanced voltage condition are not considered. Conventional control method2 proposed a circulating current control method considering the double-line-frequency negative- and zero-sequence components. The ac-side negative-sequence current is controlled to zero under unbalanced voltage conditions.

Fig.5.6 (a) and (b) shows the MMC-side ac voltage and ac cur-rent, respectively. At0.8s, the ac-side current increases because of the line to ground. In Fig.5.6 (A)-(b) the current is controlled in the three-phase equilibrium under the unbalanced voltage condition. The conventional control method 1 controls the ac-side current without separating positive- and negative-sequence current in the synchronous reference frame.

However, in Fig.5.6 (C)-(g), the proposed control method controls the inner unbalanced current without transient characteristics, and the capacitor voltage of the SM is controlled without transient characteristics. However, the ripples in the SM are larger than those in the conventional control methods because of the injection of ac-side negative current.

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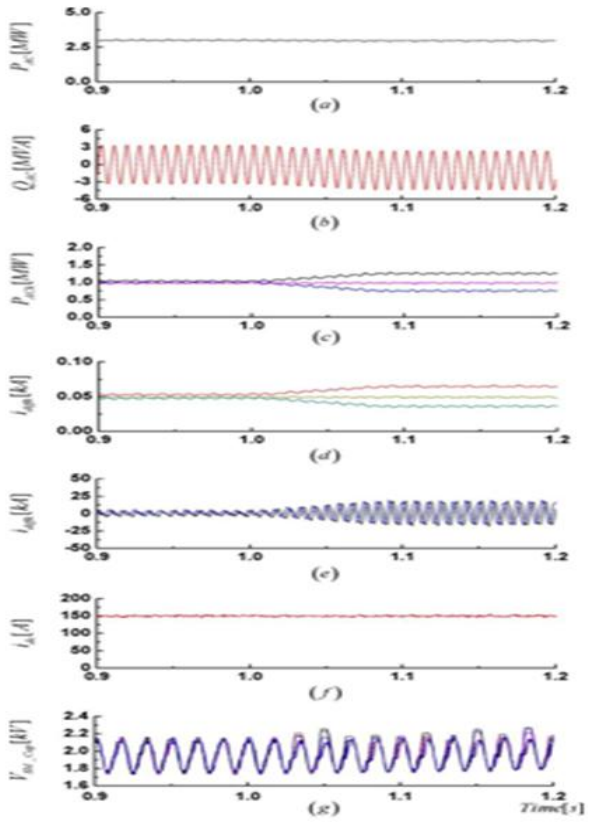

Figure 5.7.Simulation results of active power reversal demand. (a) AC side active power. (b)AC side reactive power.(c)AC side phase active power.(d)inner un balance current idiffk.(e)d-q axis circulating current.(f)DC link current.(g)SM capacitor voltage

Fig.5.7 shows the simulation results of Fig.5.6(C) simulation conditions based on the reactive power supplies. The reactive power of 0.8 MVA is applied to the ramp at 1 s. Fig. 5.7(a) shows the ac-side active power. The total active power is maintained constant magnitude regardless of the injection of reactive power.

SIMULATION RESULTS OF THE PROPOSED MODEL

The following figures shows simulation results of active power reversal demand unbalanced proposed conditions by proposed control method conditions based on the reactive power supplies. The reactive power of -0.8 MVA is applied to the ramp at t=1s.

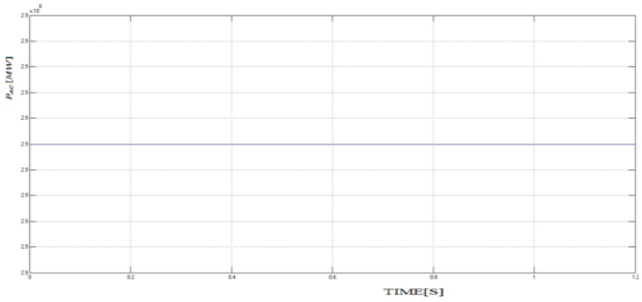

Figure 6.13(a) simulation results of active power reversal condition AC side active power by proposed method

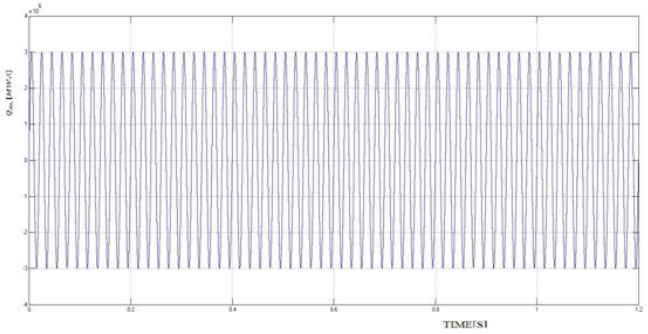

Figure 6.13(b) simulation results of active power reversal condition AC side reactive power by proposed method

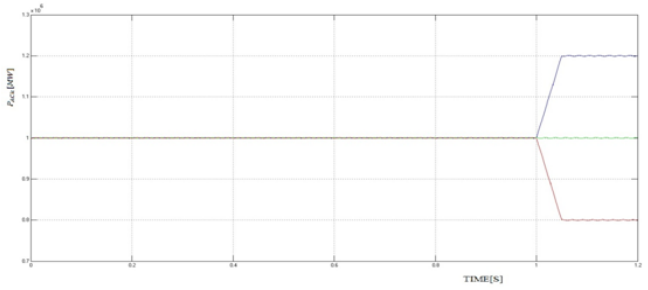

Figure 6.13(c) simulation results of active power reversal condition AC side phase active power by proposed method

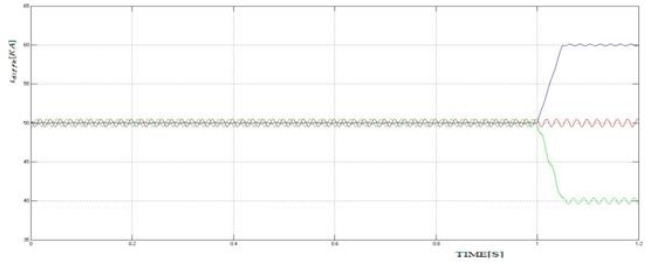

Figure 6.13(d) simulation results of active power reversal condition inner un balanced current by proposed method

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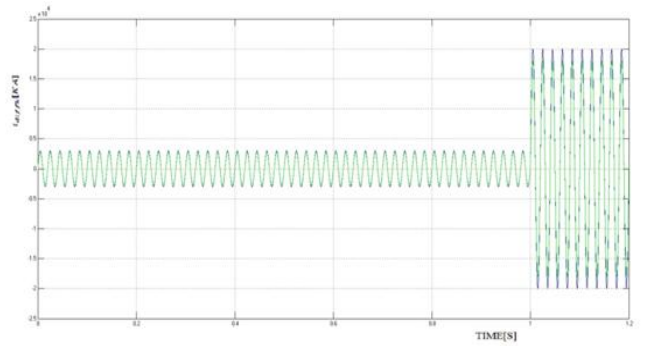

Figure 6.13(e) simulation results of active power reversal condition d-q circulating current by proposed method

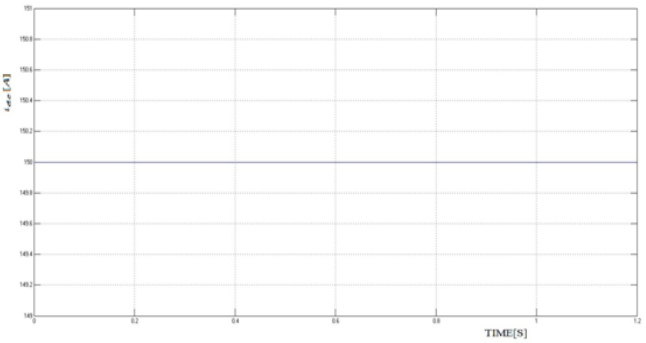

Figure 6.13(f) simulation results of active power reversal condition DC link current by proposed method

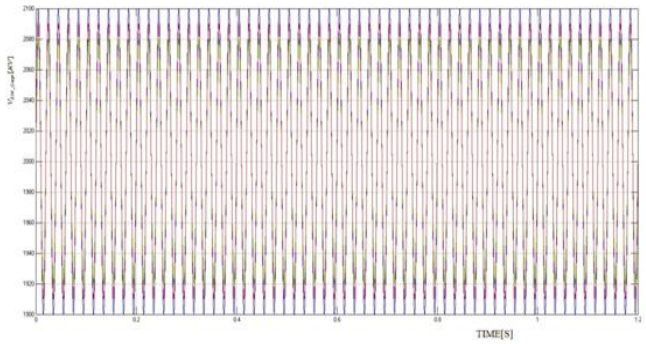

Figure 6.13(g) simulation results of active power reversal condition SM capacitor voltage by proposed method

Fig. 6.13 shows the simulation results of Fig. 6.12 simulation conditions based on the reactive power supplies. The reactive power of 0.8 MVA is applied to the ramp at 1 s. Fig. 6.13(a) shows the ac-side active power. The total active power is maintained constant magnitude regardless of the injection of reactive power.

Fig. 6.13(b) shows the ac-side reactive power. In Fig. 6.13(b), 3-MVA double-line-frequency ripple exists in the reactive power because the proposed control method injects negative current to reduce the active power ripples.

Fig. 6.13(c) and (d) shows the ac-side phase active power and the inner unbalanced current idiffk. The phase active power is controlled to the different magnitude because of the injection of reactive power. Accordingly, the inner unbalanced current of each phase is controlled in proportion to the phase active power. And the double-line-frequency component corresponding to the circulating current is stably controlled without ripple.

Fig. 6.13(e) shows the d-q axis circulating current. In Fig. 6.13(d), circulating current does not exist in inner unbalanced current idiffk However; the dc component of inner unbalanced current is controlled to a different magnitude. Accordingly, – axis circulating current obtained through a coordinate transformation of inner unbalanced current shows the double-line-frequency ripple. This ripple is a coordinate transformation of the error, not circulating current ripple.

Fig. 6.13(f) shows the dc-link current. Phase active power is controlled to a different magnitude, but total active power is maintained to the same magnitude regardless of the injection of re-active power. So, dc-link current is controlled as the same magnitude without variation.

Fig. 6.13(g) shows the a-phase SM capacitor voltage. Each SM voltage is controlled to the same magnitude, regardless of the injection of reactive power.

CONCLUSION

An enhanced control method has been proposed to control the MMC based on the arm current in a three-phase stationery reference frame. In the conventional control method, the ac-side current controller of the MMC and the circulating current controller are

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configured In a cascade form. The conventional method suffers the drawback of increasing the complexity of the control system because control must be performed by separating the ac current controllers into positive and negative sequences to consider the occurrence of unbalanced voltage. However, the proposed control method can control the MMC without separating the ac-side positive and negative-sequence current and the double-line-frequency positive-, negative-, and zero-sequence components of the circulating current. In addition, the proposed method can achieve stable control without transient characteristics in the inner unbalanced current, circulating cur-rents, and dc-link current, even under the unbalanced voltage condition.

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