ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Novel Implementation of Reversible Multiplexer Design Using MZI

Atluri Sarath Raja
M.Tech,
Usha Rama Engineering College,
Telaprolu, Vijayawada, Andhra Pradesh.

Padmanabaiah Gottipati, M.Tech
Associate professor 10 Years of Experience,
Usha Rama Engineering College,
Telaprolu, Vijayawada, Andhra Pradesh.

Abstract:

Reversible logic; transforms logic signal in a way that allows the original input signals to be recovered from the produced outputs, has attracted great attention because of its application in diverse areas such as quantum computing, low power computing, nanotechnology, DNA computing, quantum dot cellular automata, optical computing.Reversible computing has been proposed by several researchers as a possible alternative to address the energy dissipation problem. Several implementation alternatives for reversible logic circuits have also been explored in recent years, like adiabatic logic, nuclear magnetic resonance, optical computing, etc. Recently researchers have proposed implementations of various reversible logic circuits in the all-optical computing domain. Most of these works are based on semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI), which provides desirable features like low power, fast switching and ease of fabrication. In this paper we present an all-optical implementation of a digital multiplexer using MZI switches. Both non-reversible and reversible versions of multiplexer design are proposed, along with analytical evaluation of the design complexities both in terms of delay and resource requirements. Some techniques for optimizing the final optical netlists have also been proposed.

I.INTRODUCTION:

A multiplexer is a circuit that accepts many input but give only one output. Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates.

The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many input but only one output.By applying control signals, we can steer any input to the output. Few types of multiplexer are 2-to-1, 4-to-1, 8-to-1, 16-to-1 multiplexer.In the optical domain, a photon can store information in a signal having zero rest mass and provide very high speed. These properties of photon have motivated researchers to study and implement reversible circuits in optical domain. Theoretically from the decade old principles of Landauer and Bennett [2], reversible logic is considered as a potential alternative to low-power computing. Optical implementation of reversible gates can be one possible alternative to overcome the power dissipation problem in conventional computing. In recent times researchers have investigated various reversible logic gates and their all-optical implementations using micro- resonator and semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) switch . Also MZI-based implementation of reversible logic gates offer significant advantages like ease of fabrication, high speed, low power, and fast switching time [4], [14]. In this paper, an all-optical implementation methodology of reversible multiplexers has been proposed. Cost and delay analysis in implementing arbitrary functions using such mul- tiplexers have also been discussed. The rest of the paper is organized as follows. Section II provides a brief summary of MZI-based switch, reversible logic circuits, and implementing reversible logic gates using MZI-based switches. Section III describes the proposed all-optical multiplexer design method- ology, followed by discussions on implementing arbitrary functions in Section IV. Section V summarizes the results of experimental studies, followed by concluding remarks in Section VI.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

II.MACH-ZEHNDER INTERFEROMETER:

In this section we briefly discuss some relevant background about MZI-based optical switch, various reversible gates, and their all-optical implementations.

A.MZI-based all-optical switch :

Mach-Zehnder interferometer (MZI) is one of the efficient configurable building blocks in optical computing [19]. Some of the main advantages for using MZI switches in various circuit design methodologies are their compact size, ease of fabrication, thermal stability and fast switching time [3], [14]. Recently optical switches based on MZI have attracted many researchers in the area of all-optical reversible logic implementations [3], [8], [9], [12]. An all-optical MZI switch can be constructed using two SOA and two couplers. SOA amplifies an optical signal with- out converting it to electric signal and uses a semiconductor to administer the gain medium. A coupler is a passive optical component which can either combine or split a signal based on application requirement. Figure 1(a) shows the schematic diagram of a MZI switch. It consists of two input ports and two output ports. At the input port, the optical signal entering at port A is called the incoming signal (λ1) and the optical signal coming from port B is termed as control signal (λ2). The output ports are termed as bar port and cross port. The switch works as follows.

- When both incoming signal (λ1) at A and control signal (λ2) at B are present, there will be a presence of light at bar port and no light at cross port.
- When there is incoming signal (λ1) at A and no control signal (λ2) at B, then there is absence of light at bar port and presence of light at cross port.

If we represent presence of light as Boolean 1, and absence of light as Boolean 0, the working principle of the MZI switch can be expressed in terms of the following Boolean equations:

$$(A, B) \rightarrow (A.B, A.\overline{B})$$

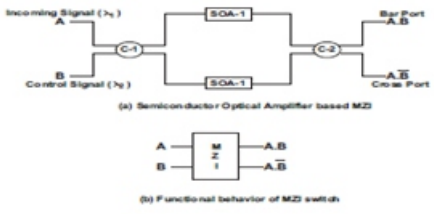


Fig. 1. SOA based MZI Switch

B. Reversible logic circuits

A Boolean function f : Bn → Bn is said to be reversible if it is one-to-one and bijective. In other words, for every input vector, there must be a unique output vector, and vice versa. A reversible logic circuit consists of a cascade of reversible gates, with several constraints. Specifically, the number of input and output lines must be equal, and there cannot be any fanouts or feedback connections [16]. Various reversible gates have been used by researchers for synthesizing reversible gate netlists, like NOT, CNOT [5], Toffoli [20], Fredkin [6], Peres [17], etc. In a reversible gate netlist, extra inputs are often added to make a function reversible, which are called constant input or ancilla input. The outputs that are not used in the circuit but required to maintain reversibility are called garbage outputs. In the proposed reversible multiplexer design, we have used one ancilla input line.

C. Implementing reversible gates using MZI switch:

Several researchers have studied and proposed all-optical implementations of reversible and non-reversible gates like Toffoli, Fredkin, Peres, XOR, NOR, etc. [3], [4], [13], [19], [22], and some function implementations like adder [9] and signed adder [1]. In all the works, the optical cost of implementation has been estimated as the number of MZI switches required, since the costs of beam splitters and beam combiners are relatively small. And the delay has been calculated as the number of stages of MZI switches multiplied by a unit Δ. Only one work exists in the literature that discusses about all-optical realization of multiplexer [12]; however, the pro- posed implementation using Feynman and Toffoli gates is costly both in terms of optical cost and delay. In the imple- mentation proposed in the present work, both the optical cost and delay are much smaller as compared to that in [12]. Figures 2 and 3 respectively show the all-optical realizations of a CNOT gate and a 3-input Toffoli gate. For the CNOT gate realization, the optical cost is 2, while the delay is 1Δ. Similarly, for the Toffoli gate realization, the optical cost is 3, while the delay is 2Δ. For a multiple-control Toffoli gate with n inputs, the optical cost is n, and the delay is [log2(n–)+ 1]Δ .

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

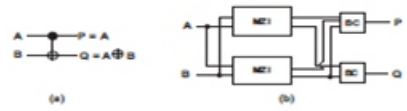


Fig. 2. All-optical CNOT gate realization

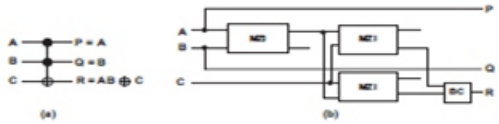


Fig. 3. All-optical Toffoli gate realization

$$M(1) = 2\ MZI$$
$$D(1) = 1\ \Delta$$

where $M(x)$ and $D(x)$ respectively denote the optical cost and delay for a $(2^x \times 1)$ multiplexer.

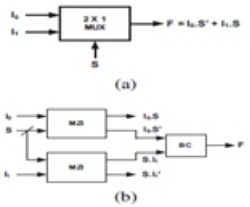


Fig. 4. A 2-to-1 MUX (a) schematic diagram, (b) all-optical implementation

III. PROPOSED ALL-OPTICAL MULTIPLEXER DESIGN:

In this section, we present the all-optical implementation of a digital multiplexer using MZI switches, beam splitters and beam couplers. In the following subsections, we discuss the design of a (2×1) non-reversible all-optical multiplexer, followed by its generalization to (2n×1) multiplexer. Then a design extension to make the multiplexer design reversible is suggested, that requires one additional ancilla line.

A.Design of (2×1) multiplexer :

The schematic diagram of a (2×1) multiplexer is shown in Figure 4(a), where I0 and I1 are the two inputs, and S is the select line. The function implemented at the output is also shown. The all-optical implementation of the multiplexer is shown in Figure 4(b), which consists of a beam splitter (BS) for splitting the select input S, two MZI switches which generates the subfunctions I0.S, I0.S, S.I1 and S.I 1 respectively, and finally a beam coupler (BC) that combines two of the MZI outputs to realize the desired functionality at the final output F. The BC essentially performs the logical OR function in the digital domain.

In the earlier reported works on implementing logic func- tions using MZI switches, BS and BC [8], [9], the cost of implementation (referred to as optical cost) has been estimated as the number of MZI switches required, as the relative costs of BS and BC are small. Similarly, the delay is measured as the length of the longest cascade of MZI switches. Denoting the units of cost and delay by MZI and Δ, for the implementation as shown in Figure 4(b).

B. Design of (2n ×1) multiplexer:

We now show how a multiplexer of any larger size can be constructed using smaller multiplexers as basic building blocks. This is a standard approach followed in conventional logic design; however, in the context of the present work, we shall be analyzing the costs and delays with respect to the all-optical implementations. A (4×1) multiplexer can be constructed using three (2×1) multiplexers, as shown in Figure 5(a), where I0, I1, I2, I3 are the inputs, S0, S1 are the select lines, and F is the output. Each of the three multiplexers can be replaced by their corresponding all-optical netlists, to get the final netlist as shown in Figure 5(b). For this implementation,

M(2) = 6 MZI

D(2) = 2 Δ

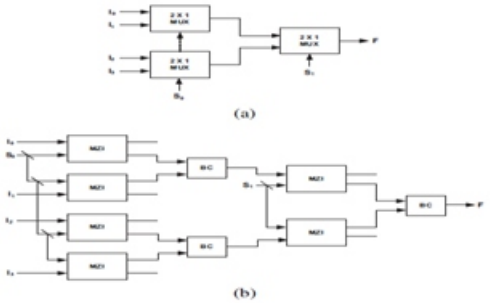


Fig. 5. A 4-to-1 MUX (a) schematic diagram, (b) all-optical implementation

Similarly, an (8 × 1) multiplexer can be built using two(4 ×1) and one (2×1) multiplexers, for which

M(3) = 62 + 2 = 14MZI

D(3) = 3 Δ

Generalizing, an (2n × 1) multiplexer can be built using two (2n−1 × 1) and one (2 × 1) multiplexers, as shown in Figure 6. We have seen earlier that M(1) = 2, M(2) = 6, and M(3) = 14. We can express the optical cost M(n) as a recurrence relation and solve it as follows

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

$$
\begin{aligned}
M(n) &= 2.M(n-1) + M(1) \\
&= 2.M(n-1) + 2 \\
&= 2[2.M(n-2) + 2] + 2 \\
&= 2^2.M(n-2) + 2^2 + 2 \\
&= 2^2[2.M(n-3) + 2] + 2^2 + 2 \\
&= 2^3.M(n-3) + 2^3 + 2^2 + 2 \\
&\vdots \\
&= 2^{n-1}.M(1) + 2^{n-1} + 2^{n-2} + \cdots + 2 \\
&= 2^n + 2^{n-1} + \cdots + 2 \\
&= (2^{n+1} - 2)\ MZI
\end{aligned} \qquad (1)
$$

C. Reversible implementation of the multiplexer:

The all-optical implementations of multiplexer as discussed in the previous subsection are not reversible. One possible

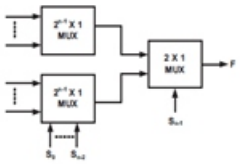


Fig. 6. A 2^n-to-1 MUX

approach to have a reversible implementation of a multiplexer is to define a suitable reversible embedding for a (2 × 1) multiplexer, and use it to build larger multiplexers. As an alternative, we can add an extra ancilla line and have a reversible implementation, as shown in Figure 7.

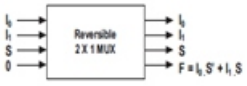


Fig. 7. Reversible multiplexer with one ancilla line

IV. IMPLEMENTING ARBITRARY FUNCTIONS USING MZI-BASED MULTIPLEXERS:

It is a well-known design practice to implement arbitrary logic functions using multiplexers. Any function of n variables can be implemented using an (2n−1 × 1) multiplexer, with an additional inverter if required. Figure 8(a) shows the truth table of an example 3-variable function, and Figure 8(b) the corresponding implementation using a (4×1) multiplexerAn all-optical implementation of the function is shown in Figure 8(c), which requires 6 MZI switches, 5 beam splitters, and 3 beam couplers.

A. Optimization rules:

It may be observed that in the all-optical multiplexer-based realization of functions, some of the MZI switches have constant inputs (0 or 1). Some of these MZI switches may be eliminated from the final netlist. These may be summarized in terms of the following four optimization rules.

a) If the upper input of a MZI switch is 0, both the outputs will be 0's and the switch can be deleted from the netlist. This is illustrated in Figure 9(a).

b) If the lower input of a MZI switch is 0, the upper output will also be 0, and the upper input will get copied to the lower output. In this case also, the MZI switch can be deleted (see Figure 9(b)).

c) If the upper input of a MZI switch is 1, the two outputs will be respectively the lower input and its complement. A MZI switch in this configuration can be used as an inverter (Figure 9(c)).

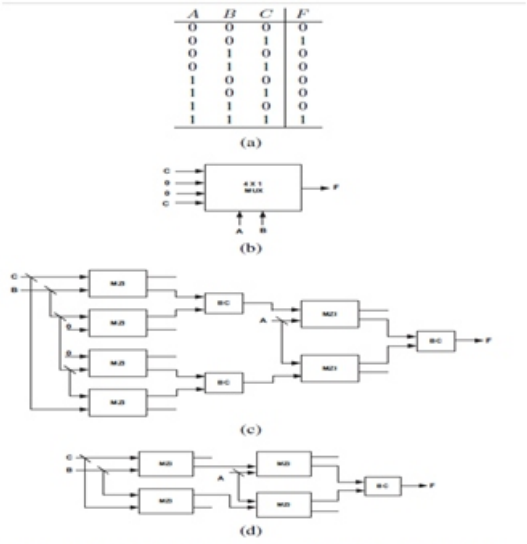


Fig. 8. Example function (a) truth table, (b) multiplexer realization, (c) all-optical implementation, (d) after applying optimization rules

d) If the lower input of a MZI switch is 1, the upper input gets copied to the upper output, and the lower output becomes 0. Here again the switch can be deleted (see Figure 9(d)).As an example, we apply the optimization rules to the all- optical netlist of Figure 8(c). After applying the rules, the netlist shown in Figure 8(d) results, which consists of 4 MZI switches, 3 beam splitters, and 1 beam coupler.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

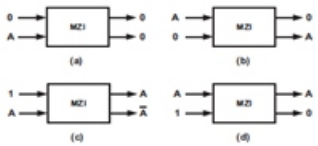
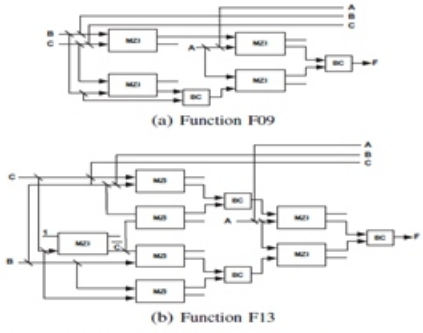


Fig. 9. The optimization rules

V. RESULTS AND ANALYSIS:

A summary of the results has been tabulated in Table I. Table I compares the optical costs and the delays for these 13 standard functions, for the proposed method against the corresponding costs reported by Kotiyal et al. [8]. The optical cost reported for the proposed method incorporates the optimization rules discussed in the previous section. It can be seen that the proposed implementations require significantly less number of MZI switches and also less delay as compared to [8]. The all-optical implementations of two of the functions (F09 and F13) after optimization using the rules are shown in Figure 10.



(a) Function F09

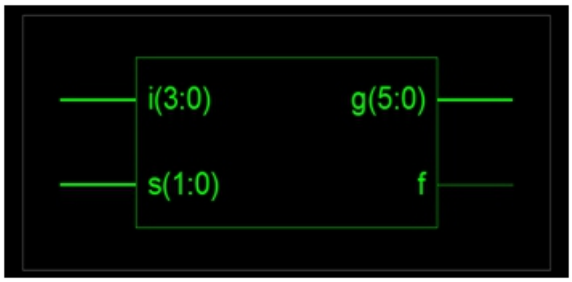
(b) Function F13

Fig. 10. All-optical implementation of two standard functions

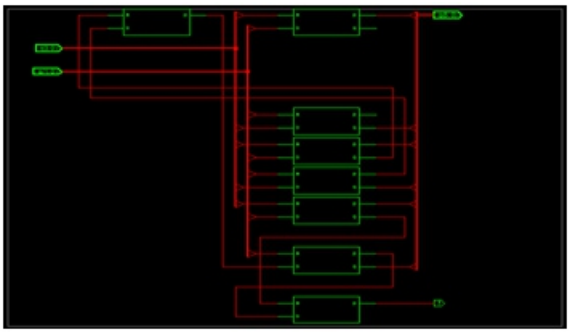
TABLE I: OPTICAL COST AND DELAY ANALYSIS COMPARISON FOR 13 STANDARD 3-VARIABLE BOOLEAN FUNCTIONS

Function No.	Standard Function	Kotiyal et al. [8]		Proposed Implementation	
		Optical Cost	Delay	Optical Cost	Delay
F01	$F = ABC$	6	4Δ	2	2Δ
F02	$F = AB$	3	2Δ	1	1Δ
F03	$F = ABC + AB'C'$	12	6Δ	4	3Δ
F04	$F = ABC + A'B'C'$	12	6Δ	5	3Δ
F05	$F = AB + BC$	5	3Δ	3	2Δ
F06	$F = AB + A'B'C$	10	6Δ	3	2Δ
F07	$F = ABC + A'BC' + AB'C'$	20	12Δ	6	3Δ
F08	$F = A$	2	1Δ	0	0Δ
F09	$F = AB + BC + AC$	10	6Δ	4	2Δ
F10	$F = AB + BC$	9	5Δ	4	2Δ
F11	$F = AB + BC + A'B'C'$	11	5Δ	4	2Δ
F12	$F = AB + A'B'$	7	4Δ	3	2Δ
F13	$F = ABC + A'B'C + AB'C' + A'BC'$	24	11Δ	7	3Δ

A summary of the synthesis and simulation results as shown in below figures.



(a)



(b)

RMD_MZI Project Status

Project File:	RMD_MZI.ise	Current State:	Synthesized
Module Name:	MUX_4to1	• Errors:	No Errors
Target Device:	xc3s100e-4vq100	• Warnings:	2 Warnings
Product Version:	ISE 9.2i	• Updated:	Wed 10 Jun 18:04:30 2015

RMD_MZI Partition Summary

No partition information was found.

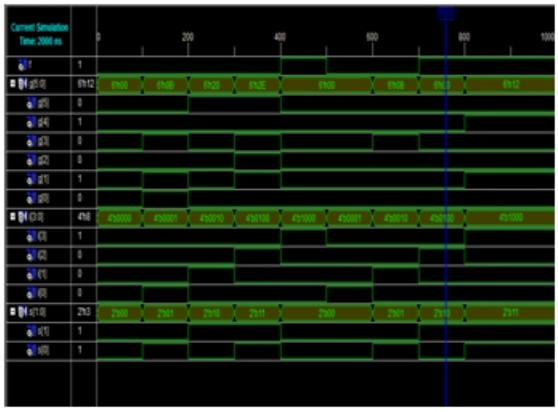
Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	4	960	0%
Number of 4 input LUTs	7	1920	0%
Number of bonded IOBs	13	66	19%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed 10 Jun 18:04:28 2015	0	2 Warnings	0
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

(c)



(d)

Fig.11.optical implementation of 4 to 1MUX (a),(b)RTL schematics,(c) synthesis summary (d) simulation results

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

VI. CONCLUSION:

The all-optical implementation of reversible multiplexers using MZI based switches have been presented in this paper, along with analysis of the corresponding costs and delays. A method for reversible implementation of functions using MZI switches and some optimization rules have also been presented. Experimental results for some of the proposed all-optical implementation results in significantly less delay as compared to the one based on conventional reversible gate implementations. Comparison with a recent work for the 13 standard 3-variable functions has also been reported, which demonstrates significant improvements both in terms of optical cost and delay.

REFERENCES:

[1] C. Bennett. Logical reversibility of computation. Journal of IBM Research and Development, 17:525–532, 1973.

[2] T. Chattopadhyay. All-optical symmetric ternary logic gate. Optics and Laser Technology, 42(6):1014–1021, 2010.

[3] T. Chattopadhyay. All-optical modified Fredkin gate. IEEE Journal of Selected Topics in Quantum Electronics, 18(2):585–592, 2012.

[4] R. Feynman. Quantum mechanical computers. Optic News, 11:11–20, 1985.

[5] E. Fredkin and T. Toffoli. Conservative logic. Inernational Journal of Theoretical Physics, 21:219–253, 1982.

[6] S. Kotiyal, H. Thapliyal, and N. Ranganathan. Mach-Zehnder interfer- ometer based all optical reversible NOR gate. In Proc. of IEEE Computer Society Annual Symposium on VLSI, pages 207–212, 2012.

[7] S. Kotiyal, H. Thapliyal, and N. Ranganathan. Mach-Zehnder interfer- ometer based design of all optical reversible binary adder. In Proc. of Design, Automation and Test in Europe (DATE), pages 721–726, 2012.

[8] G. Maity, T. Chattopadhyay, J. Roy, and S. Maity. All-optical reversible multiplexer. In Proc. of Computers and Devices for Communication (CODEC), pages 1–3, 2009.

[9] G. Maity, J. Roy, and S. Maity. Mach-Zehnder interferometer based all-optical Peres gate. In Proc. of Intl. Conf. on Advances in Computing and Communications, pages 249–258, 2011.

[10] M. Nielsen and I. Chuang. Quantum Computation and Quantum Information. Cambridge University Press, 2000.

[11] A. Peres. Reversible logic and quantum computers. Physical Review A (Atomic, Molecular, and Optical Physics), 32(6):3266–3276, 1985.

[12] C. Taraphdar, T. Chattopadhyay, and J. Roy. Mach-Zehnder interferome- ter based all-optical reversible logic gate. Optics and Laser Technology, 42(2):249–259, 2010.

[13] T. Toffoli. Reversible computing. Automata, Languages and Program- ming. Springer, Tech. Memo-MIT/LCS/TM-151, MIT Lab for Comp. Sci, 1980.

[14] M. Zhang, Y. Zhao, L. Wang, J. Wang, and P. Ye. Design and analysis of all-optical XOR gate using SOA-based Mach-Zehnder interferometer. Optical Communications, 223:301–308, 2003.