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High Performance SRAM Design for Future Memory Circuits

B.Manasa Reddy
Department Of Electronics and Communication Engineering, Teegala Krishna Reddy Engineering College, Meerpet, Hyderabad, Telangana-500005.

P.Sharmila Rani
HOD, Department Of Electronics and Communication Engineering, Teegala Krishna Reddy Engineering College, Meerpet, Hyderabad, Telangana-500005.

Dr.P.Ram Mohan Rao
Principal, Department of Electronics and Communication Engineering, Teegala Krishna Reddy Engineering College, Meerpet, Hyderabad, Telangana-500005.

Abstract:

In modern high performance integrated circuits, maximum of the total active mode energy is consumed due to leakage current. In high speed microprocessors and system on chip, SRAM array is main source of leakage current since majority of transistors are utilized for on-chip memory. Therefore the design of low leakage SRAM is required. Today's circuit designers are facing major problem of chip high power dissipation to exponentially growing cell density because of scaling down the technology in nanometer. This paper presents an extensive summary of the latest developments in low power circuit techniques. In this paper, SRAM cell using variable body bias technique is proposed and analyzed with respect to power dissipation for low voltage and energy constrain applications. This cell achieves low power dissipation due to its series connected tail transistors which reduces the leakage current in standby mode. The simulation result is based on 45nm CMOS environment.

Keywords:

SRAM Array, Variable body bias, leakage current.

I INTRODUCTION:

It has currently been an associate era of movable electronic devices like mobile phones, iPods, tablets etc… They ought to have an extended battery backup so that devices may be operational for lasting. Major part of the battery is drained by different peripheral parts like speakers etc.,. Next to them their memory parts consumes additional power from the battery. . Random-access device permits knowledge to directly access in any random order. Therefore, the time to access a given knowledge location varies considerably reckoning on its physical location.Static Random Access Memory (SRAM) is a style of semiconductor memory that uses bi-stable latching electronic equipment to store every bit. The term static differentiates it from dynamic RAM (DRAM) that should be sporadically invigorated. SRAM is volatile within the typical sense that knowledge is eventually lost once the memory isn't steam-powered. Low power and high-stability have been the main issues of SRAM designs as the demand of the portable electronic market constantly urges for less power-hungry architectures. Many techniques have been introduced to fulfill this requirement such as scaling the supply voltage, using multi threshold CMOS (MTCMOS) process to minimize the leakage, enhance its stability and to reduce dynamic power. When the design factors degrade, threshold voltage variations increases and is also linearly dependent on the reduction of the supply voltage. As a result, it is extremely difficult to maintain the cell stability as technology enters less than 100 nm regime.

Several more-than-6T SRAM cell designs are used to improve the stability and power dissipation .For increasing the battery standby time a replacement style of SRAM cell is proposed, which consumes less power than the prevailing SRAMs. In this paper a SRAM cell using variable body bias technique is proposed. A charge recycling technique is used to minimize the leakage currents and static energy dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. Tanner EDA tool is employed for simulation because of its accuracy and reliability. A comparative table of the power consumption of typical and projected SRAM is provided based on the result.

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The paper is organized as follows: Section II discusses about some existing SRAM cells, Section III describes circuit design and working principle of the proposed SRAM cell. Section IV describes the design and simulation of existing and proposed cell. Finally section V concludes the paper

II. EXISTING SRAM CELLS:

This section revolves round the performance comparison of SRAM cells consisting of different number of transistors to store single bit.

6T SRAM CELL:

Figure 1 shows the circuit diagram of a conventional SRAM cell. Word line (WL) is used for enabling the access transistors T2 and T5 for write operation. Bit lines BL and ¯BL are used to store the data and its compliment. For writing operation, one bit line is high and the other bit line is low. For writing "0", BL is low and ¯BL is high. When the word line (WL) is asserted high, transistors T2 and T5 are ON and any charge stored in the BL goes through T2-T3 path to ground. Due to zero value on ¯Q, the transistor T4 is ON and T6 is OFF. So the charge is stored at ¯Q line. Similarly in the write "1" operation, BL is high and ¯BL is low, due to this T6 is ON and the charge stored on Q is discharged through the T5-T6 path and due to this low value on the ¯Q , T1 is ON and T3 is OFF, so the charge is stored on the Q.

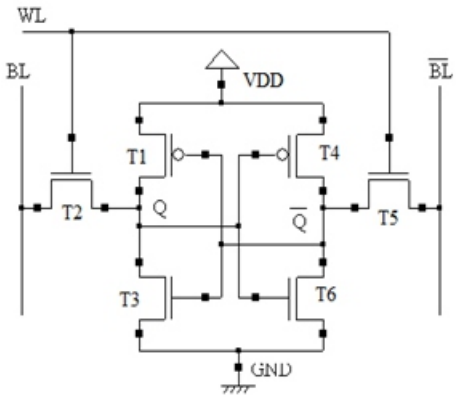

Figure 1. Conventional 6T SRAM cell.

Before the read operation of "1" at Q (for example) begins, BL and ¯BL are pre-charged to as high as Vdd. When the WL is selected, the access transistors T2 and T5 are turned ON.

Because of the pull-up transistor T1 ON and pull down transistor T3 OFF, voltage of BL will be nearly Vdd. On the other side, current will flow from the pre-charged ¯BL to ground, thus discharging ¯BL line through T5-T6 path to ground; T4 being OFF. Thus, a differential voltage develops between BL and ¯BL lines. This small potential difference between the bit lines is sensed and amplified by the sense amplifier at the data output.

12T MTCMOS SRAM CELL :

In MTCMOS technology, the SRAM cell is having low VT (LVT) transistors and high VT (HVT) transistors. The basic 4T SRAM cell is having LVT transistors. The two sleep transistors S1 and S2 used are of HVT type, while in sleep condition. Sleep transistors and a LVT Transmission gate (TG) in conjunction are used for reducing the wake up power during transition from sleep mode to active mode and sleep power during transition from sleep mode to active mode for writing operations of the SRAM cell. This reduces the static energy dissipation of the cell. In this structure two additional voltage sources are also used, one connected with the bit line and the other connected with the bit bar line in order to reduce the swing voltage at the output nodes of the bit and the bit bar lines. The reduction in swing causes the reduction in dynamic power dissipation. Because of very low leakage currents in MTCMOS technology, the stability of data retention is also enhanced.

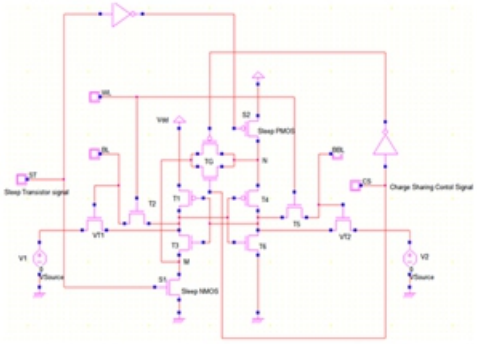

Figure2: SRAM Design Using MTCMOS Technique.

In MTCMOS design, extra mask layers for every worth of threshold voltage are needed for fabricating the transistors by selecting in step with their allotted threshold voltage values. This makes the fabrication method complicated. The techniques mentioned suffer from turning-on latency.

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III. PROPOSED SRAM CELL :

This paper proposes another SRAM architecture using "Variable body biasing" technique to achieve low power and higher stability. The proposed design uses 2 parallel connected sleep transistors at Vdd and 2 parallel connected sleep transistors at GND. The supply of one of the PMOS sleep transistor is connected to the body of alternative PMOS sleep transistor. Equally the supply of one of the NMOS sleep transistor is connected to the body of alternative NMOS sleep transistor. This is named as Body Biasing. In the proposed design, two voltage sources V1 and V2 are connected to the outputs of the BL and ¯BL respectively.

Two NMOS transistors VT1 and VT2 are used, one connected with the BL and the other with the ¯BL directly to switch ON and switch OFF the voltage sources during writing operations. NMOS sleep transistors connects node M (also called virtual ground node) to ground whereas the PMOS sleep transistors connects node N (also called the virtual supply node) to supply Vdd. Sleep transistors while in sleep condition disconnect logic cells from the supply and/or ground to reduce the current leakages in the sleep mode.

The LVT transmission gate TG is connected between the two nodes M and N for providing charge sharing. In the simulation, the sizes of the TG and the sleep transistors are chosen larger than the sizes of the logic cell transistors to maintain some trade-off between increased static plus dynamic power dissipations and higher wake up time of TG. The proposed design is illustrated in Figure 3. Sleep transistor signal ST and Charge sharing control signal CS provide the switching activity control on sleep transistors and TG, respectively.

A. Operation of Sleep Transistors:

Consider the configuration shown in Figure 3. NMOS sleep transistors connects the virtual ground node, i.e., node M in the figure, to the actual ground, whereas the other PMOS sleep transistors connects the virtual supply node i.e., node N in the figure, to the actual Vdd supply. During the active period, both types of sleep transistors are in the linear region and the voltage values of the virtual ground node M and virtual supply node N are equal to 0 and Vdd, respectively.

During Write "1" operation with active-to-sleep transition of the sleep transistors, these are turned off, and these are chosen to be high threshold devices, a very little sub-threshold leakage current is allowed to flow through them. Thus virtual nodes M and N are floating during the sleep time.

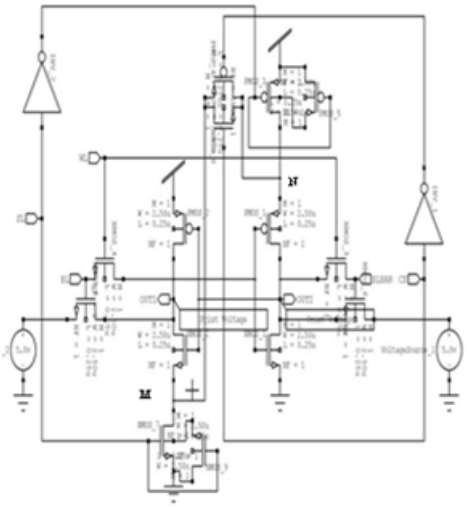

Figure 3: SRAM cell with variable body bias technique

Now, if the duration of the sleep period is sufficiently long, virtual ground node (M) will be charged up to some voltage value very close to Vdd by the leakage current. Similarly, if the duration of the sleep period is long enough, virtual supply node (N) will be discharged to some voltage value very close to 0 by the leakage current. If the total capacitances in the virtual ground node M and virtual supply node N are denoted by CM and CN , respectively, it is observed that during the active-to sleep transition, CM is charged up from 0 to very closely Vdd while CN is discharged from Vdd to very closely 0 for Write "1" operation.

During Write "0" operation, when the sleep to active transition edge arrives at the gates of the sleep transistors to turn them ON, the voltage of virtual ground node (M) starts to fall toward 0, whereas the voltage of virtual supply (N) starts to rise toward Vdd. Thus, CM will be discharged from Vdd to 0, while CN will be charged to Vdd from its initial value of 0 for Write "0" operation. These charging and discharging events on the virtual ground and virtual supply nodes are wasteful static energy dissipation from a circuit energy dissipation point of view.

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B.Charge Recycling Technique:

So to reduce the static energy dissipation as we switch between active and sleep modes of the circuit a charge recycling technique is used by adding a transmission gate TG between the virtual ground (M) and virtual supply (N) nodes as shown in Figure 3. The charge recycling strategy works as follows in connection with writing operations.

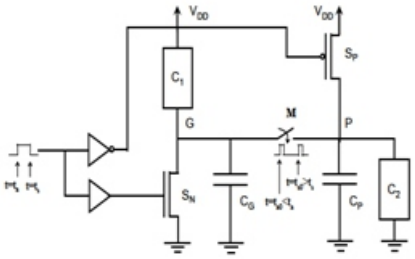

Figure 4: Charge-Recycling Technique

When the sleep-to-active transition edge arrives at the gates of the sleep transistors in proposed circuit, the voltage of GND node, "G" starts to fall towards zero, whereas the voltage of Vdd node, "P"starts to rise towards Vdd. The overall effective capacitance within the GND and VDD nodes is denoted by CG and CP. During active-to sleep transition, CG is charged up from zero to Vdd, whereas CP is discharged from Vdd to zero. During the sleep-to-active transition, CG is discharged from Vdd to zero, whereas CP is charged to Vdd from its initial value of zero. A charge-recycling technique is used to cut back the switching power consumption throughout the active-to-sleep and sleep-to-active transitions by adding a charge sharing switch between the GND and Vdd nodes as shown in Figure.Maximum energy saving of 50% is achieved by using the charge recycling technique. However, considering the power needed to turn on or off the TG, threshold voltage and size of TG, the total saving ratio is actually less than 50%.

C.Swing voltage

During switching activity from "0" to "1" or "1" to "0" at bit line or bit bar line swing voltage is required. This extra voltage increases the dynamic power dissipation. In the proposed SRAM model voltage sources V1 and V2 reduce the voltage swings and improve the switching activity during write operation. The dynamic power may be expressed as P dynamic = α CVdd V Swing f

Where C = Load capacitance; α = Activity factor; f =Clock frequency; VSwing = Voltage swing at output node; Vdd is the power supply voltage.So, one can observe that as the frequency increases the switching activity also increases and this increases the dynamic power dissipation. But the voltage sources reduce its voltage swing simultaneously at the output. So, at higher frequency the dynamic power dissipation is found to be almost constant.

Stability is also improved due to better switching capability of the proposed SRAM cell as compared to other SRAM cells. This design uses W/L ratio =3 for NMOS transistors and W/L ratio =6 for PMOS transistors within the main electrical converter portion. For the sleep transistors (NMOS and PMOS transistors) W/L ratio =1.The additional 2 transistors used for maintaining the logic state throughout sleep mode conjointly uses W/L ratio=1.

IV. SIMULATION AND RESULTS:

These circuits are designed and simulated using S-Edit, T-spice and W-edit of tanner tools 13.0.

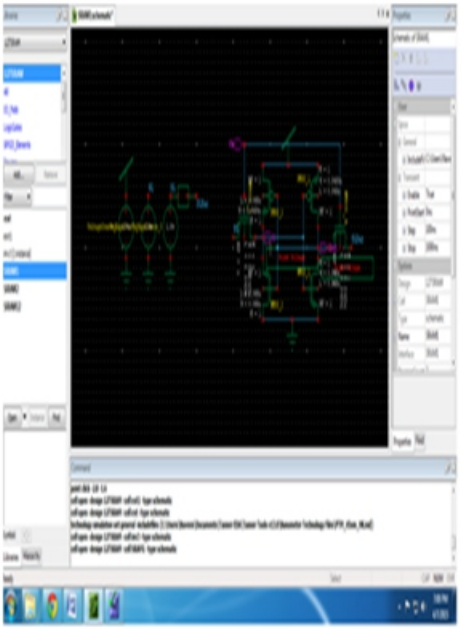

Figure 5: Conventional 6T SRAM Cell

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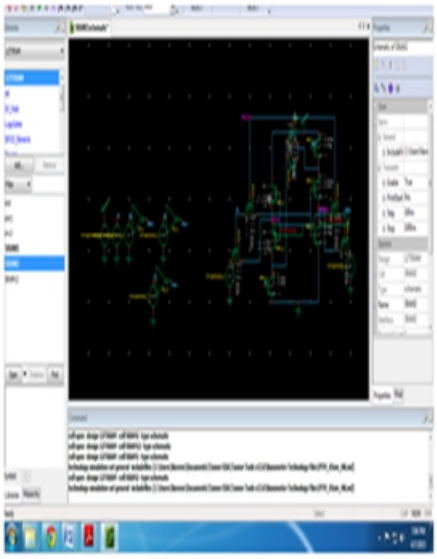

Figure 6: 12T MTCMOS SRAM Cell Design

Figure 7: Proposed SRAM Cell Design

Circuit	Power Consumption
Conventional 6T SRAM Cell	20.21035e $^{-006}$W
"12T"MTCMOS SRAM Cell	8.145905e $^{-006}$W
SRAM Cell with variable body bias technique	7.85627e $^{-006}$W

V.CONCLUSION:

In high speed memories the power dissipation is the main concern. In this paper the proposed Variable body bias SRAM cell effectively reduces both dynamic and static power dissipations. Although transistor count and area are increased in comparison to those of other SRAM cells but total low power dissipation and better stability can easily dominate over this drawback. This proposed SRAM cell can be used to provide low power solution in high speed devices like laptops, mobile phones, programmable logic devices etc. Schematic and analog simulations have been done at 0.18µm environment with the help of Tanner EDA.

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