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A Novel Leakage Reduction Technique Circuit Design for Ultra Low Power Applications

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Abstract:

Now-a-days the power dissipation is a major problem in electronic devices. The importance for power management Integrated Circuit (PMIC) is emphasized as battery-powered portable electronics such as smart phone are commonly used. Due to this problem static power dissipation is highly increased. In this paper we propose the use of a new DTMOS scheme in sub-threshold inverters. The results indicate that this scheme can provide better power efficiency than standard sub threshold DTMOS inverters. By using NAND DTCMOS to design the JKMS flip-flop design and 4x1mux design. The DTCMOS helps to achieve low power and high speed requirements. The Simulation results will be done in Tanner T-Spice at 45 nm.

Keywords:

DTCMOS, JK Flip-Flop ,PMIC.

I. INTRODUCTION:

In addition, analysis and development on high potency is crucial to maximise the utilization of moveable device that are most popular numerous functions than within the past. PMIC for prime potency sometimes amendment drastically from linear regulator to switch regulator. however the switch regulator have disadvantage of low potency compared with linear regulator at lightweight load conditions. Therefore, this paper is bestowed the mistreatment of switch regulator at significant load conditions. All power offer device of Mobile appliance should be created stable and numerous DC output voltage of high effectiveness from a unstable DC input power offer.

For that reason, it's used do an influence offer of Switched Mode Power offer(SMPS) methodology rather than an influence offer of typical linear methodology. Therefore, during this paper, the facility provides are designed mistreatment DT-CMOS that is low on-resistance than CMOS.

DTCMOS:

Switching loss is fixed cause, but conduction loss by on resistance of switch is increased by a output current increased. When output current is increased, conduction loss is increased more than switching loss in high output current. Finally, switch development that have low on-resistance to heighten efficiency of SMPS is essential.In this paper, we proposed available DT-CMOS without high leakage currents in high power supply voltages using this DT-CMOS's concept.

The proposed DT-CMOS in this paper can be seen in Fig. 3. When the switch is became ON, the body voltage of the switch MOS is controlled by diode connection CMOS and the threshold voltage is lowered. When the switch is became OFF, body of CMOS is connected to each the power supply and the ground.

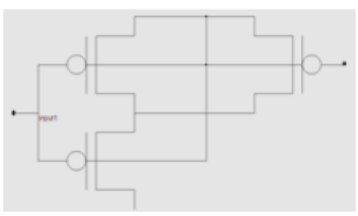

Fig1.PMOS DTCMOS

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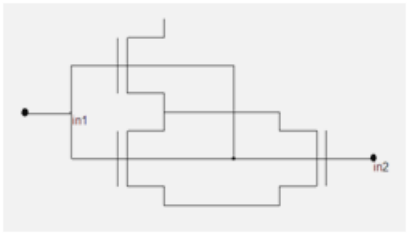

Fig2.NMOS DTCMOS

When the switch is ON, the proposed DT-CMOS due to low threshold voltage is low on-resistance than conventional CMOS switches. Limitation of power supply voltage by the leakage current is overcame by minimizing body leakage current that is a conventional DT-CMOS fault through deciding supply and the ground. In this paper, the DT-CMOS is designed with CMOS process on purpose to do one-chip of DT-CMOS and PFM control circuit. The DT-CMOS is designed with Deep-Nwell isolation from substrate and body to conventional silicon wafer as shown in Fig.4. One-chip of switching device and PFM control circuit are designed by this technique.

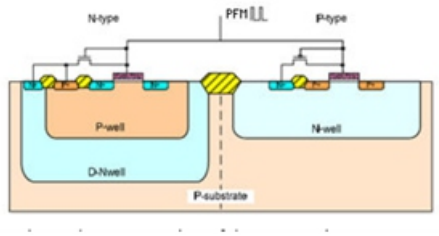

Fig3.The Cross Section of the Proposed DT-CMOS

DTCMOS NAND GATE:

A DTCMOS logic circuit for implementing a NAND perform comprising: initial, second and third transistors having a gate connected to receive initial, second and third logic signals, severally, and having a body contact connected to receive aforesaid third logic signal, said semiconductor units having serially connected drain-source connections; a fourth transistor serially connecting aforesaid initial, second associate degreed third semiconductor units to a voltage supply; and fifth and sixth transistors having gate connections connected to receive aforesaid second and third logic signals and having a source-drain connection connected in parallel with aforesaid fourth transistor source-drain connection forming an output node for aforesaid logic circuit

In that logic gate we square measure victimisation a sleep stack run reduction technique with DTCMOS and RBB to realize most potential static power reduction with optimized leads to terms of output wave form, dynamic power consumption and delay. within the active mode sleep switches S1 and S2 has been unbroken ON and within the ideal state these sleep switches has been unbroken OFF to chop off the trail of offer to ground.

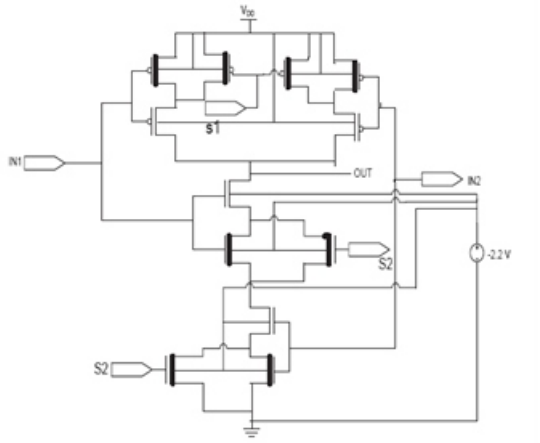

Fig4.Two input NAND gate with DTCMOS and RBB

NAND based JK Master-Slave Flip-flop::

The JK master-slave flip-flop designed with NAND gate shown in Fig. 5 . In that NAND gate we are using sleepy stack leakage reduction technique with DTCMOS and RBB to achieve maximum possible static power reduction with optimized results in terms of output waveform, dynamic power consumption and delay. In the active mode sleep switches S1 and S2 has been kept ON and in the ideal state these sleep switches has been kept OFF to cut off the path of supply to ground.

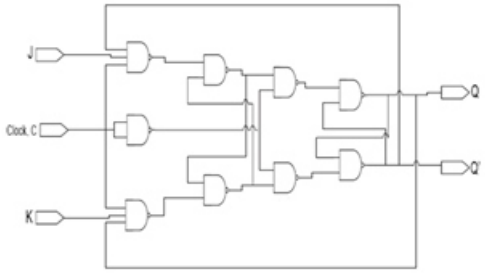

Fig5.NAND based JK Master-Slave Flip-flop circuit diagram

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3 NAND based 4*1 Multiplexer :

In electronics a multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. A 4*1 multiplexer has a Boolean equation where I0, I1, I2 and I3 are the four inputs, A and B are the selector inputs and Y is the output has been shown in Fig. 6. 4*1 multiplexer is designed using inverters, 3 inputs and 4 inputs NAND gate. These inverters and NAND gates are designed with sleepy stack with RBB approach so as to achieve minimum possible leakage power consumption, dynamic power consumption and delay. The simulation have been done to get the dynamicpower consumption by keeping sleep switches on and static power consumption by keeping the sleep switches off.

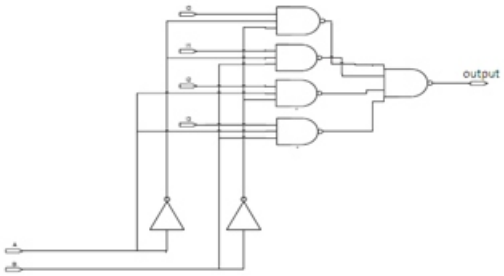

Fig.6. 3 NAND based 4*1 multiplexer circuit diagram.

SCHEMATIC:

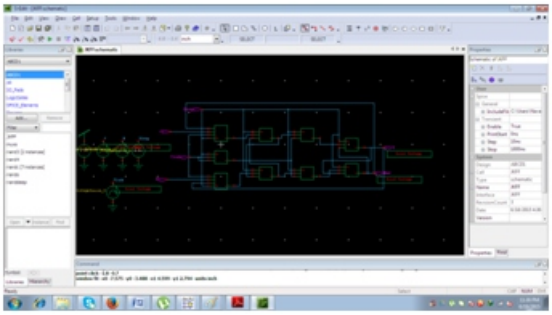

Fig.7 Output of NAND based JK Master-Slave Flip-flop

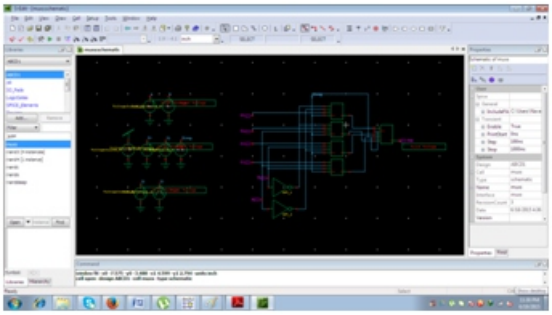

Fig.8 Output of 3 NAND based 4*1 multiplexer

SIMULATION RESULTS:

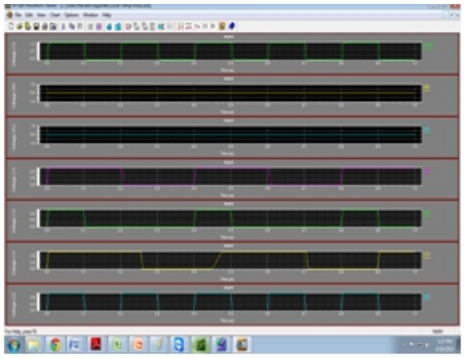

Fig.9 Output waveform of 4*1 multiplexer

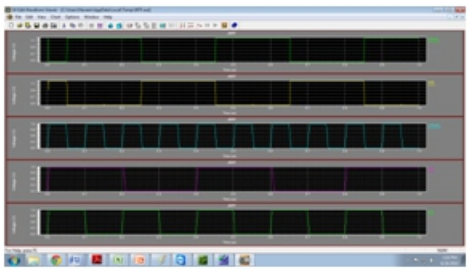

Fig.10 Output waveform JK master-slave flipflop

CONCLUSION:

In paper we propose a new power gating technique with DTCMOS. This DTCMOS method makes the sleep transistors to operate in high threshold region so that the leakage was reduced. Here we shows the power comparisons of Nand gate and Sleepy Nand gates and designed the applications JK Flip-Flop and Multiplexers using Sleepy Stack approach.

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