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A Novel Topology of Network Fault Tolerant Voltage Source Converter HVDC Transmission System

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Abstract:

This paper proposes a new breed of high-voltage dc (HVDC) transmission systems based on a hybrid multilevel voltage Source converter (VSC) with ac-side cascaded h-bridge cells. The proposed HVDC system offers the operational flexibility of VSC based systems in terms of active and reactive power control, black start Capability, in addition to improved ac fault ride-through capability and the unique feature of current-limiting capability during Dc side faults. Additionally, it offers features such as smaller footprint and a larger active and reactive power capability curve than existing VSC-based HVDC systems, including those using modular multilevel converters. To illustrate the feasibility of the proposed HVDC system, this paper assesses its dynamic performance during steady-state and network alterations, including its response to ac and dc side faults.

I. INTRODUCTION:

In this world, the converters may be isolated into two gatherings that are to be familiar by their operational standard. One gathering desires an AC system to work in additionally called as line commutated converters. regular HVDC employs on line commutated converters. The second gathering of converters does not require AC systems to work and is along these lines called as self commutated converters. Contingent upon the configuration of the DC circuits this gathering can be further partition into current source converters as well as voltage source converters. A current source converter works with a soft DC current give by a reactor, at the same time as a VSC works with a smooth DC voltage gave by storage capacitor. Along with the identity commutated converters it is predominantly the VSC that has enormous history in the lower power range for modern commute applications.

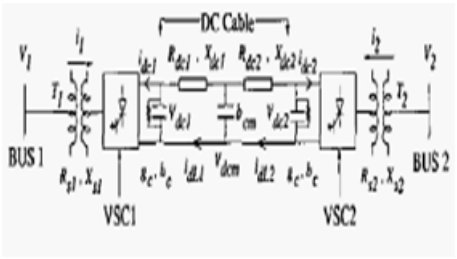

Fig 1: Schematic representation of VSC based HVDC

There are two approaches to assist VSC-HVDC transmission systems to ride-through dc side faults. The first approach is to use a fast acting dc circuit breaker, with considerably high let-through current to tolerate the high dc fault discharge current that may flow in the dc side. This breaker must be capable of operating at high voltage and isolates temporary or permanent dc faults, plus have a relatively high-current-breaking capacity.

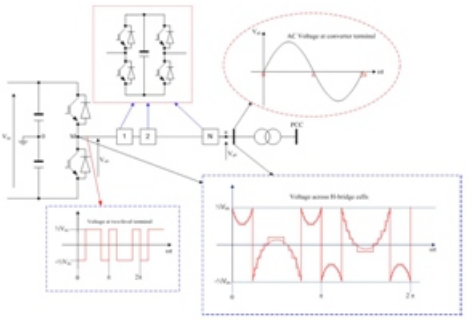

Fig 2: Hybrid voltage multilevel converter with ac side cascaded H-bridge cells.

However, this first step is inadequate, as the operating voltage of present VSC-HVDC transmission systems reach 640 kV pole-to-pole (or 320 kV for a bi-polar configuration), with power-handling capability of 1 GW. This breaker approach may introduce significant steady-state losses due to the semiconductors in the main current path.

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Each converter station must be able to block current flow between the ac and dc sides during a dc fault, allowing dc-side capacitor discharge current, which is the major component of the dc fault current, to decay to zero and then isolate the fault. Several converter topologies with this inherent feature have been proposed, including an H-bridge modular multilevel converter, an alternative arm modular multilevel converter, and a hybrid multilevel converter with ac-side cascaded H-bridge cells. However, the drawback is that the active power exchange between the ac networks reduces to zero during the dc fault period. Commensurate with the second approach, this paper presents a new HVDC transmission systems based on a hybrid-voltage-source multilevel converter with ac-side cascaded H-bridge cells. The adopted converter has inherent dc fault reverse-blocking capability, which can be exploited to improve VSC-HVDC resiliency to dc side faults. With coordination between the HVDC converter station control functions, the dc fault reverse-blocking capability of the hybrid converter is exploited to achieve the following:

• eliminate the ac grid contribution to the dc fault, hence minimizing the risk of converter failure due to uncontrolled over current during dc faults;
• facilitate controlled recovery without interruption of the VSC-HVDC system from dc-side faults without the need for opening ac-side circuit breakers;
• simplify dc circuit breaker design due to a reduction in the magnitude and duration of the dc fault current; and
• improve voltage stability of the ac networks as converter reactive power consumption is reduced during dc-sidefaults.

Section II of this paper describes the operational principle and control of the hybrid voltage source multilevel converter with ac-side cascaded H-bridge cells.
Section III describes the HVDC system control design, specifically, ac current controller in synchronous reference frame, dc link voltage, and active power, and ac voltage controllers. A detailed block diagram that summarizes howdifferent control layers of the proposed HVDC transmission system are interfaced is presented.
Section IV presents simulations of a hybrid converter HVDC transmission system, which demonstrate its response during steady-steady and network disturbances. Included are simulations of four quadrant operation, voltage support capability, and ac and dc fault ride-through capabilities.

II. HYBRID MULTILEVEL VSC WITH AC-SIDE CASCADED H-BRIDGE CELLS:

Fig. 2 shows one phase of a hybrid multi level VSC with N H-bridge cells per phase. It can generate 4N+1 voltage levels at converter terminal "a" relative to supply midpoint "o." The two-level converter that blocks high-voltage controls the fundamental voltage using selective harmonic elimination (SHE) with one notch per quarter cycle, as shown in Fig. 2. Therefore, the two-level converter devices operate with 150-Hz switching losses, hence low switching losses and audible noise are expected. The H-bridge cells between "M" and "a" are operated as a series active power filter to attenuate the voltage harmonics produced by the two-level converter bridge.

These H-bridge cells are controlled using level-shifted carrier-based multilevel pulse width modulation with a 1-kHz switching frequency. To minimize the conversion losses in the H-bridge cells, the number of cells is reduced such that the voltage across the H-bridge floating capacitors sum to (1/2)Vdc . This may result in a small converter station, because the number of H-bridge cells required per converter with the proposed HVDC system is one quarter of those required for a system based on the modular multilevel converter. With a large number of cells per phase, the voltage waveform generated across the H-bridge cells is as shown in Fig. 2, and an effective switching frequency per device of less than 150 Hz is possible.

The dc fault reverse-blocking capability of the proposed HVDC system is achieved by inhibiting the gate signals to the converter switches, therefore no direct path exists between the ac and dc side through freewheel diodes, and cell capacitor voltages will oppose any current flow from one side to another. Consequently, with no current flows, there is no active and reactive power exchange between ac and dc side during dc-side faults. This dc fault aspect means transformer coupled H-bridges cannot be used. The ac grid contribution to dc-side fault current is eliminated, reducing the risk of converter failure due to increased current stresses in the switching devices during dc-side faults.

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From the grid standpoint, the dc fault reverse-blocking capability of the proposed HVDC system may improve ac network voltage stability, as the reactive power demand at converter stations during dc-side faults is significantly reduced. The ac networks see the nodes where the converter stations are connected as open circuitnodes during the entire dc fault period. However, operation of the hybrid multilevel VSC requires a voltage-balancing scheme that ensures that the voltages across the H-bridge cells are maintained at Vdc/N under all operating conditions, where is the total dc link voltage. The H-bridge cells voltage balancing scheme is realized by rotating the H-bridge cell capacitors, taking into account the voltage magnitude of each cell capacitor and phase current polarity. An additional PI regulator is used to ensure that the cell capacitors be maintained Vdc/N at as depicted in Fig. 2(b) (inner control layer).

III. CONTROL SYSTEMS:

A HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H-bridge cells requires three control system layers. The inner control layer represents the modulatorand capacitor voltage-balancing mechanism that generates the gating signals for the converter switches and maintains voltage blance of the H-bridge cell capacitors. The intermediate control layer represents the current controller that regulates the active and reactive current components over the full operating range and restraints converter station current injection into ac network during network disturbances such as ac and dc side faults. The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points to the current controllers. The inner controller has only been discussed to a level appropriate to power systems engineers. The intermediate and outer control layers are presented in detail to give the reader a sense of HVDC control system complexity.The current, power, and dc link voltage controller gains are selected using root locus analysis, based on the applicable transferfunctions. Some of the controller gains obtained using root locus analysis give good performance in steady state but failed to provide acceptable network disturbance performance. Therefore, the simulation final gains used are adjusted in the time domain to provide satisfactory performance over a wide operating range, including ac and dc side faults. Fig. 2 summarizes the control layers of the hybrid multilevel VSC.

Current Controller Design:

The differential equations describing the ac-side transient and steady-state are

$$\frac{di_d}{dt} = -\frac{R}{L}i_d + \frac{1}{L}(V_{cd} - V_d + \omega L i_q) \quad (1)$$

$$\frac{di_q}{dt} = -\frac{R}{L}i_q + \frac{1}{L}(V_{cq} - V_q - \omega L i_d). \quad (2)$$

Assume

$$\lambda_d = V_{cd} - V_d + \omega L i_q \quad \text{and} \quad \lambda_q = V_{cq} - V_q - \omega L i_d$$

$$\frac{di_d}{dt} = -\frac{R}{L}i_d + \frac{1}{L}\lambda_d \quad (3)$$

$$\frac{di_q}{dt} = -\frac{R}{L}i_q + \frac{1}{L}\lambda_q. \quad (4)$$

The new control variables and can be obtained from two proportion-integral controllers (PI) having the same gains:

$W_d = K_i \int (i_d^* - i_d)dt$ and $W_q = K_i \int (i_q^* - i_q)dt$

To facilitate control design in state space, the integral parts of

And are replaced by and, rearranged in the following form:

$$\lambda_d = K_p (i_d^* - i_d) + W_d \quad (7)$$

$$\lambda_q = K_p (i_q^* - i_q) + W_q. \quad (8)$$

The integral parts, in differential equations form, are

$$\frac{dW_d}{dt} = -K_i i_d + K_i i_d^* \quad (9)$$

$$\frac{dW_q}{dt} = -K_i i_q + K_i i_q^*. \quad (10)$$

After substitution of (7) and (8) into (3) and (4), two identical and independent sets of equations, suitable for control design, are obtained as

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dW_d}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+K_p)}{L} & \frac{1}{L} \\ -K_i & 0 \end{bmatrix} \begin{bmatrix} i_d \\ W_d \end{bmatrix} + \begin{bmatrix} \frac{K_p}{L} \\ K_i \end{bmatrix} i_d^* \quad (11)$$

$$\begin{bmatrix} \frac{di_q}{dt} \\ \frac{dW_q}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+K_p)}{L} & \frac{1}{L} \\ -K_i & 0 \end{bmatrix} \begin{bmatrix} i_q \\ W_q \end{bmatrix} + \begin{bmatrix} \frac{K_p}{L} \\ K_i \end{bmatrix} i_q^*. \quad (12)$$

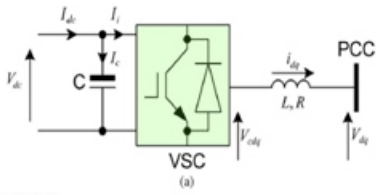

Fig. 2. (a) Representation of VSC station

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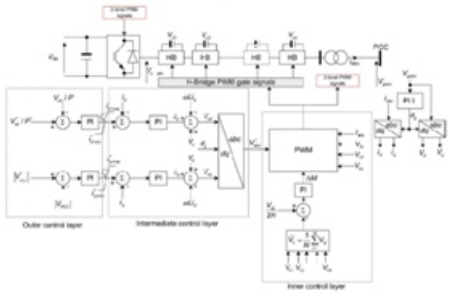

(b) schematic diagram summarizing the control layer of the hybrid multilevel converter with ac side cascaded

After Laplace manipulations of the state-space equations in (11) and (12), one transfer function is obtained for and , which is used for the current controller design

$$\frac{i_d(s)}{i_d^*(s)} = \frac{i_q(s)}{i_q^*(s)} = \frac{\frac{K_p}{L}s + \frac{K_i}{L}}{s^2 + \frac{(R+K_p)}{L}s + \frac{K_i}{L}}.$$

Equations relating the reference voltages to the modulator and, current controller output, and feed forward terms can beObtained from expressions for and as follows:

$$V_{cd}^* = \lambda_d + V_d - \omega L i_q \quad (13)$$
$$V_{cq}^* = \lambda_q + V_q + \omega L i_d. \quad (14)$$

Based on (5), (6), (13), and (14), the structure of the current controller shown in Fig. 2(b) (intermediate layer) is obtained.DC Voltage Controller: Based on Fig. 2, the differential equation describing the converter dc-side dynamics is

$$C\frac{dv_{dc}}{dt} = I_{dc} - I_i. \quad (15)$$

Assuming a lossless VSC, dc power at the converter dc link must equal the ac power at converter terminal. Therefore, (15) can be written as from

$$C\frac{dV_{dc}}{dt} = I_{dc} - \frac{(V_{cd}i_d + V_{cq}i_q)}{V_{dc}}. \quad (16)$$

Equation (16) can be linearized using a Taylor series with the higher order terms neglected. Therefore, the linearized form of (16) is

$$\frac{d\Delta V_{dc}}{dt} = \frac{\Delta I_{dc}}{C} - \frac{V_{cd}}{CV_{dc}}\Delta i_d - \frac{V_{cq}}{CV_{dc}}\Delta i_q - \frac{i_d}{CV_{dc}}\Delta V_{cd} - \frac{i_q}{CV_{dc}}\Delta V_{cq} + \frac{(V_{cd}i_d + V_{cq}i_q)}{CV_{dc}^2}\Delta V_{dc}. \quad (17)$$

$$\Delta u_{dc} = k_{pdc}(\Delta V_{dc}^* - \Delta V_{dc}) + k_{idc}\int (\Delta V_{dc}^* - \Delta V_{dc})\,dt. \quad (18)$$

Equation (17) can be reduced

$$\frac{d\Delta V_{dc}}{dt} = \frac{\Delta u_{dc}}{C} + \frac{P_{ac}}{CV_{dc}^2}\Delta V_{dc} \quad (19)$$

To where V_{dc} represents reference dc link voltage. Let the new control variable introduced for the integral part of the dc voltage controller be Δz_{dc}, therefore:

$$\frac{d\Delta V_{dc}}{dt} = -\frac{1}{C}\left(K_{pdc} - \frac{P_{ac}}{V_{dc}^2}\right)\Delta V_{dc} + \frac{1}{C}\Delta z_{dc} + \frac{\Delta V_{dc}^*}{C} \quad (20)$$

$$\frac{d\Delta z_{dc}}{dt} = K_{idc}(\Delta V_{dc}^* - \Delta V_{dc}). \quad (21)$$

The state equations in (20) and (21) in matrix form are:

$$\frac{d}{dt}\begin{bmatrix}\Delta V_{dc}\\ \Delta z_{dc}\end{bmatrix} = \begin{bmatrix}-\left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV_{dc}^2}\right) & \frac{1}{C}\\ -K_{idc} & 0\end{bmatrix}\begin{bmatrix}\Delta V_{dc}\\ \Delta z_{dc}\end{bmatrix} + \begin{bmatrix}\frac{K_{pdc}}{C}\\ K_{idc}\end{bmatrix}\Delta V_{dc}^*. \quad (22)$$

Equation (22) in the s-domain is

$$\begin{bmatrix}\Delta V_{dc}(s)\\ \Delta z_{dc}(s)\end{bmatrix} = \frac{1}{\Gamma}\begin{bmatrix}s & \frac{1}{C}\\ -K_{idc} & s + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV_{dc}^2}\right)\end{bmatrix}\begin{bmatrix}\frac{K_{pdc}}{C}\\ K_{idc}\end{bmatrix}\Delta V_{dc}^* \quad (23)$$

Where

$$\Gamma = s^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV_{dc}^2}\right)s + \frac{K_{idc}}{C}$$

$$\begin{bmatrix}\Delta V_{dc}(s)\\ \Delta z_{dc}(s)\end{bmatrix} = \begin{bmatrix}\frac{\frac{K_{pdc}}{C}s + \frac{K_{idc}}{C}}{s^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV_{dc}^2}\right)s + \frac{K_{idc}}{C}}\\ \frac{K_{idc}\left(s - \frac{P_{ac}}{CV_{dc}^2}\right)}{s^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV_{dc}^2}\right)s + \frac{K_{idc}}{C}}\end{bmatrix}\Delta V_{dc}^*. \quad (24)$$

From (24) the transfer function for the dc voltage controller is

Where $\overline{v}_{cd}$ and $\Delta\overline{v}_{cd}$ are normalized by V_{dc}^*.

Active Power Controller: The active power controller sets the reference active current component i_d^* assuming a constant voltage at the PCC as follows:

$$i_d^* = K_{pp}(P^* - V_d^* i_d) + K_{ip}\int (P^* - V_d^* i_d)\,dt. \quad (27)$$

Assume the voltage vector at the PCC is aligned with the-axis and its magnitude is regulated at V_d^* as $V_q^* = 0$ as, and

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represents active power reference. After replacing the integral part with a new control variable, the following sets of equations result:

$$i_d^* = K_{pp}\,(P^* - V_d^* i_d) + z_p \qquad (28)$$

$$\frac{dz_p}{dt} = K_{ip}\,(P^* - V_d^* i_d)\,. \qquad (29)$$

After substituting (28) into (11), the following state space representation for the power controller is obtained:

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dz_d}{dt} \\ \frac{dz_p}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+K_p+K_pK_{pp}V_d^*)}{L} & \frac{1}{L} & \frac{K_p}{L} \\ -(K_i+K_iK_{pp}V_d^*) & 0 & K_i \\ -K_{ip}V_d^* & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ z_d \\ z_p \end{bmatrix} + \begin{bmatrix} \frac{K_pK_{pp}}{L} \\ K_iK_{pp} \\ K_{ip} \end{bmatrix} P^*$$

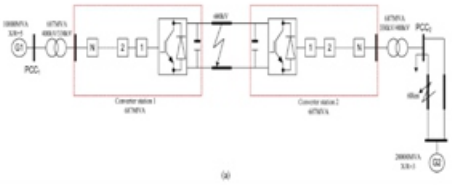
Where we have (30), shown at the bottom of the page.
AC Voltage Controller: The reference reactive power current component is set by the ac voltage controller as

$$i_q^* = K_{pv}\,(|V_{ac}^*| - |V_{ac}|) + K_{iv}\int (|V_{ac}^*| - |V_{ac}|)\,dt$$

Where $|V_{ac}^*|$ represents reference voltage magnitude at PCC.
However, the gains for the ac voltage controllers are obtained using a trialoand-error search method that automatically runs the overall system simulation several times in an attempt to find the gains that produce the best time domain performance.

$$\frac{P(s)}{P^*(s)} = V_d^* \times \frac{i_q(s)}{P^*(s)} = V_d^* \times \frac{\frac{(K_iK_{pp}+K_iK_{pp}+K_pK_{ip})}{L}s + \frac{K_i}{L}}{s^3 + \frac{(R+K_p+K_pK_{pp}V_d^*)}{L}s^2 + \frac{(K_i+K_iK_{pp}V_d^*+K_pK_{ip}V_d^*)}{L}s + \frac{K_iK_{ip}V_d^*}{L}} \qquad (30)$$

IV. PERFORMANCE EVALUTION:



Test network along with waveforms signifying the steady-state operation of HVDC system supported on hybrid voltage source multilevel converter with ac side cascaded H-bridge cellsWaveforms signifying ac fault ride-through competence of HVDC transmission systems supported on hybrid voltage multilevel converter with ac side cascaded H-bridge cells.

Waveforms demonstrating dc fault ride-through competence of HVDC transmission systems supported on hybrid voltage multilevel converter with ac side cascaded H-bridge cells.A.t A. test network and waveforms demonstrating the steady-state operation of HVDC system based on hybrid voltage source multilevel converter with ac side cascaded h-bridge cellsFigures are show converters 1 and 2 active and reactive power exchange trade with Pcc1 and Pcc2 separately.

The converters have the capacity to change their reactive power exchange with Pcc1 and Pcc2 to backing the voltage accompanied by the entire working period. Figures are demonstrate that converter 2 modifies its reactive power exchange with Pcc2 when the heap is acquainted at t=2 s with backing the voltage magnitude.

Figures are demonstrate that converter 2 infuses and display high-quality current and voltage waveforms into Pcc2 with no ac channels introduced. Figure shows that the voltage stresses over the H-scaffold cell capacitors of converter 1 are controlled to the in demand set point amid the complete period. Figure representation the total dc link voltage across converter over converter 2, which controls the dc link voltage.

In light of these outcomes, the proposed VSC-HVDC system has the capacity meet essential enduring state fundamentals, for example, procurement of voltage backing as well as four quadrant operations without exchanging off the voltage and current stresses on the converters switches.

Fig 4.2: active and reactive power converter station 1 exchanges with Pcc1

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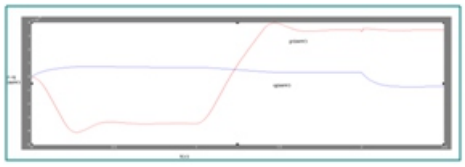

Fig 4.3: active and reactive power converter station 1 exchanges with Pcc2

Fig 4.4: voltage magnitude at Pcc2

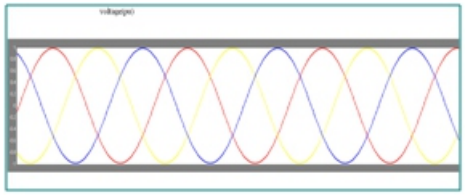

Fig 4.5 :voltage waveforms at Pcc2

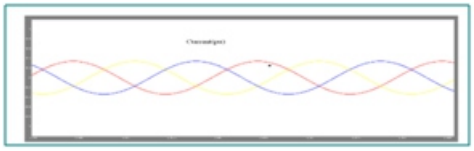

Fig 4.6: current waveforms converter station 1 exchanges with pcc1

Fig 4.7:voltage across 21 cell capacitors of the three phases of converter 1

Fig 4.8: voltage across the dc link of converter station 2

B. Waveforms demonstrating ac fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells.

To exhibit the ac problems ride-through ability of the introduced HVDC system, the test system is subjected to a 140 ms three-stage fault to ground at the area demonstrated in Figure.

Amid the deficiency period the power charge to converter 1 is diminished in extent to the decrease in the ac voltage size (this is accomplished by detecting Pcc2 voltage).

This is to minimize the two-level converter dc link voltage rise in light of the caught energy in the dc side, since power can't be exchanged as the voltage at Pcc2 breakdown. Figure shows the outcomes when the test system exchange 0.5 Pu (343.5 MW) from matrix G1 and G2 and is subjected to the three-stage insufficiency at t=1s.

Figure demonstrates the active and reactive power converter 1 exchanges with Pcc1 Note that converter 1 matches its active power send out G2 to minimize the ascent of converter 2 dc link voltage as its capacity to infuse active power into lattice G2 decreases with the voltage breakdown at Pcc2, as demonstrated in Figure and expressed previously.

Figure demonstrates the active and reactive powers that converter 2 infuses into Pcc2. The system has the capacity recover when the shortcoming is cleared, as well as converter 2 alters its reactive power exchange with network G2in request bolster voltage at Pcc2.

The homeless people indicated of active and reactive powers at PCC2 are identified with the response of the ac voltage controller that directs the air conditioner voltage Pcc2 Figure demonstrates that the voltage size at pcc1remains unaffected; affirming that the cross breed voltage source multilevel converter does not bargain the HVDC transmission system's decoupling element regardless of receiving active power coordinating at converter 1, as clarified.

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Figure demonstrates that converter 2 controls its commitment to the fault current to not as much as full load current in spite of the voltage at Pcc2 give up in to 20% of its appraised voltage, because of converter 2's present controller. Figure demonstrates that coordination of the HVDC controllers, as showed, minimizes the effect of ac side blames on the transient power flow on the dc side, consequently minimizing aggravation on the dc link voltage.

Figure demonstrates that the H-scaffold cell voltage burdens are controlled as the framework rides through the ac side fault. This affirms that the many-sided quality of a HVDC framework in light of the half breed multilevel VSC does not exchange off its ac shortcoming ride-through capacity. Figure demonstrates the half and half multilevel VSC shows improbable voltage to the converter transformer, with low consonant substance and dv/dt. This may allow clearance of ac side channels and the utilization of standard protection ac transmission transformers.

The outcomes in Figures are exhibited to exhibit the capacity of the proposed HVDC system to work in flawed networks,\ autonomous of its working point and fault length of time. This case exhibits the prevalence of current-constraining VSCs more than a synchronous generator amid ac system aggravations. (Converter 2 present infusion Pcc2 into is constantly controlled and not as much as full load appraised current notwithstanding the insufficiency span and the measure of force trade between air conditioning systems G1and G2

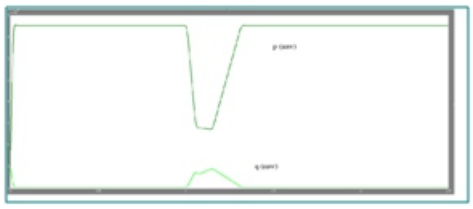

Fig 4.9: Active and reactive power converter 1 exchanges with pcc1

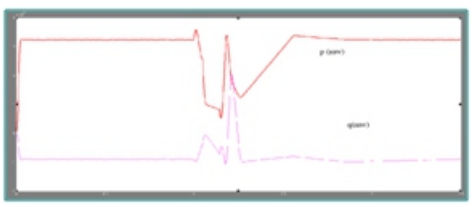

Fig 4.10 :Active and reactive power converter to injects into pcc2

Fig 4.11: Voltage magnitude at pcc1

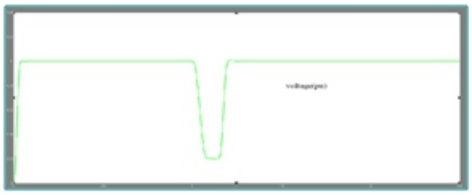

Fig 4.12: Voltage magnitude at pcc2

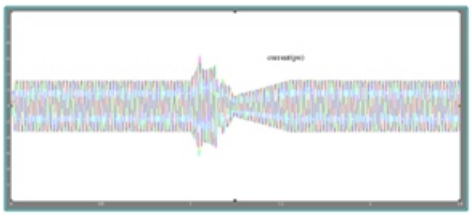

Fig 4.13: Current waveforms converter 2 injects into pcc2

Fig 4.14: Converter2 dc link voltage.

Fig 4.15:Voltage across 21 H-bridge cells of the converter 2.

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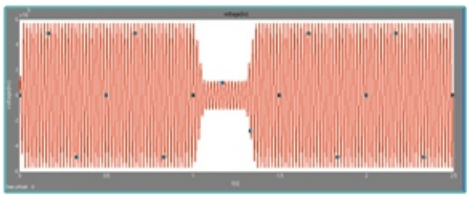

Fig 4.16: Line-to-line voltage waveform at the terminal of converter 1 (before transformer

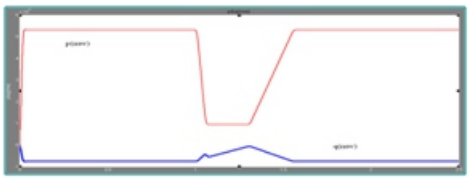

Fig 4.17: Active and reactive power at PCC1.

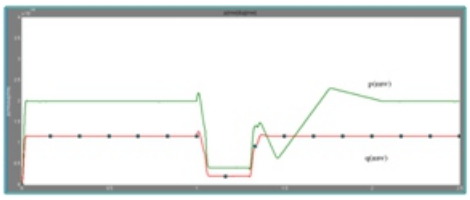

Fig 4.18 :Active and reactive power at PCC2.

Fig 4.19: Voltage magnitude at Pcc1

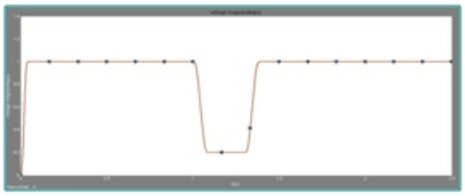

Fig 4.20: Voltage magnitude at PCC2

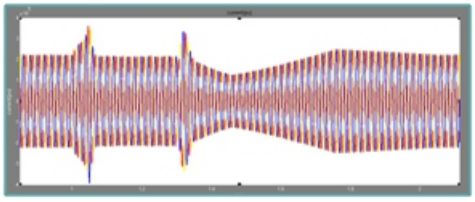

Fig 4.21:Current waveforms converter 2 injects into PCC2.

Fig 4.22: Converter 2 dc link voltage.

Fig 4.23: Voltage across the 21 H-bridge cell capacitors of converter 2

C. Waveforms demonstrating dc fault ride through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells.Figure demonstrates the outcomes when the test system is subjected to a brief strong post to-shaft dc fault at the centre of the dc link. Figures are demonstrates the active power and reactive power that converter stations 1 and 2 exchange with Pcc1 and Pcc2. Watch zero active power and reactive power exchanges between the converter stations and ac lattices G1 and G2 amid the deficiency period, subsequently there is no present stream in the switches of converters 1 and 2. Figures demonstrates that the present surge experienced by both converter stations causes detectable voltage plunging at Pcc1 and Pcc2 because of expanded utilization of reactive power amid system start-up and dc join voltage assemble up taking after lack flexibility. The surge in active and reactive powers in both converter stations happens as the dc side capacitors challenge to charge from both ac sides; this causes an extensive current flow from both ac sides to the dc side to charge the dc link capacitors and link disseminated capacitors as indicated in Figures.

The outcomes in Figures likewise show the advantages of dc shortcoming converse blocking ability innate in this mixture system, as the converter switches encounter high current magnify just amid dc link voltage assemble up. Figure demonstrates that converter 2 dc join voltage recoups to the pre-fault state after the issue is cleared. Notice the getting better period for the dc link voltage is generally long; this is the major fault of the proposed HVDC systems as it uses a typical dc link capacitor.

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Figure is extends the dc issue current and demonstrates the 60-kA crest perishes to zero in less than four cycles (for 50 Hz) after release of dc connection and link circulated capacitors. Figures are likewise demonstrates the ac systems begin to add to the dc link current after the issue is cleared, to charge the dc side capacitors. Figure is demonstrates the voltage over the 21 H-extension cells of the converter stations 1 and 2 (every gathering of follows articulate to voltages over 7 H-scaffold cell capacitors in every phase).

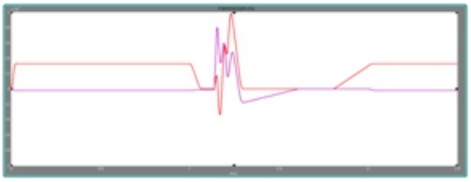

Fig 4.24: Active and reactive power converter 1 exchanges with Pcc1

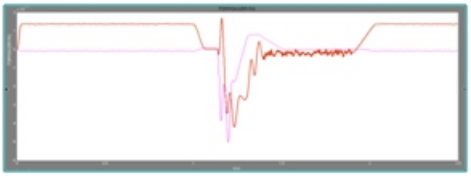

Fig 4.25: Active and reactive power converter 2 exchanges with Pcc2

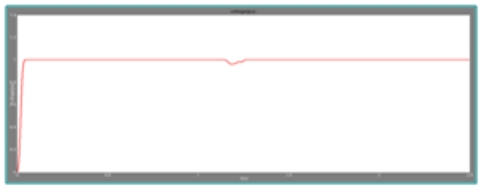

Fig 4.26: Voltage magnitude at Pcc1

Fig 4.27: Voltage magnitude at Pcc2

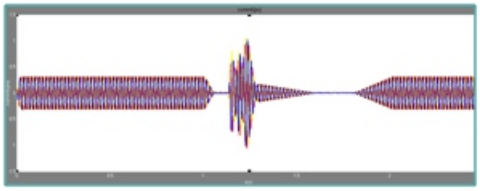

Fig 4.28: Current waveforms converter 1 exchange with grid G1 at Pcc1

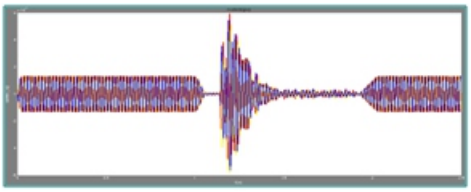

Fig 4.29: Current waveforms converter 2 exchange with grid G2 at Pcc2

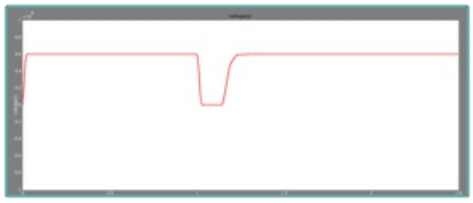

Fig 4.30: Converter 2 dc link voltage

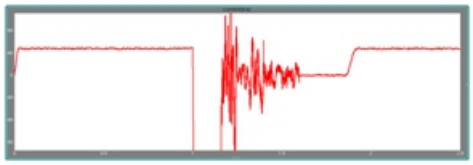

Fig 4.31: Zoomed version of dc link current demonstrating the benefits of dc fault reverse blocking capability.

V.CONCLUSION :

This project existence on the recent generation VSC-HVDC transmission system supported on a hybrid multilevel converter by means of ac-side surge H-bridge cells. The most important advantages of the future HVDC system are: Prospective small footprint along with minor semiconductor losses put side by side to current HVDC systems. Little filtering requirements on the ac sides and presents high-quality voltage to the converter transformer. Does not compromise the advantages of VSC-HVDC systems such as four-quadrant operation; voltage support capability; and black-start capability, which is vital for connection of weak ac networks with no generation and wind farms.

Modular design and converter fault management (inclusion of redundant cells in each phase may allow the system to operate normally during failure of a few H-bridge cells; whence a cell bypass mechanism is required). Resilient to ac side faults (symmetrical and asymmetrical). Inherent dc fault reverse blocking capability that allows converter stations

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to block the power paths between the ac and dc sides during dc side faults (active power between ac and dc sides, and reactive power exchange between a converter station and ac networks), hence eliminating any grid contribution to the dc fault current.

VI.REFERENCES:

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