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A Proposed Pulse Triggered Flip Flop Design for CDN Networks

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ABSTRACT:

As technology was growing the demand of low power devices are more concern. In order to increase the performance of the system there was a rapid change in the system design .Low Power research major concern in today's VLSI world. In order to reduce the power consumption of circuits we look for design of a lower power clocking system, because clock system consumes about 70% of power dissipation of the total system. So here we propose the Pulse triggered Flip-Flop in order to reduce the power Consumption of the circuit. These Pulse Triggered Flip-Flips are designed and analyzed using Tanner T-Spice using TSMC018 Technology.

Keywords:

pulse-triggered flip-flop (FF), Clock System, clocking system.

1.INTRODUCTION:

Over the past decade, power consumption of VLSI chips has constantly been in-creasing. Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the number of on-chip transistors increase about 40% every year. The operating frequency of VLSI systems increases about 30% every year. Al-though capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems can not improve as fast as the power consumption increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving Consumption of the clock tree system.

Instead of traditional Master-Slave Flip-Flop a P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network .

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power economical than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs have lengthened discharging path in latch design, which leads to inferior timing characteristics.The situation deteriorates further when low-power techniques such as conditional capture, conditional pre-charge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch.

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Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches. In this paper, we will present a novel low-power explicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

Explicit Pulse Triggered Flip-Flop:

Explicit Pulse triggered Flip-Flop consists of Pulse generator and a Latch network.

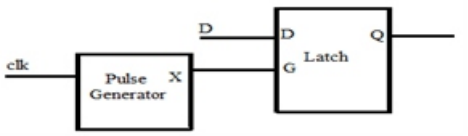

Fig1: Block Diagram of Pulse Triggered Flip-Flop

Where as in Pulse triggered flip flops, a short pulse around the rising (or falling) edge of the clock is created through a pulse generator circuit.

This pulse acts as the clock input to a latch.

Pulse Generator:

The Pulse generator consists of and gate and whose inputs are clk and another was delayed of clock signal by three inverters which will be used for generating the strobe signals.

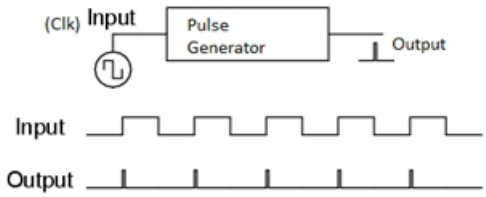

Figure 2: Pulse Generator

The duration of each output pulse is set by components in the pulse Generator itself. This can be done using of a time-delay circuit with a very short delay time.

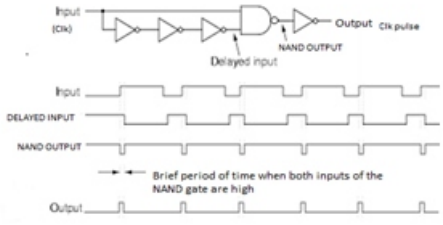

Figure 3: Output Signal using Pulse Generator

Implementing this timing function with logic gates is done as it shows the time delay within every logic gate (known as propagation delay). An input signal (Clock) and split it up two ways, then placing a gate or a series of gates in one of those signal paths just to delay it a bit, then have both the original signal and its delayed counterpart enter into a two-input gate that outputs a high signal for the brief moment of time and the delayed signal.The output is obtained for a short duration. Figure 2 is an example for producing a clock pulse on a low-to-high input signal transition.

IMPLEMENTATION EXPLICT DATA CLOSE TO OUTPUT FLIP FLOP:

The basic Explicit Flip-Flip was Ex-DCO(Explicit Data Close Flip-Flop)Flip-Flop as shown below.

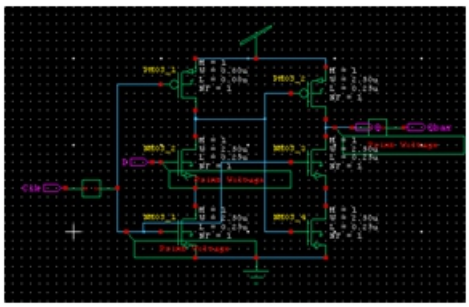

Fig4: Explicit Data Close Flip-Flop

In Explicit Data Close Flip-Flop it has a unwanted discharge problem whenever it has static input 1 case. In order to reduce we introduce a Conditional discharge mechanism to reduce power dissipation.

CONDITIONAL DISCHARGE DATA CLOSE TO OUTPUTFLIP FLOP:

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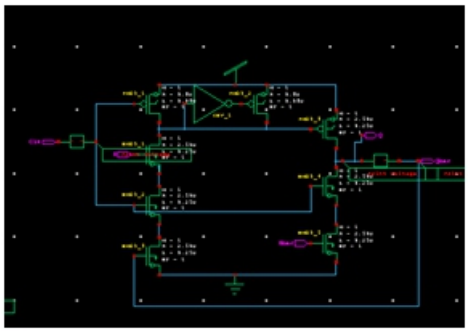

Fig5: CDFF Flip-Flop

An extra n MOS transistor controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up p MOS transistor. The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown above. It uses a pulse generator as in [9], which is suitable for double-edge sampling. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. If the input is HIGH in the sampling window, the internal node is discharged, assuming that were initially (LOW, HIGH) for the discharge path to be enabled. As a result, the output node will be charged to HIGH through PMOS of D input in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input was LOW during the sampling period, then the first stage is disabled, and node retains its pre-charge state. Whereas, node will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data.

STATIC CONDITIONAL DISCHARGE FLIP FLOP:

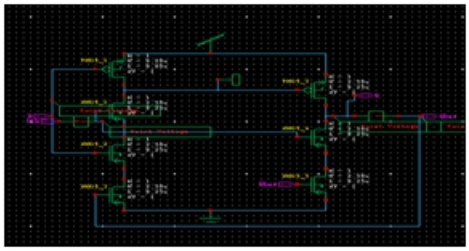

Fig6: Static CDFF structure

Static CDFF has same operation but it doesn't consist of pre-charging as present in dynamic structure. So, it take longer time for processing.

Modified Hybrid Latch Flip-Flop:

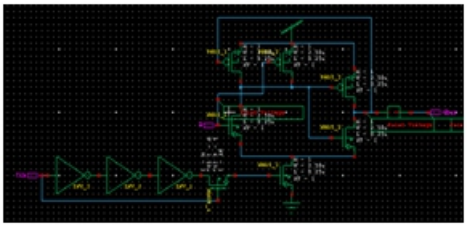

Fig 7: MHLFF

In MHLFF we reduce the longer stack of NMOS transistor at output node in order to increase the speed of the Flip-Flop. It also flows the static latch structure whose pre-charging was depend on the data. MHLFF drawback is that internal node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".

PROPOSED PULSE TRIGGERED FLIP-FLOP:

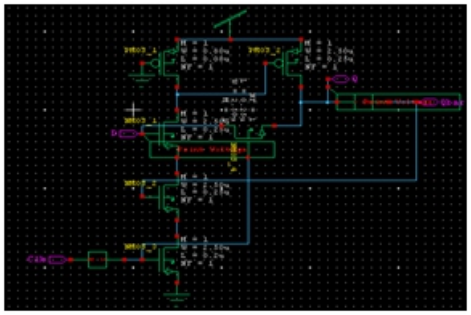

Fig8: Proposed Flip-Flop

They there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor with gate connected to the ground.This gives rise to a pseudo-n MOS logic style design, and the charge keeper circuit for the internal node X can be saved .In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [20], [21]. Second, a pass transistor controlled by the pulse clock is included so that input data can drive node Q of the latch directly. The pull down network of output node was reduced so the we reduce the discharge path.

PROPOSED FLIP-FLOP WITH ENHANCE PULSE:

The proposed Flip-Flop consists of 24 transistors are used to design the Flip-Flop. In order to reduce the no of transistor count here we introduce Pass transistor based pulse generator design which useful to reduce the no of transistors so as the power dissipation.

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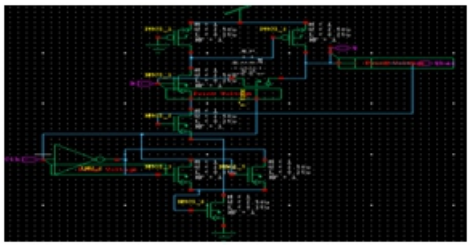

Fig9: Proposed Flip-Flop with Enhance Pulse

SIMULATION:

These Flip-Flops are designed and simulated using T-Spice using TSMC018 Technology.

Fig10: Explicit Data Close Flip-Flop

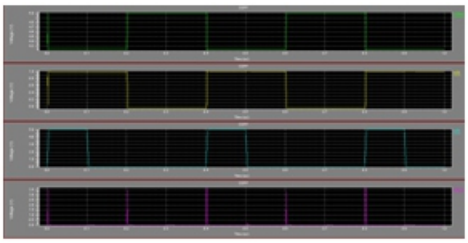

Fig11: Conditional Discharge Data Close To Output Flip Flop

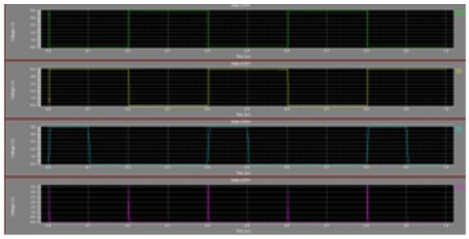

Fig 12: Static Conditional Discharge Data Close To Output

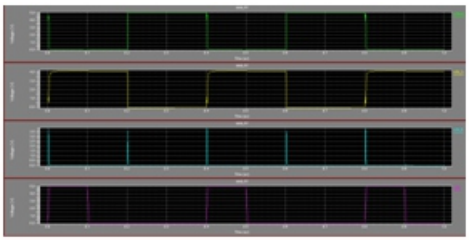

Fig13: Modified Hybrid Latch Flip-Flop

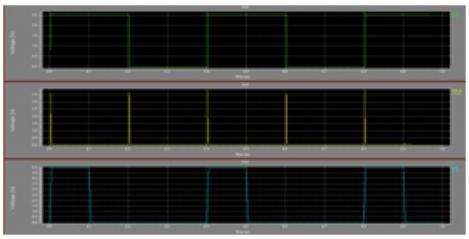

Fig14: Proposed Pulse Triggered Flip Flop

COMPARISON TABLE:

Circuit	Power Dissipation	Delay
DCO	1.780866e-002 watts	7.9248e-008
CDFF	3.486329e-003 watts	7.9248e-008
Static CDFF	3.576771e-003 watts	9.6062e-008
MHLFF	2.393216e-005 watts	4.7318e-008
PFF	2.239547e-007 watts	9.6025e-008

Table 1: Comparison Table

CONCLUSION:

In this paper we modified the existing true single phase clocked lath in oder to reduce the dynamic power consumption and to reduce the delay we proposed a new proposed Flip-Flop which was designed with less area and less power consumption

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