ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

# Design and simulation of 4-bit ALU Design using GDI Technique for Low Power Application on Microwind 2.6K

Mr.Arshadali Rahut
Department of Electronics & Communication Engineering
B.V.B College of Engineering & Technology, Hubli, Karnataka.

Dr. Anil V Nandi
Department of Electronics & Communication Engineering
B.V.B College of Engineering & Technology, Hubli, Karnataka.

Mr.S.S.Kerur
Department of Electronics & Communication Engineering
S.D.M. College of Engineering & Technology, Dharwad, Karnataka.

Dr Harish Kittur
VLSI Division,
School of Electronics,
VIT Vellore.

## Abstract:

The purpose of this paper is the designing and implementation of an Arithmetic Logic Unit (ALU) using Gate-Diffusion-input (GDI) technique. The main sub-blocks of ALU are Adder, Substractor, shifter and Logical Block. This work evaluates and compares the performance and optimized area of ALU with Static CMOS technique and GDI technique in 90nm CMOS(6 Metal) process technology. Simulations are performed by using Microwind2.6k tool using Verilog file 90nm CMOS technology. At first, using DSCH 2.7f Tool, the circuits are implemented with Static CMOS technology and then with GDI techniques. Simulations results validate the proposed concept and verify that GDI technique decreases the area and power used by ALU.

## Keywords:
ALU, GDI, CMOS, Low Power, Power Dissipation, Area.

## Introduction :

A processor is a main part of any digital system. And an ALU is one of the main components of a microprocessor.To give a simple analogy, CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They consist of fast dynamic logic circuits and have carefully optimized structures. Of total power consumption in any processor, CPU accounts a significant portion of it. ALU also contribute to one of the highest power density locations on the processor, as it is clocked at the highest speed and is busy mostly all the timewhich results in thermal hotspots and sharp temperature gradients within the execution core. Therefore , this motivate us strongly for a energy efficient ALU designs that satisfy the high performance requirements, while reducing peak and average power dissipation.[1,2] Basically ALU is a combinational circuit that performs arithmetic and logical operations on a pair of n bit operands for e.g. The typical internal structure of a 3 bit ALU is shown in Fig.1. The architecture can be modified similarly for lower bits. Our work is divided into following sections: Section (I) give description of various units and operations of ALU, Section (II) briefly presents the designing of various ALU components such as Mux, adder, logic gates etc. using conventional Complementary design. Sections (III) present the GDI technique. Section (IV) present the simulation results and performance analysis of various ALU blocks with complementary and GDI technique and comparison of their performance & optimized area. Finally the work is concluded in Section (V).

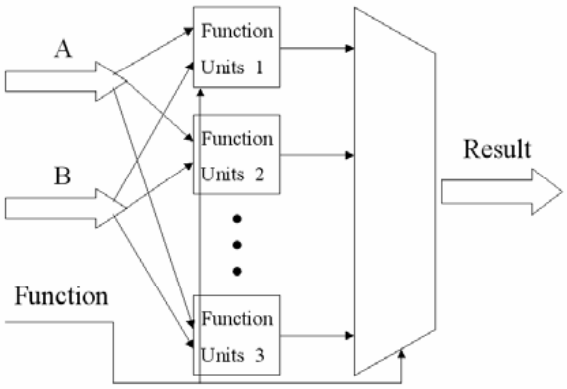


Fig.1 internal structure of ALU

## I ARITHMETIC LOGIC UNIT:

### 1.1 Arithmetic Unit:

Employing fast and efficient adders in arithmetic logic unit will aid in the design of low power high performance system. Other operations such as subtraction and multiplication also employ addition in their operations, and their internal hardware is almost similar though not identical to addition hardware.Various adder families have been proposed in the past to trade-off power, area and speed for possible use in ALUs.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The performance criticality of the ALU demands a dynamic adder implementation. Dynamic logic family of adders are the most efficient in terms of transistor-count, speed and power dissipation. This work covers the design of 4bit adder using Complementary logic. This same Adder unit is used for the implementation of subtractor unit. This reuses the current hardware we made for adder and saves area.

### 1.2 Logic Unit:

ALU can perform various logic operations like NOT, AND, OR, NAND, NOR, XOR, XNOR etc. For these operations a special unit is made called as Logical Unit. This Logic Unit performs all logic operations asked to perform. A MUX operated by select lines, for which particular logic operation to perform, is used inside this logic block.

### 1.3 Low Power ALU using 4:1 MUX:

There is a substantial increase in the standby mode leakage power. As technology scales Reducing the power consumption of the ALU of high-end processors is important not only because they consume a considerable percentage ofprocessor energy, but also because they are one of the most active and busiest component of the processor . As a result of that they dissipate a lot of dynamic energy. This is aggravated by the exponential dependence of leakage on the temperature, & ALU also become a site of high leakage. The total leakage of the ALU can be given as

IS,T=N.IS,i

Where, N= number of transistors in the ALU

IS,i= sub threshold leakage of gate i which is a function of gate length L.

Similarly, the dynamic power of the ALU is given as

ID=α.Ceff.Vdd2.f

where α is the switching factor

Ceff. is the total effective capacitance

Vdd is the supply voltage

& f is the frequency of operation.

## II. COMPONENTS DESIGN WITH COMPLEMENTARY LOGIC:

The various components are designed using complementary logic(CMOS logic). Figure shows the schematic design of various components such as ADDER, MUX, LOGICAL GATES (NOT,OR,EXOR).

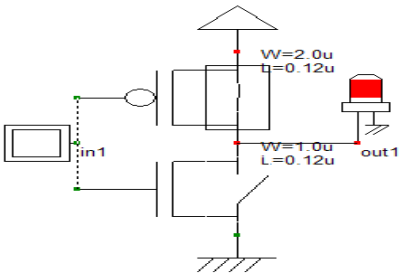


Fig.2 Inverter Using CMOS Logic

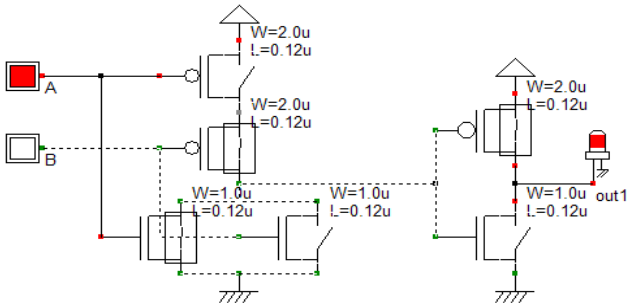


Fig.3 2-input OR gate using CMOS Logic

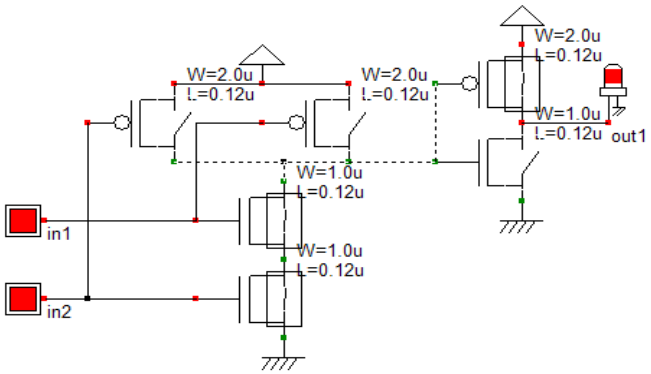


Fig.4 2-input AND gate using CMOS Logic

Mostly all the other circuits are implemented with the above three gate circuit.

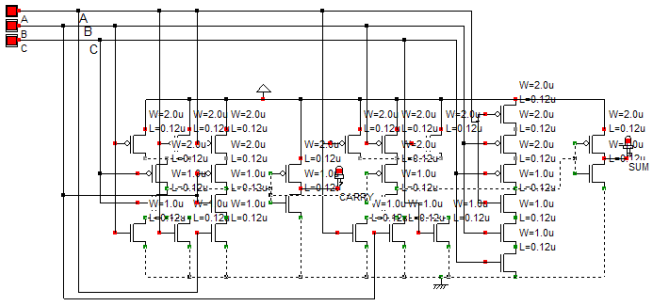


Fig.5 1-bit adder circuit using CMOS Logic

Similarly subtractor is implemented. Also with this logic MUX can be implemented. The schematic of 2:1 MUX is given below

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

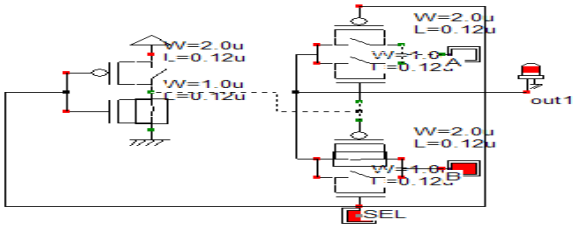


Fig.6 2:1 MUX using CMOS technology Here A and B are inputs SEL is select line

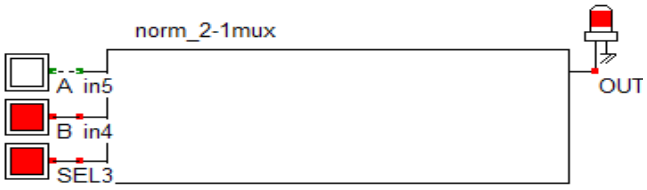


Fig.7 Cell representation of MUX

Using the CMOS logic MUX in ALU. results in more power consumption and more area for chip. So in order to get a more optimized and low power consuming circuit we've to used a technique where the number of transistor used will be less. That's why we will use one of the such techniques known as Gate- Diffusion-Input (GDI) method.

## III. GDI METHOD AND COMPONENTS DESIGN:

The Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in Fig. 8. One may be think of the CMOS inverter in the first look of this circuit, but there are some major differences in the two, (I) The GDI cell contains three inputs—G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to thesource/drain of NMOS). (II) Bulks of NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast to CMOS inverter.[4] The basic GDI cell is shown in Fig. 8.

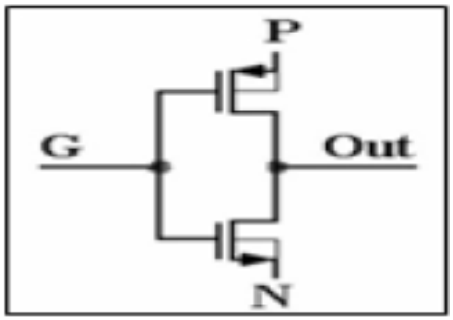


Fig.8 Basic Gate Diffusion Input cell

The GDI cell with four ports is totally a new Multifunctionaldevice, which can achieve six functions with just different combinations of inputs G, P and N.TABLE 1. shows that simple configuration changes in the inputs P, G and N of the basic GDI cell can lead us to totally different Boolean functions at the output port Out . Most of these functions are complex (usually consists of 6-12 transistors) in CMOS, while very simple (only 2 transistors per function) in the GDI design methodology. Meanwhile, multiple-input gates can be implemented by combining several GDI cells.

| Sr. No. | Input | | | Output | Function |
|---|---|---|---|---|---|
| | P | G | N | | |
| 1 | B | A | 0 | $A.\overline{B}$ | F1 |
| 2 | 1 | A | B | $A \overline{+} B$ | F2 |
| 3 | B | A | 1 | A + B | OR |
| 4 | 0 | A | B | A.B | AND |
| 5 | B | A | C | $A.\overline{B} + A.C$ | MUX |
| 6 | 1 | A | 0 | $A\ \overline{\ }$ | NOT |

TABLE1 Functions of the basic GDI cell

The XOR gate made with the help of GDI cell is a application of the GDI technique. As it can be seen in Fig. 9, the XOR made using GDI technique requires only four transistors. Obviously, the proposed GDI XOR gate use less transistors compared with the conventional CMOS XOR.

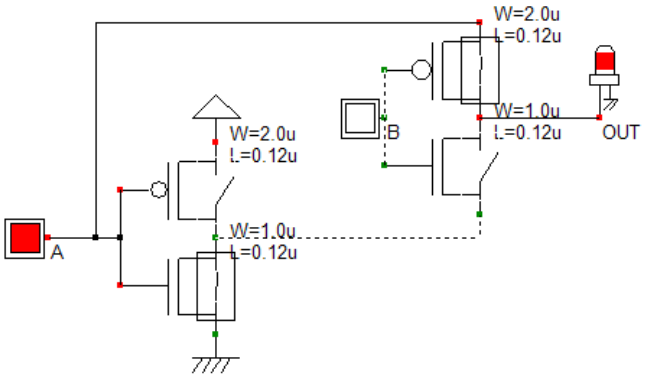


Fig.9 XOR using GDI cell

Now using this same XOR circuit many other more complex circuit can be implemented such as a Full Adder which will require very less transistor than its counterpart. A such 1-bit full adder is shown in fig.10

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

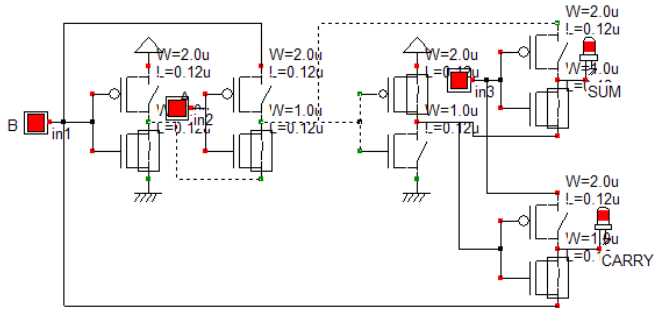


Fig.10 Full adder using XOR-GDI gate

| Function | Power | |
|---|---|---|
| | GDI | CMOS |
| OR | 0.329uw | 4.914uw |
| XOR | 1.721uw | 19.89uw |
| FULLADDER | 5.843uw | 20.48uw |

## TABLE 2 Comparision of Power of GDI and Static CMOS

Simulation result and layout of some of the operation using GDI technique are given below using MICROWIND 2.6K tool.

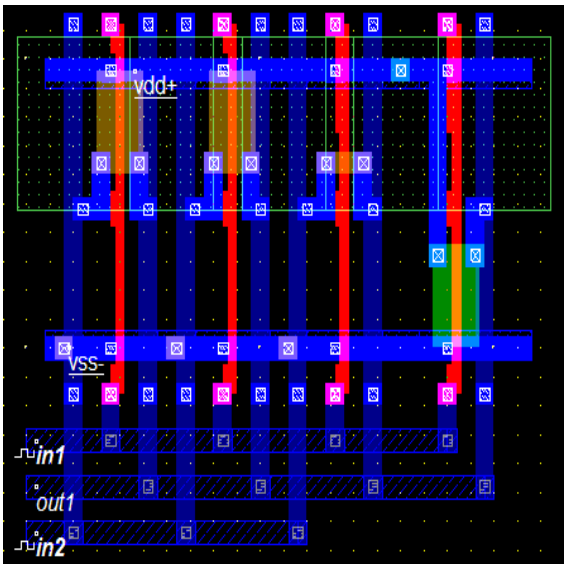


Fig.11a Layout of AND gate using GDI technique.

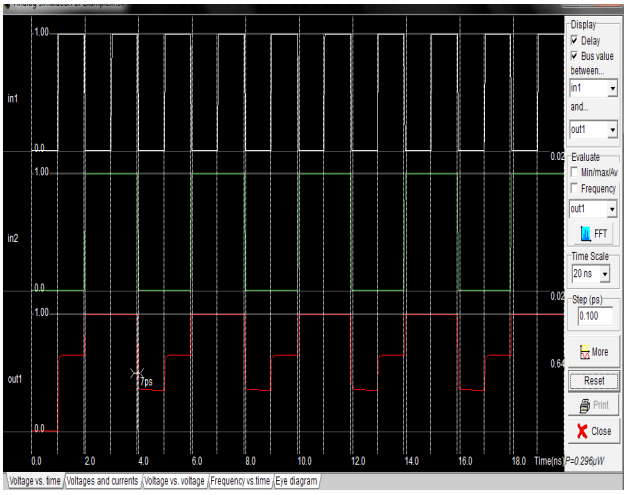


Fig.11b Simulation of AND gate using GDI technique.

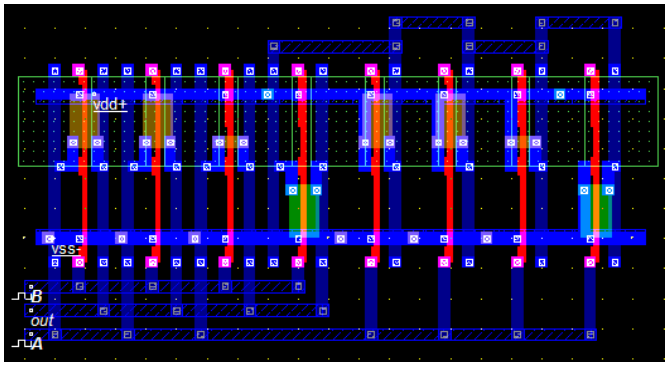


Fig.12a Layout of XOR gate using GDI technique

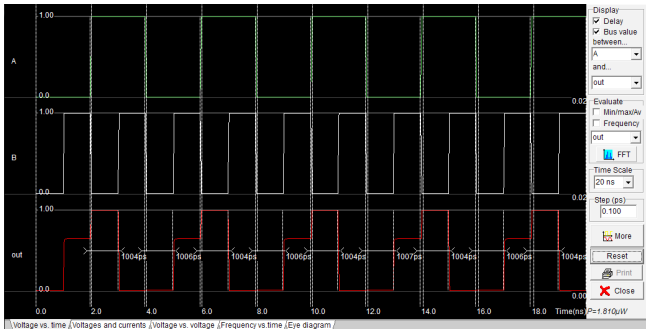


Fig.12 Simulation of XOR gate using GDI technique.

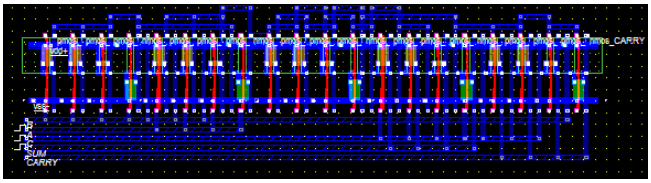


Fig.13a layout of Full adder using XOR-GDI gate

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

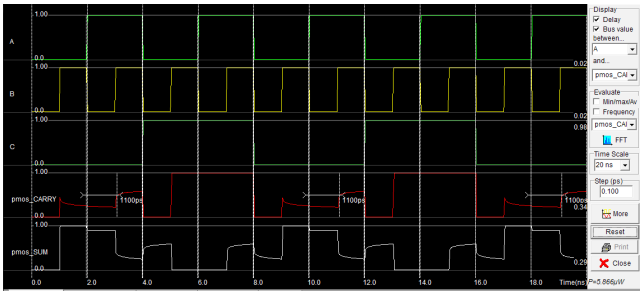

Fig.13b simulation of Full adder using XOR-GDI gate

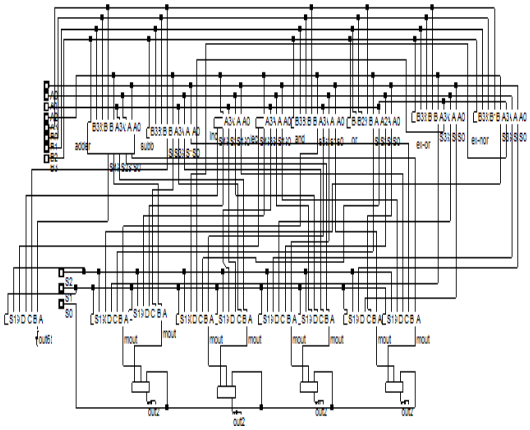

Fig.14a Schematic of 4-bit ALU using GDI technique

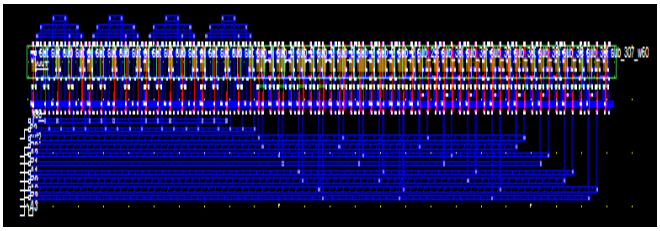

Fig.14b Layout of 4-bit ALU using GDI technique

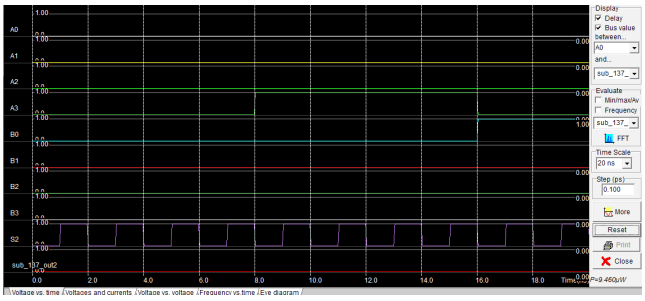

Fig.14c Simulation of 4-bit ALU using GDI technique

## IV. RESULT:

As the number of transistor is reduced in the GDI technique ALU it is obvious that its area is optimized. Apart from this optimized area of ALU the other evident advantage we get is speed. Apparently as the number of transistor used is reduced the operating time is also reduced and operation are done in less time. So our new ALU is also fast in operation as compare to its counterpart.Also due to some attractive features which allow improvements in design complexity, transistor counts, static power dissipation and logic level swing, research on GDI is becoming feverish in VLSI area.

However, the GDI scheme suffers the defect of special CMOS process, specifically, it requires twin well CMOS or silicon on insulator (SOI) process, which are more expensive than the standard p-wellCMOS process [3]. Similarly with certain modification the subtractor circuit can be made which again will use less transistor than its CMOS counterpart. Same is the case with each gate's and other component's circuit. Every design made with this GDI technique have considerably reduced the no. of transistor. The following table compares the no. of transistor used in Complementary Logic Design and the GDI design technique.

| Sr. No. | Components | No. of transistor required | |
|---|---|---|---|
| | | CMOS | GDI |
| 1 | Adder | 28 | 10 |
| 2 | Substractor | 26 | 10 |
| 3 | AND2 | 6 | 2 |
| 4 | OR2 | 6 | 2 |
| 5 | XOR | 16 | 4 |
| 6 | XNOR | 16 | 4 |
| 7 | 2:1 MUX | 4 | 2 |

**TABLE 3 Comparision of Transistors count used by CMOS and GDI technique.**

## CONCLUSION:

In this paper, the traditional CMOS technique for the designing of ALU is discussed first. A area optimizing technique is introduced and the components with this technique are implemented. Later the comparison between the number of transistor used in old and GDI design of ALU is done. And in the demonstration it is shows that this GDI design evidently reduces the number of transistor and hence optimize the area of ALU as well increase its working speed.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

## References:

[1] VLSI IMPLEMENTATION OF AREA OPTIMIZED ALU USING GDI TECHNIQUE1.AKSHAY DHENGE, 2.ABHILASH KAPSE, 3.SANDIP KAKDE Proceedings of International Conference on Research in Electrical, Electronics & Mechanical Engineering, Dehradun, 26th April-2014, ISBN: 978-93-84209-11-7

[2]Shrivastava, A.; Kannan, D.; Bhardwaj, S. Vrudhula, Reducing functional unit power consumption and its variation using leakage sensors, IEEE transactions on verylarge scale integration (VLSI) systems, vol. 18, no. 6,pp.988-997, June 2010

[3] Sanu K. Mathew, Mark A. Anders, and Ram K.Krishnamurthy, High-Performance Energy-Efficient Dual-Supply ALU Design, High-Performance Energy EfficientMicroprocessor Design, Springer, pp.171-187, 2006.

[4] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan,Zhangming Zhu, Yintang Yang, "Novel Low Power FullAdder Cells in 180nm CMOS Technology", ICIEA 2009,978-1-4244-2800-7/09/$25.00 ©2009 IEEE

[5] M.Kamaraju, K.Lal Kishore, A.V.N.Tilak, "Power Optimized ALU for Efficient Datapath", International ournal of Computer Applications (0975 – 8887), Volume11– No.11, December 2010(IJISME), ISSN: 2319-6386, Volume-1, Issue-8, July 2013.

[6] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner, "Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 5, October 2002

[7] Hamid Reza Naghizadeh, Mohammad Sarvghad-Moghadam, Saber Izadpanah Tous and Abbas Golmakani,"Design of Two High Performance 1-Bit CMOS Full Adder Cells", International Journal of Computing and Digital Systems 2, No. 1, 47-52 (2013)