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Performance Analysis of Current Starved Voltage Controlled Oscillator

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ABSTRACT:

This paper deals with the design and implementation of optimal and robust Current Starved Voltage Controlled Oscillators (CSVCO) using CNFET technology. CNFET is very promising and superior technology for application to circuits like CSVCO. CSVCO using conventional CMOS, hybrid CMOS-CNFET and pure CNFET CSVCO circuit are simulated in Hspice. The parameters are estimated from simulation results i.e. power consumption, Oscillation Frequency and linearity of CSVCO circuit. Results obtained to compare performance of conventional CMOS, hybrid CMOS-CNFET and pure CNFET CSVCO circuit. It is decided how this CNFET devices are efficient compared to others.

Keywords:

CNFET, CMOS Technology, HSPICE, Current Starved VCO.

I.INTRODUCTION:

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits. In a wireless system the quality of the communication link is determined in large part by the characteristics of the VCO and in today's wireless communication systems greater frequency range is required by the VCOs. Traditionally, VCOs using CMOS technology have been used for low frequency applications, but this use of some hybrid and nano devices have allowed better oscillations frequencies in the gigahertz range [3].

This is made possible with the use of CNFET technology. VCO can be built using many circuit techniques [8]. In this paper designing of current starved VCO using conventional CMOS, Hybrid CNFET-CMOS and pure CNFET is done. An oscillator is an electronic device that used for the aim of generating a signal or waveform. Applications vary from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillators, oscillators' topologies and performance parameters. With respect to digital phones that use these circuits, low power consumption, improved oscillations frequencies, small size are important design factors [3].

II.DESIGN METHODOLOGY AND EXPERIMENTAL SETUP:

Circuit of Pure CMOS, hybrid CMOS-CNFET and pure CNFET are designed in netlist of HSPICE. HSPICE netlist uses a powerful program used in IC and board level design to check integrity of circuit designs and to predict circuit behaviour [4]. An experimental setup contains PC/Laptop with Operating System Windows XP/7 with Software Platform HSPICE (Version Z-2007.03). Output File: Oscillations are observed on Avanwave while Parameters of simulated circuit observed on Output listing file (.lis).

III.CURRENT STARVED VCO:

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. This current starved VCO is designed using ring oscillator and its operation is also similar to that.

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From the schematic circuit shown in the Figure 1, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of all lower NMOS transistors. Consider Figure 1 shows the simplified schematic of one stage of the VCO [6].

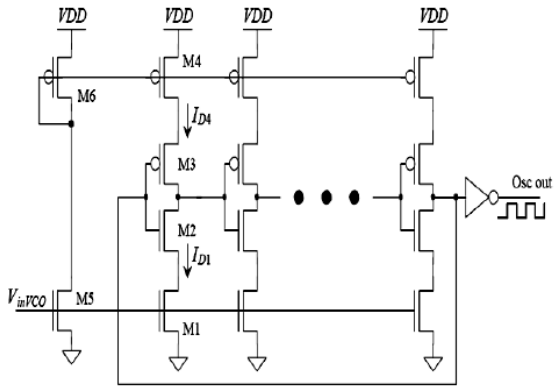

Figure 1: Current Starved VCO [6].

IV.PURE CMOS DESIGN:

To make the current in a MOSFET linearly related to the VCO's input voltage, consider the circuit seen in Figure 2. The width of M5R is made wide so that its VGS is always (independent of VinVCo) approximately VTHN. The current in M6R is mirrored over to M6 and M5 to control the current used in the current-starved VCO. Linearizing scheme is used with R of 10k and a wide device (M5R) with a size of 100/1.

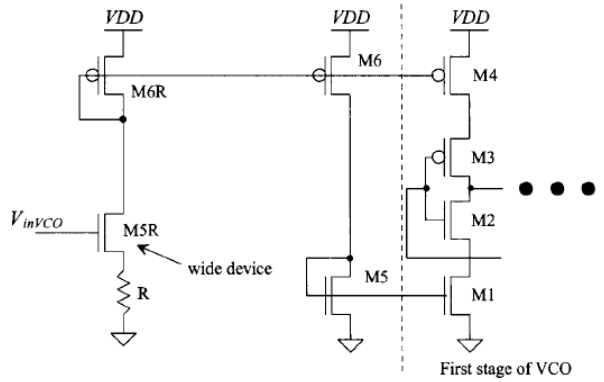

Figure 2: Linearizing the current in a current-starved VCO [6].

In the above circuit all the devices used are of CMOS including all the stages of VCO and output inverter stage. On simulation of HSPICE, parameters obtained are plotted on graph figure 3, 4, 5 [6].

V. HYBRID CNFET-CMOS CIRCUIT DESIGN:

A hybrid CNFET-CMOS circuit has been designed using same circuit (Figure 2) by replacing nMOS devices by nCNFET devices. The designed circuit called as nCNFET CSVCO. On simulation of HSPICE, parameters obtained for both the circuit are plotted on graph figure 3, 4, 5.

VI.PURE CNFET DESIGN:

A pure CNFET circuit has been designed using same circuit (Figure 2) by replacing all the CMOS devise by CNFET devices. On simulation of HSPICE, parameters obtained are plotted on graph figure 3, 4, 5.

VII.SIMULATION RESULTS:

A.Simulated results performance parameters for Conventional CMOS CSVCO.

Vin (V)	Average Power (µw)	Oscillations Frequency (MHz)
0.3	0.249	0.645
0.4	0.361	0.975
0.5	0.476	0.0127
0.6	0.592	0.0156
0.7	0.710	0.0185
0.8	0.825	0.0215
0.9	0.923	0.0239

Table 1: Parameters of Conventional CMOS CSVCO.

B.Simulated results performance parameters for Hybrid CNFET-CMOS CSVCO.

i.nCNFET CSVCO:

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Vin (V)	Average Power (µw)	Oscillations Frequency (MHz)
0.3	0.194	8.33
0.4	0.304	0.136
0.5	0.401	0.189
0.6	0.498	0.244
0.7	0.596	0.296
0.8	0.693	0.349
0.9	0.775	0.392

Table 2: Parameters of nCNFET CSVCO.

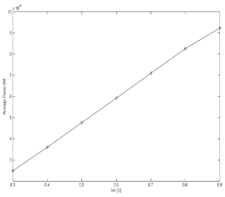
C.Simulated results performance parameters for Pure CNFET CSVCO.

Vin (V)	Average Power (µw)	Oscillations Frequency (MHz)
0.3	0.102	5.89
0.4	0.158	7.59
0.5	0.197	0.443
0.6	0.259	0.922
0.7	0.324	0.0130
0.8	0.361	0.0149
0.9	0.372	0.0150

Table 4: Parameters of Pure CNFET CSVCO.

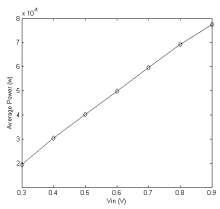
VIII.COMPARISON OF SIMULATION GRAPHS

A.Pure CMOS CSVCO



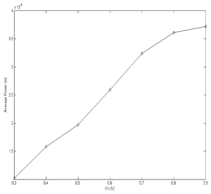
(a)

B. nCNFET CSVCO



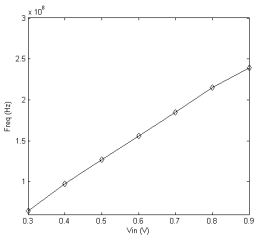
(d)

C. Pure CNFET CSVCO.

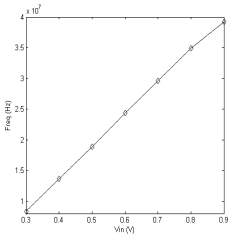


(g)

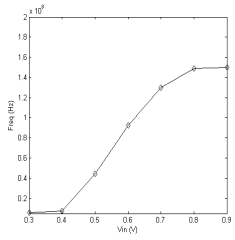
Figure 3: Average Power Vs Vin.



(b)

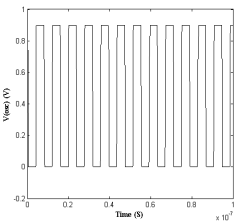


(e)



(h)

Figure 4: Oscillations Frequencies Vs Vin.



(c)

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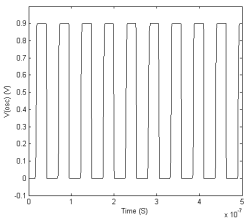
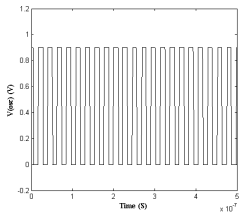


(f)



(i)

Figure 5: Output Oscillations.

IX.CONCLUSION:

This paper compares the performance of CSVCO's designed using conventional CMOS, Hybrid CNFET-CMOS and pure CNFET. A current starved VCO has been designed and simulated with HSPICE and the qualitative evaluation has done. Our measurement results shows graphs with considerably reduced power consumption and improved oscillations frequency also the effect of change in number of tubes of the CNFET devices i.e. enhancement in drive current and hence improved oscillations frequencies. The techniques proposed in this paper can also be applied to other low voltage and low power applications like analog and RF circuits to improve their performance.

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