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Design of Level Shifter Circuit Using Double Tail Comparator

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Abstract:

The proposed level shifter circuit capable with a wide input voltage range. The circuit is based on a Double-Tail comparator, and has a distinctive feature in current generation scheme by monitoring input and output logic levels. The proposed circuit can convert low voltage input digital signals into high voltage output digital signals. The circuit achieves low power operation because it dissipates operating current only when the input signals change.

Dynamic Comparator is a one of the basic building block. Clocked comparators are called as the dynamic comparator. The accuracy of comparators which is defined by its power consumption and speed. Conventional dynamic latched comparators suffer from low supply voltages especially when threshold voltage of the devices is not scaled at the same pace as the supply voltages of the modern CMOS process.

A new double tail comparator is designed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Without complicating the design and adding the few transistors to the conventional circuit we will speed up the comparison. The positive feedback during the regeneration results in remarkably reduced delay time.

I. INTRODUCTION:

COMPARATOR is one of the fundamental building blocks. High-speed, low power with small chip area designs are required for fastest operated circuit designs.

Due to low supply voltages, designing of the high speed comparators are very challenging. The structure of double-tail dynamic comparator first proposed based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure, a new dynamic comparator is presented, which does require boosted voltage or stacking of too many transistors.

Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator. By using this circuit we developed the level shifter circuit. The rest of this paper is organized as follows. Section II investigates the operation of the conventional comparators and the pros and cons of each structure is discussed. Delay analysis is also presented. The proposed comparator is presented in Section III. Simulation results are addressed in Section IV, followed by conclusions in Section V.

II. CLOCKED REGENERATIVE COMPARATORS:

Clocked regenerative comparators are nothing but conventional comparators. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset, random decision errors, and kick-back noise.

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In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

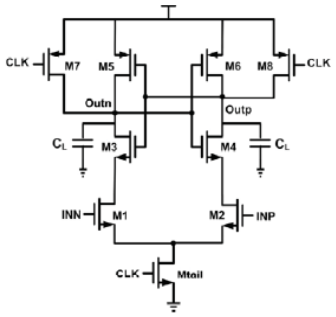

Fig.1: Schematic diagram of the Conventional dynamic comparator.

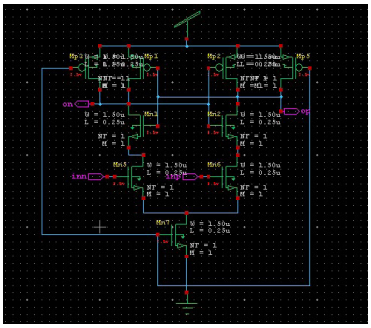

Fig:2.a: Conventional Comparator circuit design in tanner tool.

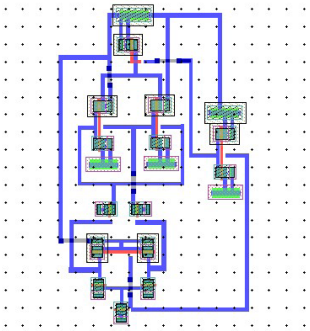

Fig.2.b: Lay out for fig2.a.

A. Conventional Dynamic Comparator:

The schematic diagram of the conventional dynamic comparator is shown in fig.1 and having high input impedance, rail-to-rail output swing, and no static power consumption. The operation of the comparator is as follows.

During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6).

Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. The fact is an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield. In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time.

The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances. Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch(the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration

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in the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. Conventional Double-Tail Dynamic Comparator:

A conventional double-tail comparator is shown in Fig3. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset.

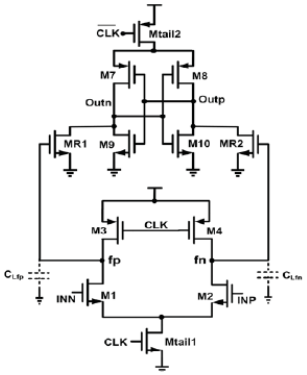


Fig.3: Conventional Double-Tail Comparator.

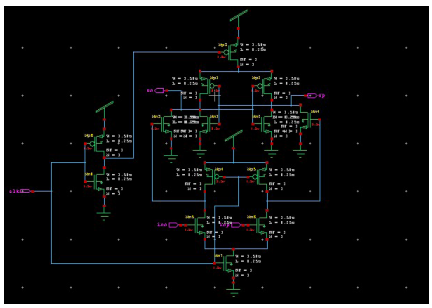
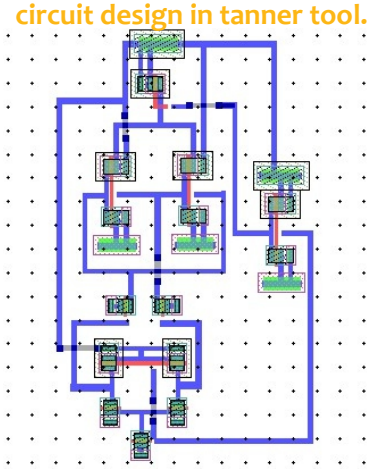


Fig3.a: Conventional Double-Tail Dynamic Comparator circuit design in tanner tool.



The operation of this comparator is as follows. During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage ΔVfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes ΔVfn(p) to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, to and tlatch.

The delay to represents the capacitive charging of the load CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus to is obtainedAfter the first n-channel transistor of the latch turns on (for , M9), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD). The regeneration time (tlatch) is achieved.

1) The voltage difference at the first stage outputs (ΔVfn/fp) at time to has a profound effect on latch initial differential output voltage (ΔVo) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR:

Fig. 4 demonstrates the schematic diagram of the latched dynamic double-tail comparator.

ISSN No: 2348-4845
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Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the latched comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

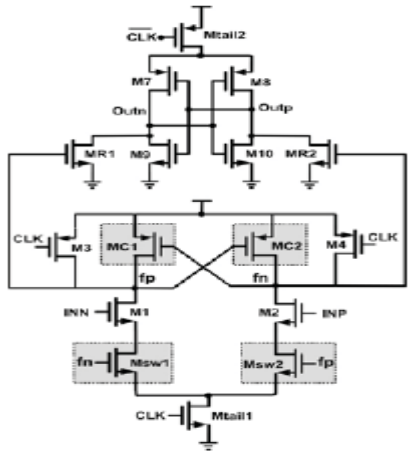

Fig. 4.a. Schematic diagram of the Latched Dynamic comparator

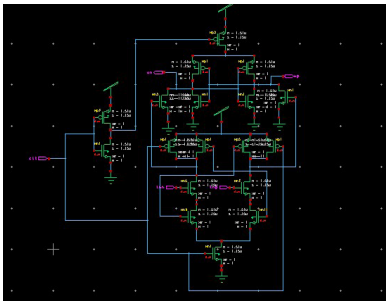

Fig.4.b.: Latched comparator in Tanner Tool

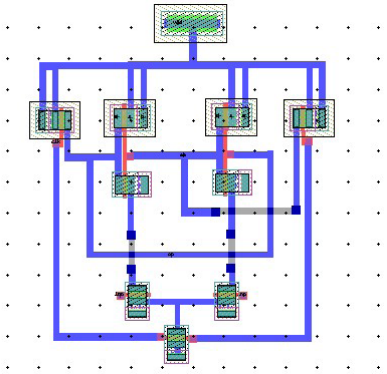

Fig.5.c: Layout for fig.5.b.

A. Operation of the Proposed Comparator using Switching Transistor

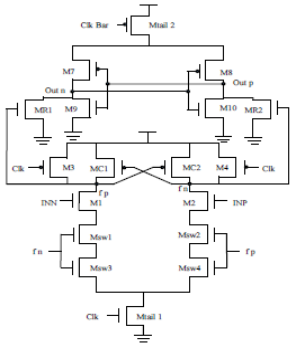

Fig: 6.: Proposed Double-Tail Comparator

The operation of the proposed comparator is as follows in fig.6. During reset phase, clk = 0, tail transistors are off to avoiding static power, M3 and M4 pulls both fn and fp nodes to Vdd, hence transistor MC1 and MC2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision making phase clk = Vdd, both the tail transistors are on, transistors M3 and M4 are turn off. At the beginning of this phase, the control transistors are still off, since fn and fp are about Vdd. Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, since M2 provides more current than M1.

As long as fn continues falling, the corresponding pMOS control transistor ,MC1 in this case, starts to turn on, pulling fp node back to the Vdd, so another control transistor (MC2) remains off, allowing fn to be discharged completely.In other words, unlike conventional double tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor turns on, pulling the other node fp back to the Vdd.

Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors turns on, a current from Vdd is drawn to the ground via input and tail transistor, resulting in static power consumption. To overcome this issue, four nMOS switches are used below the input transistors such as Msw1, Msw2,Msw3 and Msw4.

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B. Delay Analysis :

The dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (ΔVo) at the beginning of the regeneration (t = to); and second, it enhances the effective transconductance of the latch.

1)Effect of Enhancing ΔVo: to is a time after which latch regeneration starts. In other words, to is considered to be the time it takes until the first nMOS transistor of the back to back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. The latch output voltage difference at time to, (ΔVo) has a considerable impact on the latch regeneration time, such that bigger ΔVo results in less regeneration time.

2) Effect of Enhancing Latch Effective Transconductance: In conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. The fact that one of the first stage output nodes (fn/fp) will charge up back to the Vdd at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of Vth/Vdd, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator.

3) Reducing the Energy per Comparison: In conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the Vdd. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required.

C. Level Shifter using Double-Tail Comparator:

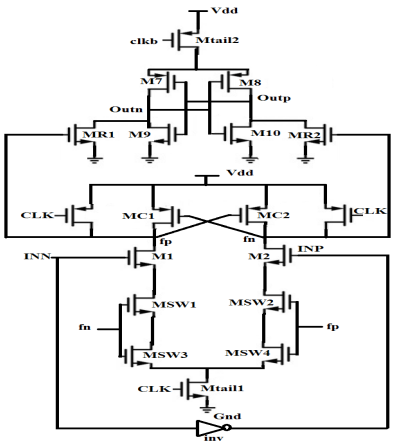

Fig.7: Level shifter using double-tail comparator

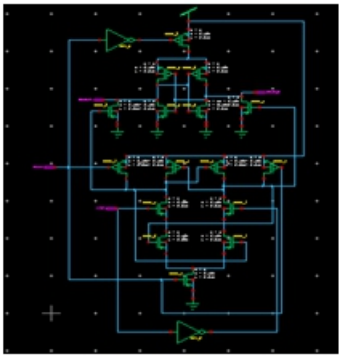

Fig.7.a: Level shifter in tanner tool

Operation of the Level shifter circuit:

The Comparator has few applications. In which we designed Level shifter. Basically, scaling down of the technology and the trend of using small portable devices necessitates the much attention on low power design of CMOS circuits/systems and driven numerous research efforts to a

ddress various kinds of power reduction techniques. One of the most common techniques to reduce the leakage and dynamic power is to use multiple power supplies in a same system. In multi power domain systems different blocks operate with different power supplies. In order to minimize the crow bar current, voltage level shifters are used among the blocks with different power supply domains. Mostly the level shifters are used as a constant Vdd supplier. Here we used voltage level shifters. We considered VL as low input voltage and VH as the high output voltage

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For any comparator circuit one input is the reference voltage and another input is the applied voltage. For level shifter application we considered only one input node. That means from the proposed double-tail comparator INN is considered as reference input and INP is considered as applied input. INN is connected to INP with inverter. Here INN (VL) is only the input. The input voltage VL is given to the INN and output taken from Outn (VH). If VL =0.45v then VH=1.05V. Here VH is the applied Vdd. Always VL>VT.This simulation will be done in 45nm technology and implemented using Tanner 13 version. Applied frequency is 0.6GHz.

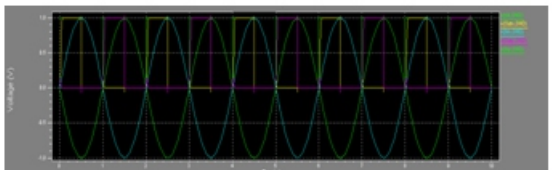

Fig.: Simulation for fig 5.a.

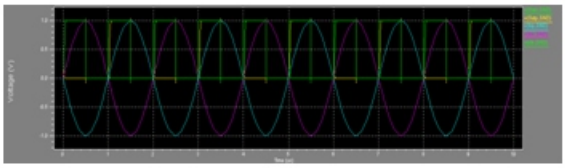

Fig: Simulation for fig 6.

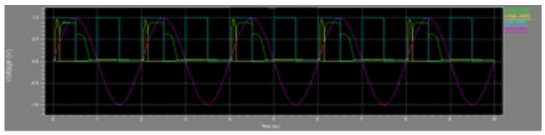

Fig: Simulation for fig 7.

Conclusion:

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and implemented in application. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.045-µm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

Comparator	Power	Delay
Double-Tail Comparator	0.49nW	66ns
Latched Double Tail Comparator	0.96µW	7ns
Proposed Double Tail Comparator	0.18µW	0.9ns
Level Shifter	4.06mW	1.2ns

References:

1. A Level Shifter Circuit Design by Using Input/Output Voltage Monitoring Technique for Ultra-Low Voltage Digital CMOS LSIs-

Yuji Osaki, Tetsuya Hirose, Nobutaka Kuroki, and Masahiro Numa.

2. Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator- Samaneh Babayan-Mashhadi, Student Member, IEEE, and Reza Lotfi, Member, IEEE

3. Low Power Level-Up Shifter for Reduction of Static Power Dissipation in CMOS Technology -Pawan Kumar, Munish Verma, Vijay Lamba

4. A High speed, Low Voltage to High Voltage Level Shifter in Standard 1.2V 0.13µm CMOS Bert Serneels, Michiel Steyaert and Wim Dehaene

5. Voltage up level shifter with improved performance and reduced power Devesh Dwivedi, Suman Dwivedi, Eswararao Potladhurthi

6. DESIGN OF LOW POWER HIGH SPEED LEVEL SHIFTER G.Srinivasulu1, K. Venkata Ramanaiah2, K. Padma Priya3

7. D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta,"A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers,Feb. 2007, pp. 314–315.

8. B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.

9. A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.