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Single Ended SRAM Array Design Using NBTI Technique

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Abstract:

SRAM is a major source to store the data for a long time. The major reason for this power leakage could be a bitline. This leakage should be reduced for better performance of the circuit and it can avoid the Chip damage. The manufacturing by using this circuit contains poor performance and high leakage. In this paper power is reduced, by designing the circuit using single bitline. In single bitline SRAM only one bitline is used for read operation and the voltage level at another bitline node is remains low. So it has high Static Noise Margin compared to the two bitline SRAM.To reduce the extra leakage from this circuit while recycling the Negative Bias Temperature Instability based SRAM circuit is implemented. This reduces the leakage from the SRAM circuit and also increases the read stability in the circuit. Designing and verification of the circuit is done in TANNER EDA.

Keywords:
Adiabatic SRAM, NBTI, Tanner EDA.

I.INTRODUCTION:

Aggressive scaling of semiconductor dimensions with every technology generation has resulted in raise integration density and improved device performance. Leakage current will increase with the scaling of the device dimensions. Raised integration density at the side of raised outflow requirements ultralow-power operation was major one for operating a device.The ability demand for the battery-operated devices like cell phones and laptops is even additional tight. Reducing supply voltage reduces the dynamic power quadratically and leakage power linearly to the primary order. Hence, offer voltage scaling has remained the main focus of low power style.

On chip caches plays a important in speed of processors. In order to increase the speed majorly the frequency of operation is increased which makes caches to operate faster. To achieve higher reliability and longer battery life low power caches are required.

The problems found in the existing SRAM designs are listed below:

- SRAMs consume most of the power of the core Processor Element.
- The leakage in the SRAM circuit is high when compared to the all other processor components.
- As it consumes much power, heat dissipation also occurs.

The total effect of the supply voltage scaling along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write failure, and access-time failure

II PREVIOUS WORKS:

Conventional 6T SRAM design:

There are many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell design. The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only.Read Operation: Before starting of the read operation, the bit lines are charged to VDD. When the word line (WL) is enabled, the bit line which connected to the node of the cell containing ‘0’ is discharged through the NMOS transistor.

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By this we can know which node is containing'0' and which is having '1' in it. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing '1' means it's connected to the node containing '1' and vice versa.

Write Operation:

For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar ((BL)). When the word line (WL) is enabled the data is written into respective node.

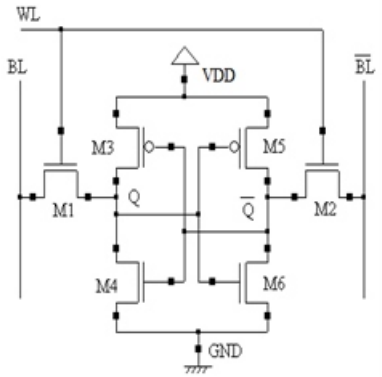

Fig.1. Conventional 6T SRAM

But the conventional 6T SRAM have stability limitations at low supply voltages.

Existing SRAM Cell:

A conventional 6T SRAM Cell uses a two bit line precharge for the Read operation but in the proposed SRAM cell ,a single bit line SRAM reading is introduced. The problem is that the low-voltage node of an FF increases from 0 V. In contrast, a single-BL SRAM uses only one BL for reading. When V1 = 1 and V2 = 0, V2 is not connected to the precharged BL; so it remains at a low level.

Therefore, a single-BL SRAM has a larger SNM than one with two BLsTo examine the effect of adiabatically charging, it is assumed that the capacitance of a BL is small and that the voltage of a BL decreases from the Precharge voltage to 0 because the initial conditions are V1 = 0 and V2 = 1.

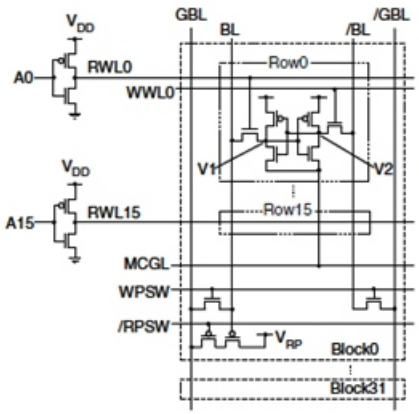

Fig.2. Adiabatic SRAM Cell

Operation:

The proposed SRAM Cell consists of two bit line writing and Single bit line reading. The BL is connected to the global bit line (GBL) via the writing port and the reading port. The writing port is composed of an nMOS transistor. The reading port is composed of two pMOS transistors. The writing and reading ports are activated by the writing port switch signal (WPSW) and the reading port switch signal (RPSW), respectively.

The memory cell ground line (MCGL) is shared in 16 words (row0- row15). The difference from the circuit is that only the read word line (RWL) goes high during reading, while the RWL and the write word line (WWL) go high during writing. The GBL and BL are set to the precharged voltage (VPC) using a precharged circuit.

At reading, RPSW is set to be low. When the flip-flop (FF) node voltage V1 is low, the GBL increases from precharged voltage to reading port power supply voltage (VRP); when V1 is high, GBL is maintained at precharged voltage. With this reading port, we can divide the BL from the GBL and can decrease the BL capacitance. Therefore, the current flow into the cell can be decreased so that electro migration can be reduced.

III PROPOSED SRAM CELL:

Negative bias temperature instability (NBTI) is an important lifetime reliability problem in microprocessors. SRAM based structures within the processor are especially susceptible to NBTI since one of the pMOS devices in the memory cell always has an input of "0".

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Previously proposed recovery techniques for SRAM cells aim to balance the degradation of the two pMOS devices by attempting to keep their inputs at logic "0" exactly 50% of the time. However, one of the devices is always in the negative bias condition at any given time. Negative Bias Temperature Instability (NBTI) is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.

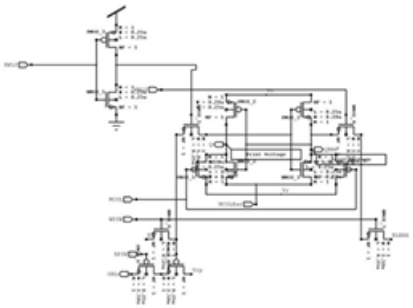

Fig.3. NBTI based SRAM Cell

This NBTI makes PMOS threshold voltage to increase. In order to reduce this NBTI problem of SRAM network here we introduce a recovery boosting technique. In recovery boosting technique SRAM operates in two modes of operation by switching line. One was normal mode which acts like normal SRAM network and another was recovery mode which makes PMOS to off and acts like a recovery transistor.In this paper, a technique called Recovery Boosting is proposed that allows both pMOS devices in the memory cell to be put into the recovery mode by slightly modifying to the design of conventional SRAM cells. The circuit- level design of a physical register file and an issue queue that use such cells through SPICE-level simulations is evaluated.

An architecture-level evaluation of the performance and reliability of using area-neutral designs of these two structures is conducted. Recovery Boosting provides significant improvement in the static noise margins of the register file and issue queue while having very little impact on power consumption and performance is shown.

IV RESULTS:

The figures illustrated below gives the schematics of the conventional 6T SRAM cell, single bit line SRAM cell and the NBTI based SRAM cell.

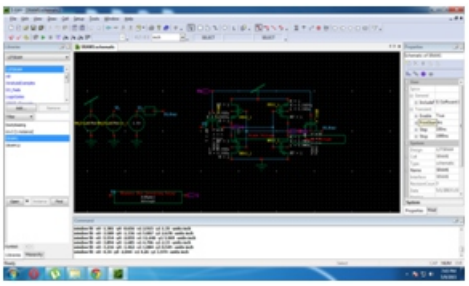

Fig.4. Schematic of the conventional SRAM.

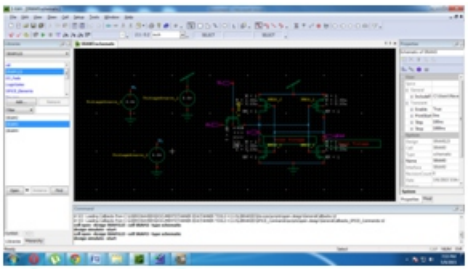

Fig.5. Schematic of single bit line SRAM.

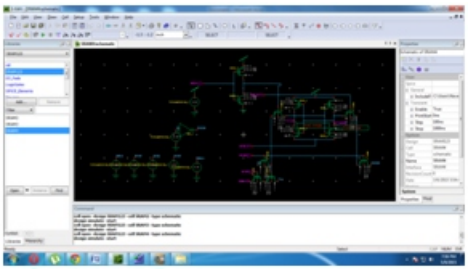

Fig.6. Schematic of NBTI based SRAM.

The memory cells are designed using the TANNER EDA software tool The table (1) gives the comparison of the power dissipation of the existing and the proposed SRAM cells

Table.1. Comparison

CIRCUITS	POWER DISSIPATION
Conventional 6T SRAM Cell	1.372269e-006 watts=1.372µWatts
Single Bit Line SRAM Cell	3.995417e-007 watts=0.399µWatts
NBTI Based SRAM Cell	2.434318e-008 watts = 0.0243µWatts

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Conclusion:

In this paper, NBTI recovery technique which helps in the Vt voltage change SRAM and there is no need of large precharge of bit lines by providing single bit line reading operation.

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