

Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Using Power Gating Techniques



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Abstract:

In this paper, a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF are introduced. The DDFF offers power and area reduction when compared to the conventional flip-flops. The main aim of DDFF-ELM is to reduce pipeline overhead which arises due to the pipeline setup time, propagation delay and clock skew. It gives an area, power and speed efficient method to incorporate complex logic functions into the flip-flop. Power can be reduced by using techniques such as dual stack and sleepy stack in combination of embedded logic which possess a design of low power. This low power design made in 90nm CMOS technology in turn provides an efficient criteria for designing in VLSI. Here the performance improvements indicate that proposed designs are well suited for modern high performance designs.

Index Terms:

Embedded logic, dual stack, sleepy stack, flip-flops, high-speed, leakage power, low-power.

I.INTRODUCTION:

Technology is moving forward from low scale integration to large scale and VLSI. The speed is also increasing from megahertz (MHz) to gigahertz (GHz). With the continuous advancing process of technology and speed of operation, the system requirements are also rising up. In deep-pipelined architectures, pushing the speed additional up demands a lower pipeline overhead.

This overhead is the latency related to the pipeline elements, like the flip-flops and latches. Intensive work has been dedicated to improve the performance of the flip-flops within the past few decades. Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. Among all the types of flip-flops and latches, mostly D Flip-flop latches are used.

They are often called as level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal, which is usually the controlling clock signal. In this paper, different types of flip-flop architectures are compared. They are Power PC 603, Hybrid Latch Flip-flop (HLFF), Semi-dynamic Flip-flop (SDFF), Conditional Data Mapping Flip-flop (CDMFF), and Cross Charge Control Flip-flop (XCFF). In general HLFF and SDFF are classic high performance flip-flops. They are having hybrid architecture, that has combined advantages of both dynamic and static structures.

In addition, SDFF has a capability of incorporating logic very efficiently, because unlike the true single phase latch (TSPC), only one transistor is driven by the data input. This helps in reducing the pipeline overhead. All these flip-flops are aiming at reduction of power, delay and area. The disadvantages in the above flip-flops are reduced in DDFF and DDFF-ELM. A recent paper introduced, in which a flip-flop architecture named Cross Charge Control Flip-flop (XCFF), which has advantages over SDFF and HLFF in terms of both power and speed. There are some disadvantages in XCFF like large hold-time requirement, redundant power dissipation, large power consumption and susceptibility to charge sharing at the internal dynamic nodes.

In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power such as dual stack and sleepy stack.

The remaining paper is divided as follows. Here Section II describes different types of flip-flop architectures and disadvantages of the existing flip-flop architectures and challenges in achieving high performance. In Section III, details the flip-flops with embedded logic. Section IV details the power reduction techniques. In Section V, gives the layout designs of flip-flops. In section VI, it gives the simulation results and finally in section VII, we conclude the proposed flip-flop designs over the existing modern high performance designs.

II. ANALYSIS OF DIFFERENT TYPES OF FLIP-FLOP ARCHITECTURES:

The flip-flop designs are basically grouped as static and dynamic design styles. The master-slave designs include, transmission gate based master-slave flip-flop and the Power PC 603 master-slave latch.

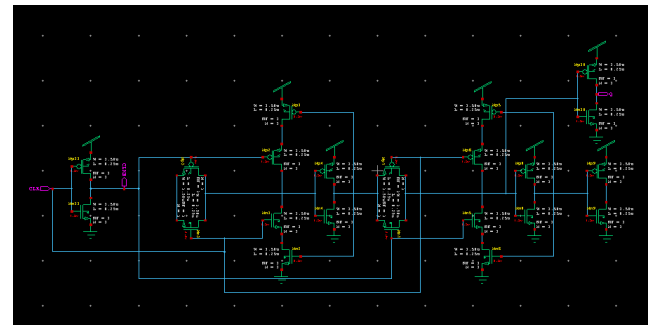


Figure.1. Power PC 603 Flip-Flop.

Here Power PC means Performance Optimization With Enhanced RISC Performance Computing. They dissipate comparatively low power and they are also having low clock-to-output (CLK-Q) delay. In synchronous systems, the latching elements have the delay overhead which is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here, D-Q delay is the combination of CLK-Q delay and the setup-time of the flip-flop. But the static designs lack the low D-Q delay due to their large positive setup-time, and also most of them are susceptible to flow through resulting from CLK overlap.

Power PC 603 (Figure. 1) is one of the most efficient classic static structures. The advantages of Power PC include low-power keeper structure and low latency direct path. The keeper structure in the circuit saves the leakage power. Latency is the time to complete a single instruction from start to finish. The large D-Q delay resulting from the positive setup-time is one of the disadvantages of this design. The large data and CLK node capacitances make the design inferior in performance. Despite among all these cons, static designs still remain as low power solution when the speed is not considered as a primary concern. Abbreviations and Acronyms.

The dynamic flip-flops includes the modern high performance flip-flops. They are divided into purely dynamic designs and pseudo-dynamic structures. The distinctive performance improvements are achieved by having an internal precharge structure and a static output. They are called as the semi-dynamic or hybrid structures because of having a dynamic frontend and a static output. HLFF (Figure.2) and SDFF (Figure.3) fall under this category. Here the CLK overlaps to perform the latching operation.

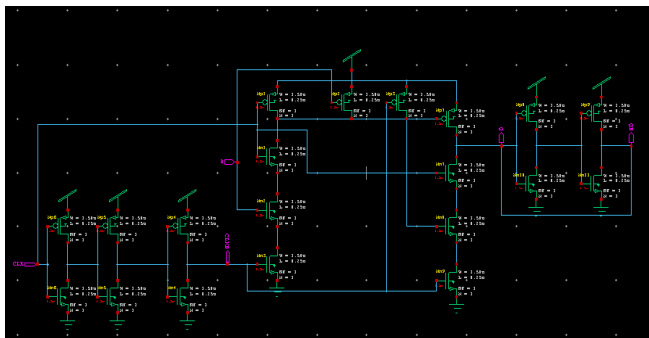


Figure.2. Hybrid Latch Flip-Flop (HLFF).

HLFF is not the fastest but has a lower power consumption when compared to SDFF because of the longer stack of nMOS transistors at the output node makes it slower than SDFF and causes large hold-time requirement. Due to this large hold time requirement, makes the integration of HLFF to complex circuits difficult process. And also HLFF is inefficient in embedding the logic.

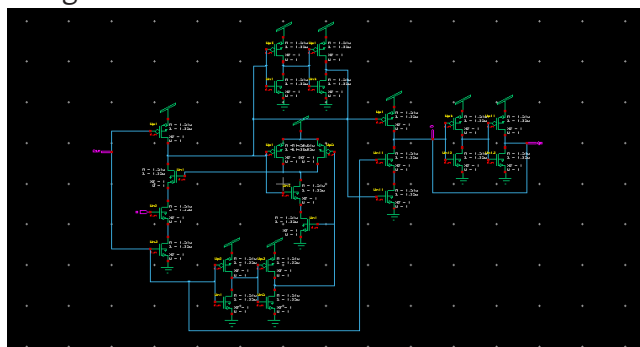


Figure.3. Semi-Dynamic Flip-Flop (SDFF).

SDFF is the fastest classic hybrid structure, but it has high power consumption because of the large CLK load as well as the large precharge capacitance. Its speed is high when compared to that of the HLFF. In conventional semi-dynamic designs, the major sources of power dissipation are the redundant data transitions and large precharge capacitance. The Conditional Data Mapping Flip-Flop (CDMFF) which is present in Figure. 4. is the most efficient attempt to reduce the redundant data transitions in the flip-flop.

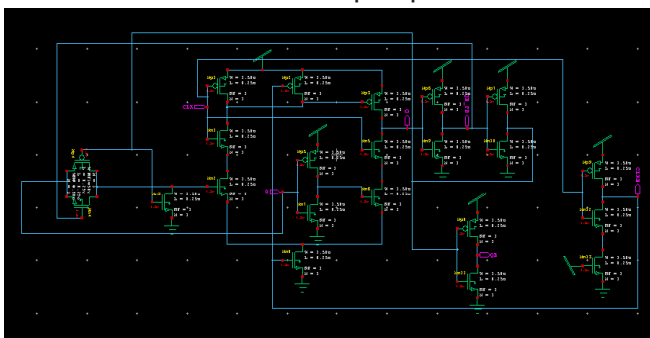


Figure.4. Conditional Data Mapping Flip-Flop (CDMFF).

CDMFF uses an output feedback structure to conditionally feed the data to the flip-flop which reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Considerable speed performance is there, since there are no added transistors at the output node, similar to that of the HLFF. The presence of the conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop. The CDMFF circuit is bulky and cause an increase in power dissipation at higher data activities due to the additional transistors added for the conditional circuitry. In a wide variety of designs, the large precharge capacitance results due both the output pull-up and the pull-down transistors are driven by the precharge node. Most of the capacitance at this precharge node is due to the transistors being driving large output loads. This drawback is considered in the design of XCFF (Figure. 5).

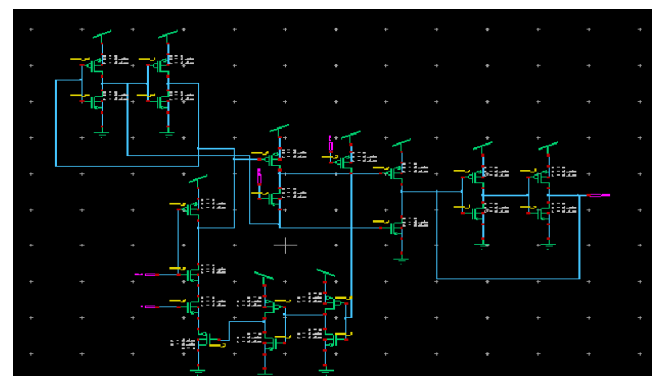


Figure.5. Cross Charge Control Flip-Flop (XCFF).

XCFF reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors. The total power consumption is almost reduced without any degradation in speed because, only one of the two dynamic nodes is switched during one clock cycle. XCFF has a comparatively lower CLK driving load. The major drawback of this design is that, the redundant precharge at node X2 and X1 for data patterns containing more 0s and 1s respectively. Due to the conditional shutoff mechanism, the large hold time requirement appears, and a low to high transition in the CLK when the data is low, causes charge sharing at node X1. This charge sharing can trigger erroneous transition at the output, unless the inverter pair INV1-2 is carefully skewed. The problem of charge sharing becomes very high when complex functions are embedded into the design.

In Dual Dynamic Node Hybrid Flip-Flop (DDFF), there are two nodes in the circuit among which one is purely dynamic and another is pseudo-dynamic. So, called as dual dynamic. As it is having dynamic front end and static output, it is hybrid in nature. So this is the reason for calling this flip-flop as DDFF (Figure. 6).

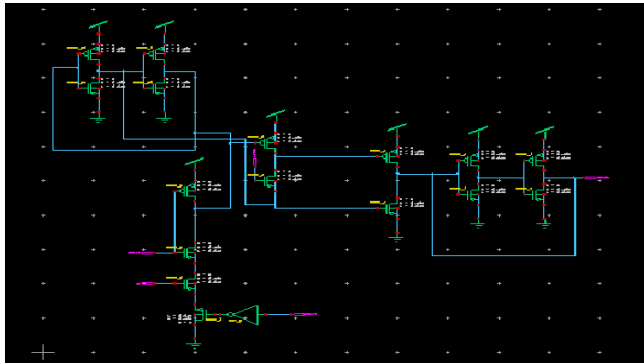


Figure.6. Dual Dynamic Node Hybrid Flip-Flop (DDFF).

In DDFF, node X1 is pseudo-dynamic with a weak inverter acting as a keeper. Node X2 is purely dynamic when compared to XCFF. Here we provide unconditional shutoff mechanism at the frontend where as conditional shutoff mechanism in XCFF. The DDFF operates in two phases:

- 1) The Evaluation Phase, when CLK is high, and
- 2) The Precharge Phase, when CLK is low.

The actual latching occurs in evaluation phase during 1-1 overlap of CLK and CLKB. If D is high (prior to this overlap period), node X1 is discharged from NM0-2, this switches the cross coupled inverter pair INV1-2 which causes node X1B to high and output QB discharge through NM4. For low level, node X1 retained by inverter pair INV1-2, for the rest of evaluation phase no latching occurs. Node X2 is held high throughout evaluation period by pMOS transistor PM1. As CLK falls low, the circuit enters in the precharge phase and node X1 pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If D is low i.e zero (prior to the overlap period), node X1 remains high and node X2 pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically.

The circuit exhibits negative setup time due to the short transparency period defined by the 1-1 overlap of CLK and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low. The minimum time period before the CLK edge is setup time and the minimum time period after the CLK edge is the hold time, where the data should be stable so that proper sampling is possible. Here setup time and hold time depend on the CLK overlap period.

III. FLIP-FLOPS WITH EMBEDDED LOGIC :

As earlier we mentioned, the major advantage of the SDF is the capability to incorporate the complex logic functions efficiently. The efficiency in terms of speed and area can be predicted from the fact that an N-input function can be realized in appositive edge triggered structure using a pull-down network (PDN) consisting of N transistors .

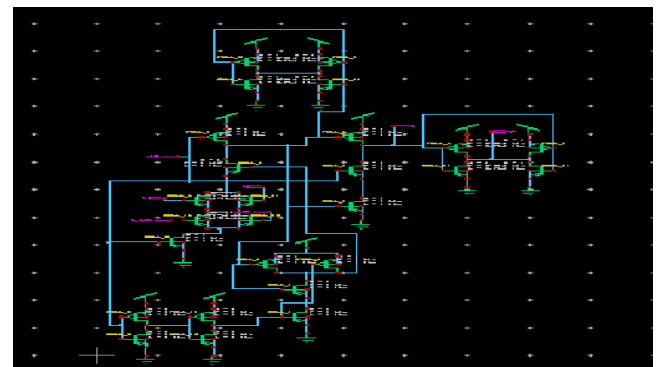


Figure.7. SDF-ELM WITH MUX

This embedded structure offers a very fast and small implementation. Although SDF is capable of offering efficiency in terms of speed and area, it is not a good solution as far as power consumption is concerned. So we consider SDF with embedded logic for comparative purposes. SDF is considered to be the benchmark of comparison; it was also simulated under similar conditions when embedded with the same functions. SDF has a fast non-inverting output and a slow inverting output, whereas the proposed design has a fast inverting output and a slow non-inverting output. In order to have a fair comparison of delay, inverting and non-inverting outputs, respectively were considered for SDF and the proposed design. A two-input multiplexer implementing the function $A.SELA + B.SELB$ were embedded into both the designs by replacing the respective PDN.

Since DDFF-ELM performs the function of a flip-flop when no logic is embedded, its performance as a flip-flop is compared with other flip-flops along with DDFF. The proposed dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Figure. 8.

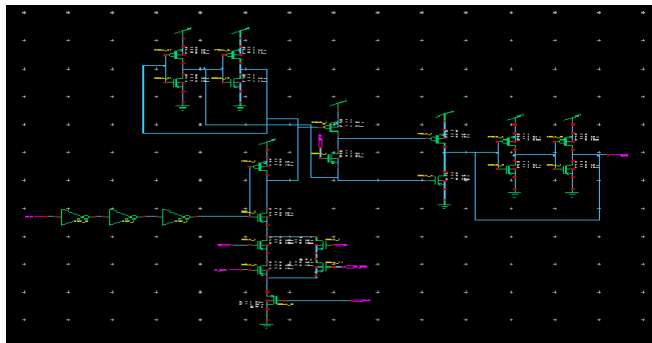


Figure. 8. DDFF_ELM WITH MUX

IV. POWER REDUCTION TECHNIQUES:

The method is dual stack approach, in sleep mode, the sleep transistors are off, i.e. transistor N1 and P1 are off. We do so by making $S=0$ and hence $S'=1$. Now the other 4 transistors P2, P3 and N2, N3 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network and 2 NMOS in the pull-up network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decrease the voltage applied across the main circuit. As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention.

Another advantage is got during off mode if we increase the threshold voltage of N2, N3 and P2, P3. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current. As a result of stacking, P2 and N2 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. $S=1$ and $S'=0$ both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

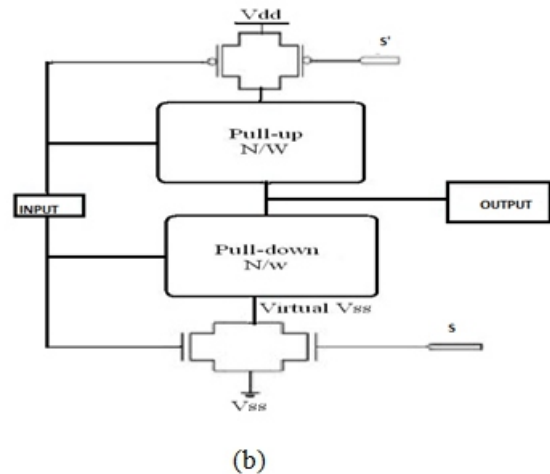
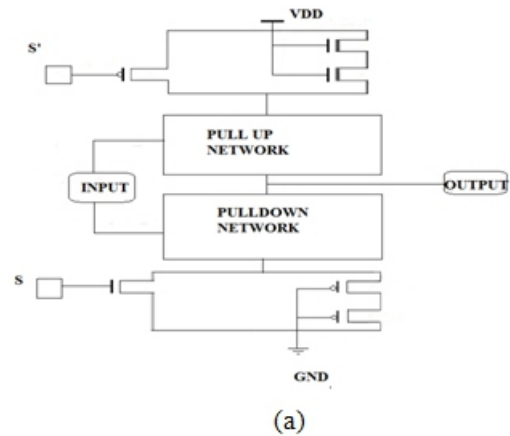


Figure. 9. Power reduction techniques (a) dual stack, (b) sleepy stack

The Sleepy Stack Technique combines the Stack & Sleep techniques. The existing transistors divided into two half size transistors in the Sleepy Stack technique like as Stack technique. Between the divide transistors one of sleep transistor will be added in parallel. Stacked transistors suppress leakage current while saving state & Sleep transistors are turned off during sleep mode. In active mode it reduces delay & resistance of the path because of sleep transistor, sleep transistor is placed in parallel to the one of the stacked transistors.

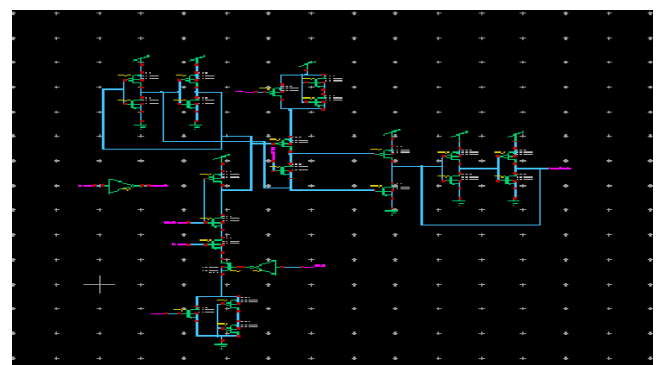


Figure. 10. Schematic for Dual Stack DDFF

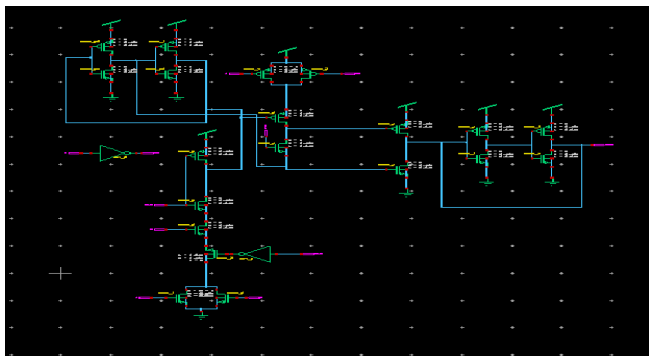
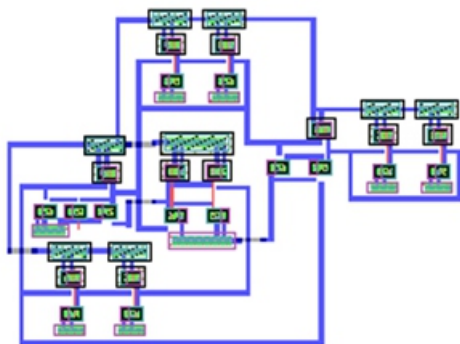


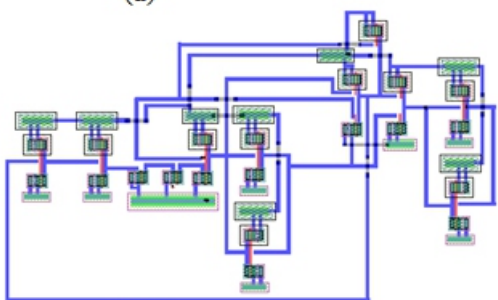
Figure.11 Schematic for Sleepy Stack DDFF

V. Layouts

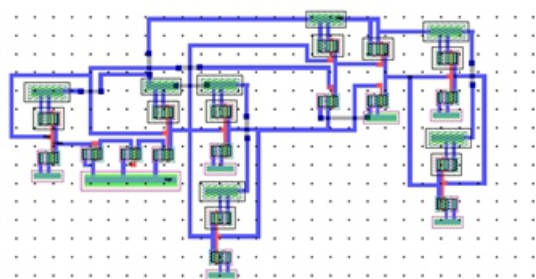
The layout designs of SDDF, XCFF and DDFF are shown in the following figures respectively.



(a)



(b)

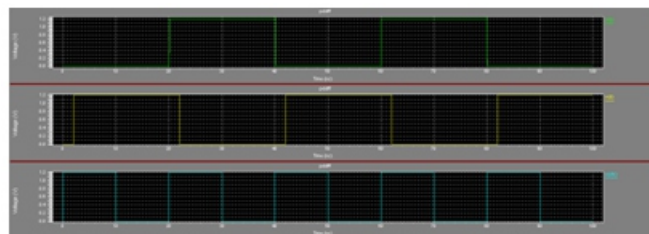


(c)

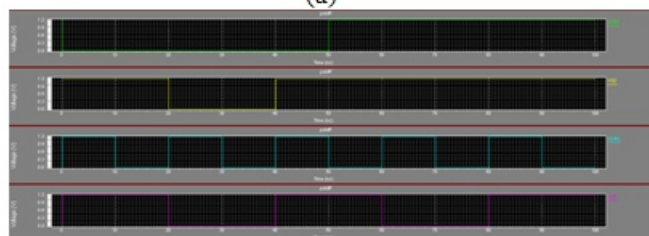
Figure.12. Layout designs for (a) SDDF,(b)XCFF,(c)DDFF.

VI. SIMULATION RESULTS:

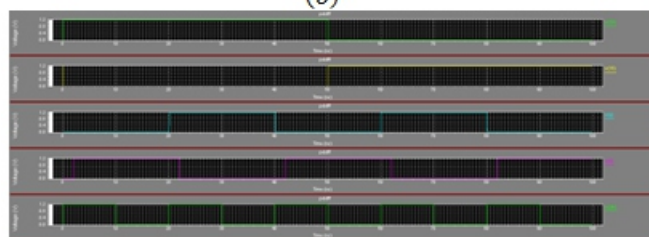
The above discussed regarding the DDFF, DUAL STACK DDFF and SLEEPY STACK DDFF. Here below figures represents the output waveforms in simulation and their contribution towards low power by reducing leakage power reduction.



(a)



(b)



(c)

Figure. 13. Simulation results for (a)DDFF,(b)DUAL STACK DDFF,(c)SLEEPY STACK DDFF.

PERFORMANCE COMPARISON OF VARIOUS FLIP-FLOPS

FLIP_FLO P	Number of transistors	Total power watts(W)	Minimum D-Q (ps)	PDP (fJ)
SDDF	23	2.039862e-006	295	0.601
HLFF	20	2.404293e-006	327.1	0.786
PowerPC 603	22	1.819156e-006	521	0.947
CDMFF	22	6.153578e-005	456.1	0.280
XCFF	21	1.809342e-006	362.0	0.655
DDFF	18	1.794255e-006	356.7	0.640
DDFF-ELM-MUX	25	1.918427e-006	391.2	0.750
DUAL STACK DDFF	24	2.460186e-006	399.2	0.982
SLEEPY STACK DDFF	22	1.394739e-006	313.5	0.437

VII. CONCLUSION :

In this paper, a new low power and low area DDFF and a novel DDFF-ELM were proposed. The proposed DDFF eliminates the redundant power dissipation present in XCFF. Comparison of the proposed flip-flop with the other flip-flops showed that it exhibits lower power dissipation along with area and speed performances. Dual stack and Sleepy stack technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly low power than the existing. So, it can be used for future IC'S for area & power Efficiency.

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