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Modeling Of Three-Phase Drive System With Fault Compensation By Parallel Single-Phase Rectifier

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Abstract: In this paper the three-phase drive is fed by single-phase power supply by using of two 1-ϕ rectifiers which are connected in parallel. The rectifiers are connected to three-phase inverter and to induction motor. By using conventional control topology, it has problem of harmonic distortion, fault characteristics and switching losses. The proposed strategy having two rectifiers is connected in parallel to inverter. The proposed system is having fewer losses than conventional even also having more-switches. In the design of system, it is very important to reduce circulating current. An efficient double-PWM technique is proposed and simulation results are presented for validation.

Index terms: double-PWM technique, parallel rectifier, fault compensation.

I. INTRODUCTION

It is quite common to have only a single-phase power grid in residential, commercial, manufacturing, and mainly in rural areas, while the adjustable speed drives may request a three-phase power grid [1]-[3]. The conventional topology nothing but 1-phase to 3-phase ac-dc-ac conversion is full-bridge type.

There are number of techniques were proposed to supply a 3-phase induction motors from a single-phase supply. Proposed Parallel rectification technique is having advantages of reliability, efficiency and power capability [4], [5]. And it is having Applications of fault tolerance of DFIG, UPS, and performance improvement of APF. The transformer isolation is required for parallel operation of converters; it increases the size and cost of transformer, if not used reducing of circulating currents will get difficult. The conventional full bridge type ac-dc-ac converter is shown in fig.1.

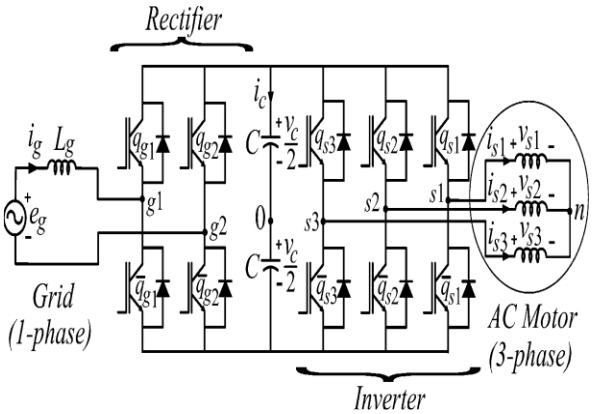

Fig 1: Conventional 1-phase to 3-phase drive system.

In this paper, a single-phase to three-phase drive system composed of two parallel single-phase rectifiers and a three-phase inverter is proposed. The proposed system is conceived to operate where the single-phase utility

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grid is the unique option available. Compared to the conventional topology, the proposed system permits: to reduce the rectifier switch currents; the total harmonic distortion (THD) of the grid current with same switching frequency or the switching frequency with same THD of the grid current; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial investment of the proposed system, due to the increase of number of switches.

DYNAMIC MODELLING OF SYSYEM

Dynamic modeling of system is helps for better understanding of system performance and behavior under dynamic conditions. The proposed system circuit diagram with parallel converter is shown in fig 2.

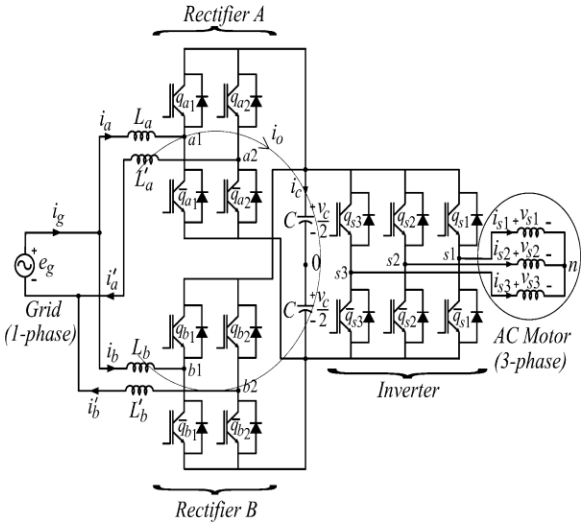

Fig 2: Proposed single-phase to three-phase drive system with parallel converters.

The system is designed of input inductors ($L_a, L'_a, L_b, and\ L'_b$), rectifiers (A and B), DC capacitor links, inverter, and induction machine feeding to grid. Rectifier A and B switches are represented as $q_{a1}, \bar{q}_{a1}, q_{a2}$, and $\bar{q}_{a2}$, and $q_{b1}, \bar{q}_{b1}, q_{b2}$, and $\bar{q}_{b2}$, respectively. The inverter switches are represented as $q_{s1}, \bar{q}_{s1}, q_{s2}$, $\bar{q}_{s2}$, q_{s3}, and $\bar{q}_{s3}$. The switch conduction states are noted as $s_q = 1$, when switch open and $s_q = 0$, when closed.

The voltage equations for the rectifier in proposed system as follows

$$v_{a10} - v_{a20} = e_g - (r_a + l_a p)i_a - (r'_a + l'_a p)i'_a \quad ..1.1$$

$$v_{b10} - v_{b20} = e_g - (r_b + l_b p)i_b - (r'_b + l'_b p)i'_b \quad ..1.2$$

$$v_{a10} - v_{b10} = (r_b + l_b p)i_b - (r_a + l_a p)i_a \quad ..1.3$$

$$v_{a20} - v_{b20} = (r'_a + l'_a p)i'_a - (r'_b + l'_b p)i'_b \quad ..1.4$$

$$i_g = i_a + i_b = i'_a + i'_b \quad ..1.5$$

Where p= d/dt, and r, l are represents the resistance, inductance respectively.

The circulating current i_o

$$i_o = i_a - i'_a = -i_b + i'_b \quad ..1.6$$

Adding equations 1.3 and 1.4 and the above equations are written as

$$v_a = e_g - [r_a + r'_a + (l_a + l'_a)p]i_a + (r'_a + l'_a p)i_o \quad ..1.7$$

$$v_b = e_g - [r_b + r'_b + (l_b + l'_b)p]i_b + (r'_b + l'_b p)i_o \quad ..1.8$$

$$v_o + -[r'_a + r'_b + (l'_a + l'_b)p]i_o - [r_a - r'_a + (l_a - l'_a)p]i_a + [r_b - r'_b + (l_b - l'_b)p]i_b \quad ..1.9$$

Where

$$v_a = v_{a10} - v_{a20} \quad ..1.10$$

$$v_b = v_{b10} - v_{b20} \quad ..1.11$$

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} \quad ..1.12$$

Relations (1.7)–(1.9) and (1.55) constitute the front-end rectifier dynamic model. Therefore, v_a (rectifier A), v_b (rectifier B), and v_o (rectifiers A and B) are used to regulate currents i_a, i_b, and i_o, respectively. Reference currents i_a^* and i_b^* are chosen equal to $i_g^*/2$ and the reference circulating current $i_o^*$is chosen equal to 0.

In order to both facilitate the control and share equally current, voltage, and power between the rectifiers, the four inductors should be equal, i.e., $r'_g = r_a = r'_a = r_b = r'_b$ and $l'_g = l_a = l'_a = l_b = l'_b$. In this case, the model (1.7)–(1.9) can be simplified to the model given by

$$v_a + \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i_a \quad ..1.13$$

$$v_b - \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i_b \quad ..1.14$$

$$v_o = -2(r'_g + l'_g p)i_o \quad ..1.15$$

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In ideal case nothing but all inductors are identical, circulating currents are becomes zero

$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} = 0$ ..1.16

When

$i_o = 0$ ($l_a = l'_a, l_b = l'_b$) the system is modeled as

$v_a = e_g - 2(r'_g + l'_g p)i_a$ ..1.17

$v_b = e_g - 2(r'_g + l'_g p)i_b$ ..1.18

Then, the model of the proposed system becomes similar to that of a system composed of two conventional independent rectifiers.

CONTROL STRATEGY (PWM)

The inverter controlling was done by pulse width modulation (PWM) strategy for three-phase voltage source inverter (VSI) [6]. The PWM strategy for the rectifier will be observed in this section.

The rectifier pole voltages vv_{a10}, v_{a20}, v_{b10} and v_{b20} depends on the conduction states of the power switches, i.e.

$v_{jo} = \frac{(2s_{qj}-1)v_c}{2}, for\ j = \ a1\ to\ b2$ ..2.1

Here v_c is the total dc-link voltage.

The reference voltages can taken as$v_a^*, v_b^*, and\ v_o^*$, they can be written as

$v_a^* = v_{a10}^* - v_{a20}^*$ ..2.2

$v_b^* = v_{b10}^* - v_{b20}^*$ ..2.3

$v_a^* = v_{a10}^* + v_{a20}^* - v_{b10}^* - v_{b20}^*$ ..2.4

The reference pole voltages will be used for finding gate signals. The auxiliary variable $v_x^* = v_{a20}^*$, then system equations can be written as

$v_{a10}^* = v_a^* + v_x^*$ ..2.5

$v_{a20}^* = v_x^*$ ..2.6

$v_{b10}^* = \frac{v_a^*}{2} + \frac{v_b^*}{2} - \frac{v_o^*}{2} + v_x^*$ ..2.7

$v_{b20}^* = \frac{v_a^*}{2} - \frac{v_b^*}{2} - \frac{v_o^*}{2} + v_x^*$ ..2.8

It can be observed that$v_a^*, v_b^*\ and\ v_o^*$, the pole voltages depend onv_o^*. The limit values of the variable v_x^* can be calculated by taking into account the maximum $\frac{v_c^*}{2}$ and minimum $\frac{-v_c^*}{2}$ value of the pole voltages

$v_{xmax}^* = \frac{v_c^*}{2} - v_{max}^*$ ..2.9

$v_{xmin}^* = -\frac{v_c^*}{2} - v_{min}^*$ ..210.

The control block diagram of the system is shown in fig 3. The rectifier circuit of the proposed system has the same objectives of that in Fig. 1, i.e., to control the dc-link voltage and to guarantee the grid power factor close to one. Additionally, the circulating current i_o in the rectifier of the proposed system needs to be controlled.

By using the conventional PI controller the dc-link voltage v_c is adjusted to its reference value v_c^*. To control power factor and harmonics in the grid side, the instantaneous reference current i_g^* must be synchronized with e_g voltage, as given in the voltage-oriented control (VOC) for three-phase system [7]. This is obtained via blocksG_{e-ig}, based on a PLL scheme. The reference currents i_a^* and i_b^* are obtained by making $i_a^* = i_b^* = \frac{i_g^*}{2}$, which means that each rectifier receives half of the grid current.

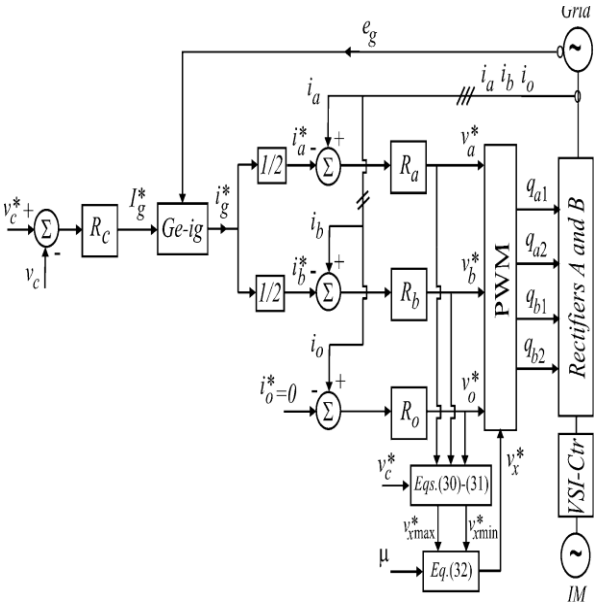

Fig. 3: Control block diagram

The control of the rectifier currents is implemented using the controllers indicated by blocks Ra and Rb. These controllers can be implemented using linear or nonlinear techniques [8]–[10]. In this paper, the current control law is the same as that used in the two sequences synchronous controller described in [11]. These current controllers define the input reference voltages$v_a^*\ and\ v_b^*$.

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RATINGS OF SWITCHES

Assuming same rms voltages at both grid and machine sides, a machine power factor of 0.85 and neglecting the converter losses, currents of the rectifier switches normalized in terms of currents of the inverter switches are 2.55 and 1.27 for the conventional and the proposed single-phase to three-phase converter, respectively. Fig. 4(a) and (b) shows the flow of active power in the conventional and in the proposed single-phase to three-phase converter, respectively. For balanced system (L'_g =L_a = L'_a = L_b =L'_b), voltage v_o is close to zero, so that the dc-link voltage is equal to that required by the conventional system. Since the parallel connection scheme permits to reduce the switch currents and preserve the dc-link voltage, the rating of each power switch in the rectifier side is reduced.

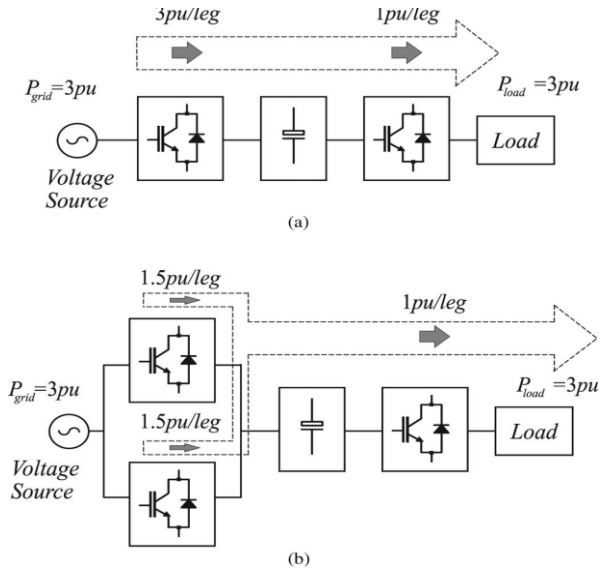

Fig. 4: Flow of active power. (a) Conventional ac–dc–ac single-phase to three-phase converter. (b) Proposed system with two rectifiers.

Input inductors

The PWM with double-carrier strategy reduces the WTHD of the resultant rectifier voltage v_{ab}, as observed in Fig. 4. When the input inductors of the proposed topology (L'_g) are equal to that of the conventional topology (L_g), the reduction of the THD of the grid current is directly indicated in Fig. 5.

The THD of the grid current as a function of μ for different values of ln [the inductances of rectifiers A and B (l'_g) referred to that of the conventional configuration (l_g), i.e, $l_n = l'_g/l_g$]. For ln > 0.4 (lg > 0.4lg) the THD of the grid current of the proposed topology is smaller than that of the conventional topology.

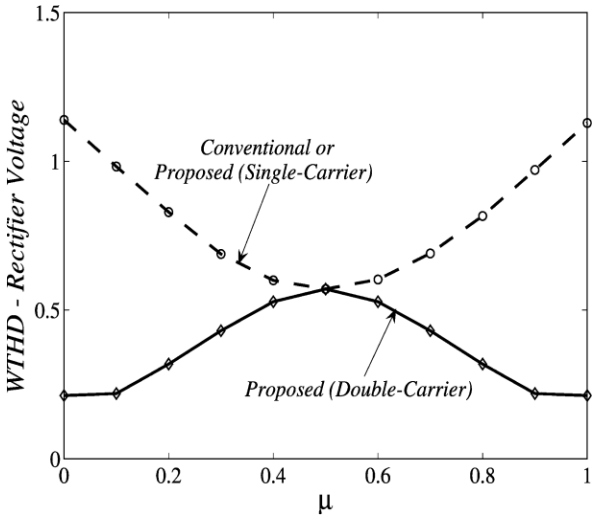

Fig. 5: WTHD of rectifier voltage (v_{ab} for proposed configuration and v_g for standard configuration) as a function of μ.

The harmonic distortion of the rectifier currents (i_a, i'_a, i_b, i'_b andi_o.) is higher than that of the grid current ig. The adequate choice of the PWM strategy permits to operate with minimum harmonic distortion. We have considered the losses as the main concern to define the maximum acceptable harmonic distortion of the rectifier currents.

In any case, the use of additional common-mode inductors is a very efficient manner of reduces the harmonic distortion of these currents. This approach may be also employed in the present case to reduce the total inductance required for an adequate operation of the system.

COMPENSATION OF FAULT

The proposed system presents redundancy of the rectifier converter, which can be useful in fault-tolerant

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systems. The proposed system can provide compensation for open-circuit and short-circuit failures occurring in the rectifier or inverter converter devices.

The fault compensation is achieved by reconfiguring the power converter topology with the help of isolating devices (fast active fuses—F_j, j = 1 . . . 7) and connecting devices (back to- back connected SCRs—t1, t2, t3), as observed in Fig. 6(a) and discussed in [12]–[13]. These devices are used to redefine the post-fault converter topology, which allows continuous operation of the drive after isolation of the faulty power switches in the converter. Fig. 6(b) presents the block diagram of the fault diagnosis system. In this figure, the block fault identification system (FIS) detects and locates the faulty switches, defining the leg to be isolated. This control system is based on the analysis of the pole voltage error.

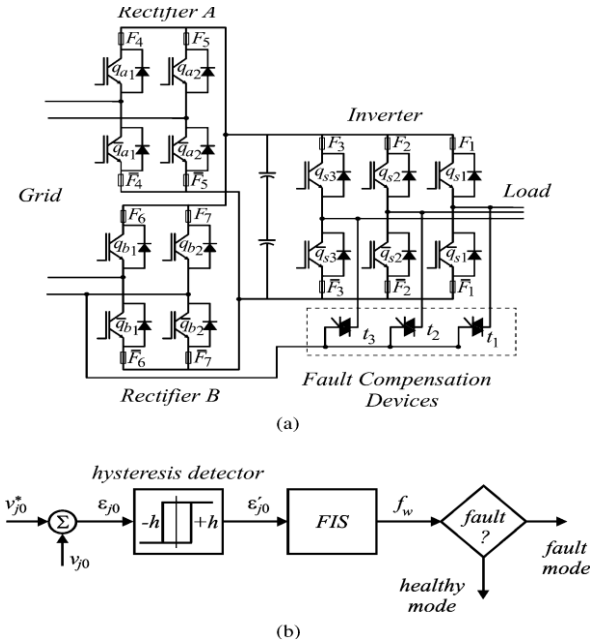

Fig. 6: (a) proposed configuration highlighting devices of fault-tolerant system. (b) Block diagram of the fault diagnosis system.

The fault detection and identification is carried out in four steps:

1) Measurement of pole voltages (v_{j0});

2) Computation of the voltage error εj0 by comparison of reference voltages and measurements affected in Step 1);

3) Determination as to whether these errors correspond or not to a faulty condition; this can be implemented by the hysteresis detector shown in Fig. 6(b);

4) Identification of the faulty switches by using ε'j0.

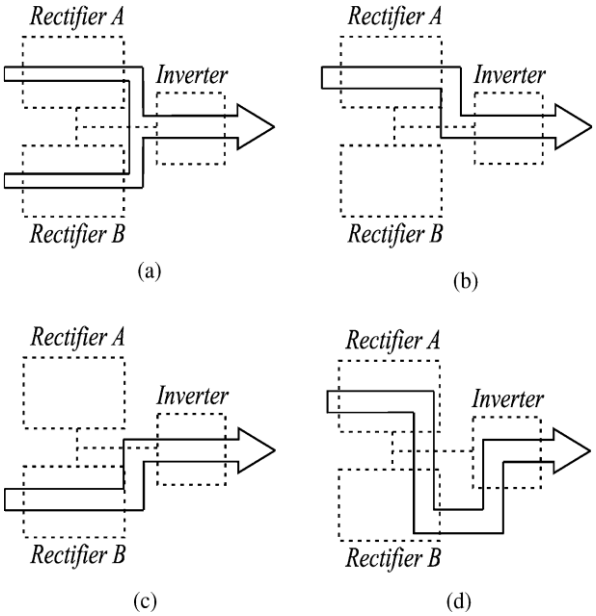

Fig. 7: Possibilities of configurations in terms of fault occurrence. (a) Pre-fault system. (b) Post-fault system with fault at the rectifier B. (c) Post-fault system with fault at the rectifier A. (d) Post-fault system with fault at the inverter.

This way, four possibilities of configurations have been considered in terms of faults:

1) Pre-fault ("healthy") operation [see Fig. 7(a)];

2) Post-fault operation with fault at the rectifier B [see Fig. 7(b)];

3) Post-fault operation with fault at the rectifier A [see Fig. 7(c)];

4) Post-fault operation with fault at the inverter [see Fig. 7(d)].

When the fault occurrence is detected and identified by the control system, the proposed system is reconfigured and becomes similar to that in Fig. 1.

For instance, if a fault in any switch of rectifier A has been detected by the control system, the whole rectifier needs to be isolated. This isolation procedure depends on the kind of fault detected. If an open-circuit failure is detected, the control system will open all switches of the rectifier A. On the other hand, if a short circuit is

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detected, the control system will turn on all switches related to rectifier A, and in this case, the fuses will open, and consequently, the rectifier will be isolated. Considering now a fault in one leg of inverter, in this case the SCR related with this leg in turned on and the leg b1 is isolated, so that the leg b2 of rectifier B will operate as the leg of inverter.

Losses and efficiency

The evaluation of the rectifier losses is obtained through regression model presented in [12]. The switch loss model includes:

1) IGBT and diode conduction losses;
2) IGBT turn-ON losses;
3) IGBT turn-OFF losses; and
4) Diode turn-OFF energy.

The loss evaluation takes into account just the rectifier circuit, since the inverter side of converter is the same for the proposed and standard configurations.

When the rectifiers operate with a switching frequency equal to 5 kHz, the conduction and switching losses of the proposed topology were 70% and 105%, respectively, of the corresponding losses of the conventional topology. Consequently, in this case, the total losses of the proposed topology were smaller than that of the conventional topology. The increase of the switching frequency does not change the conduction losses of both topologies, but increases their switching losses, especially for the proposed topology that has a high number of switches.

The proposed system can be used in the same applications as the conventional configuration (rural or remote application), especially when the THD of the grid current, fault tolerance and efficiency of converter are critical issues. In Brazil, it is quite common to have a single-phase distribution system and a demand to supply a three-phase motor. A single-phase to three-phase converter with bidirectional flux in the rectifier circuit has been required in the distributed generation system.

SIMULATION RESULTS

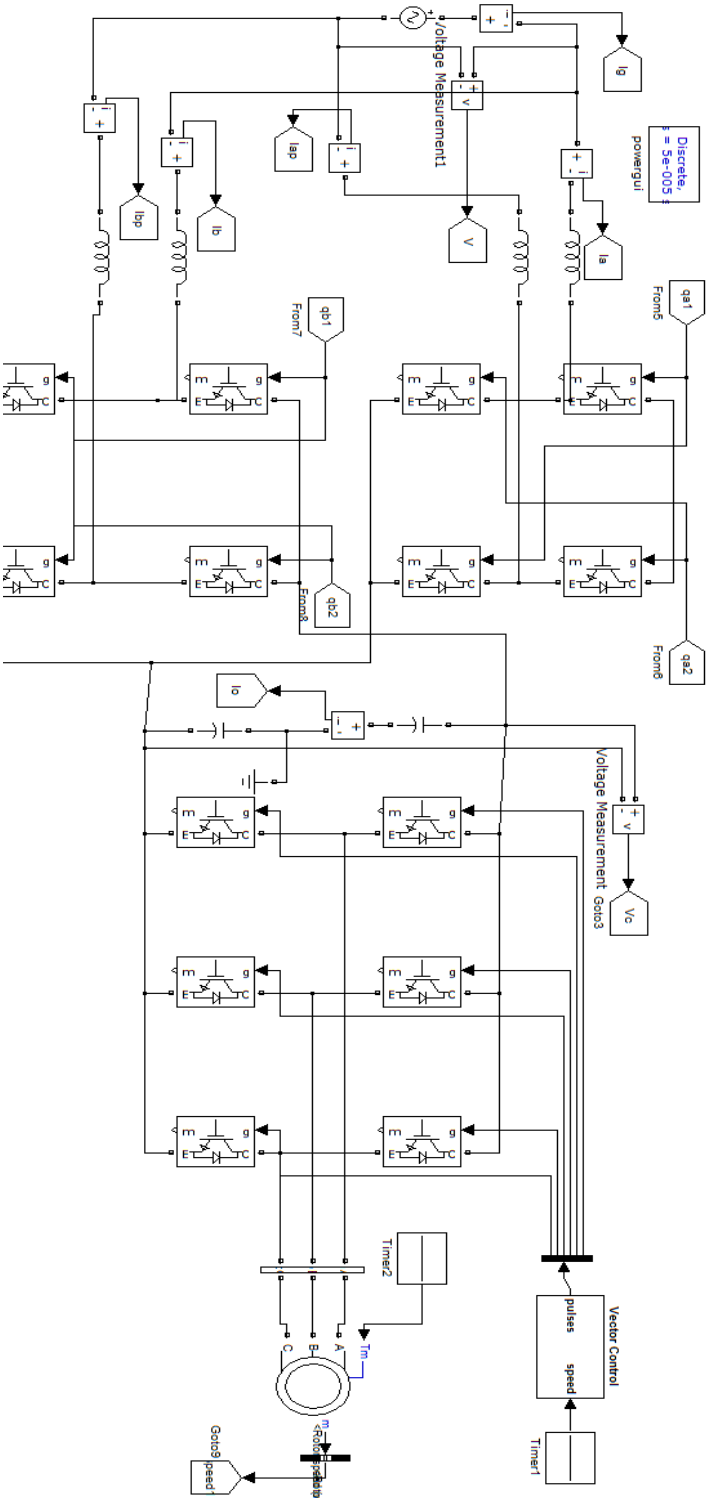

Fig 8: simulation design of proposed converter

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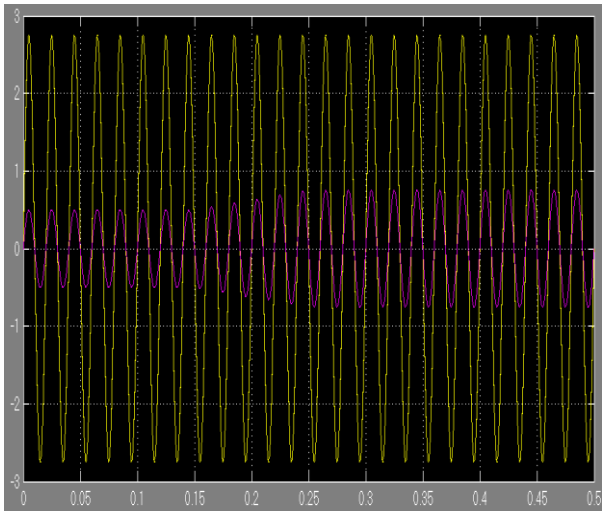

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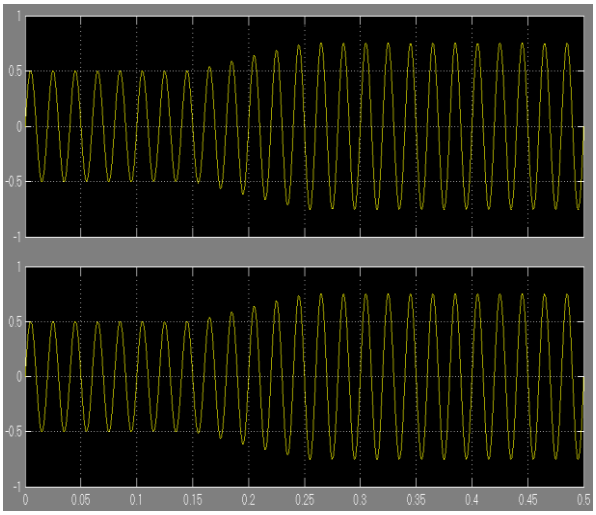
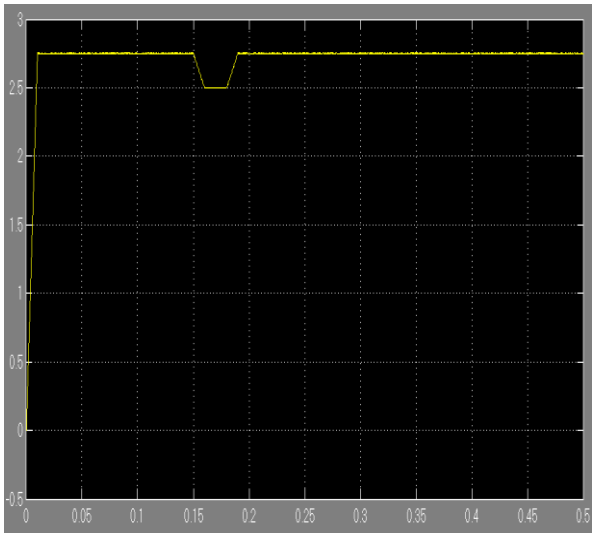


(d)



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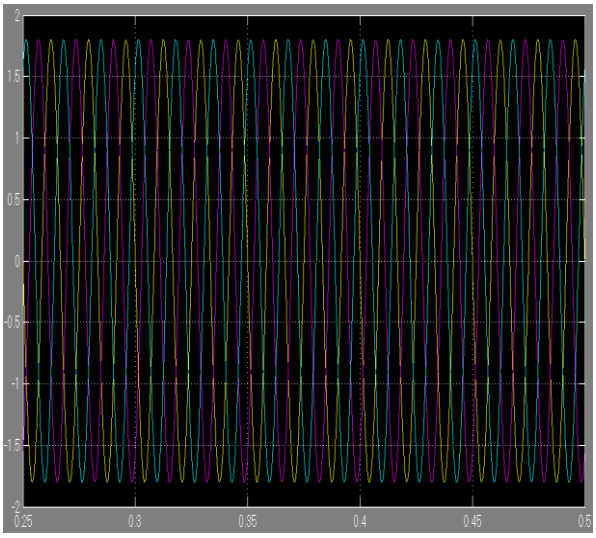

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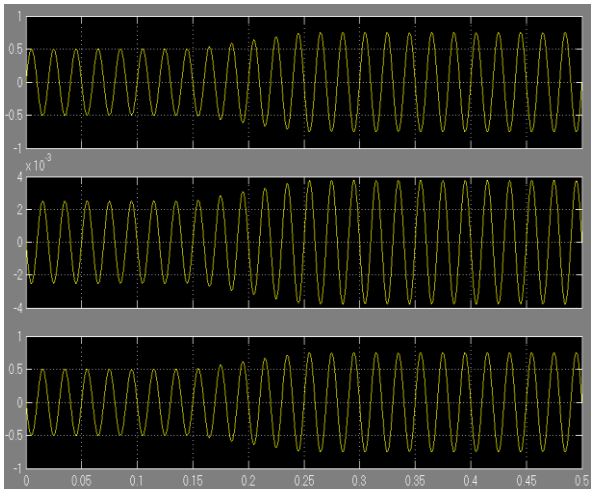
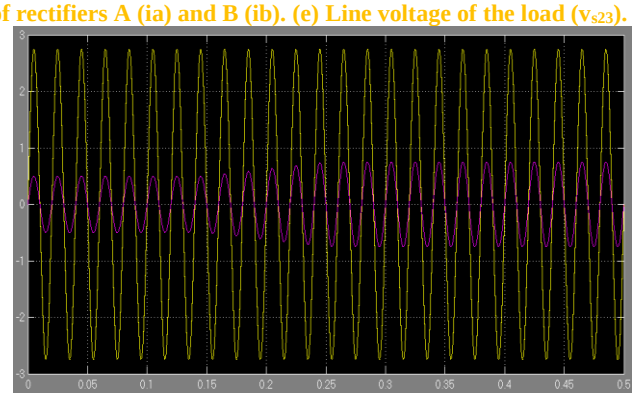


(c)

Fig. 9: Steady-state experimental results. (a) Grid voltage (eg) and gird current (ig). (b) Capacitor voltage (vc). (c) Currents of rectifier A (ia and I'a) and circulating current (io). (d) Currents of rectifiers A (ia) and B (ib). (e) Line voltage of the load (v_{s23}).



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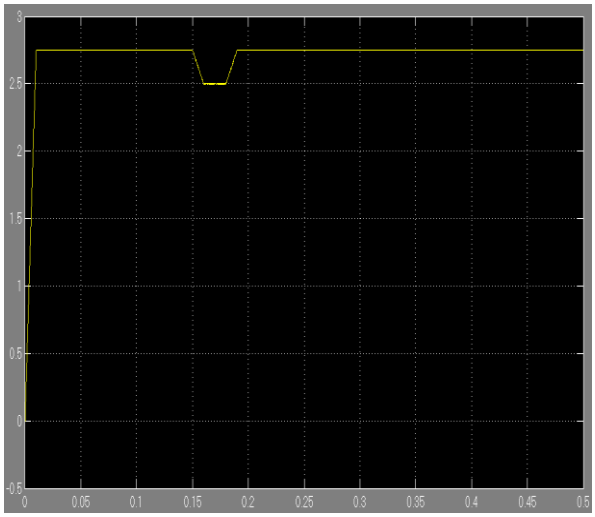
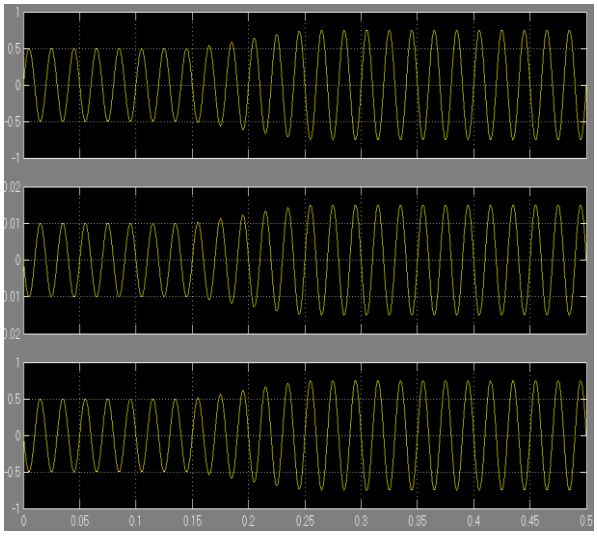


(a), (b)



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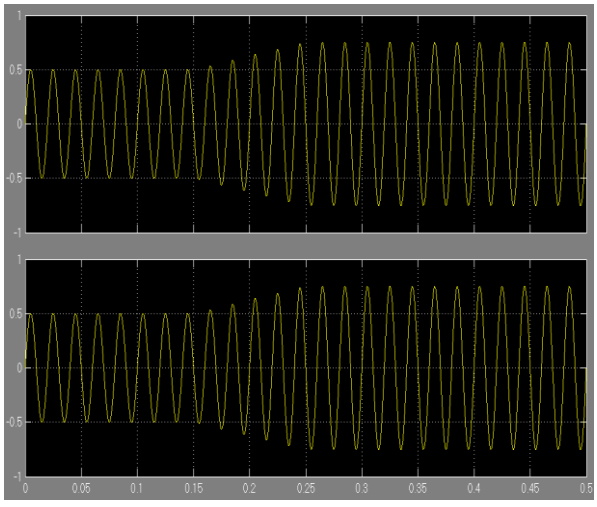

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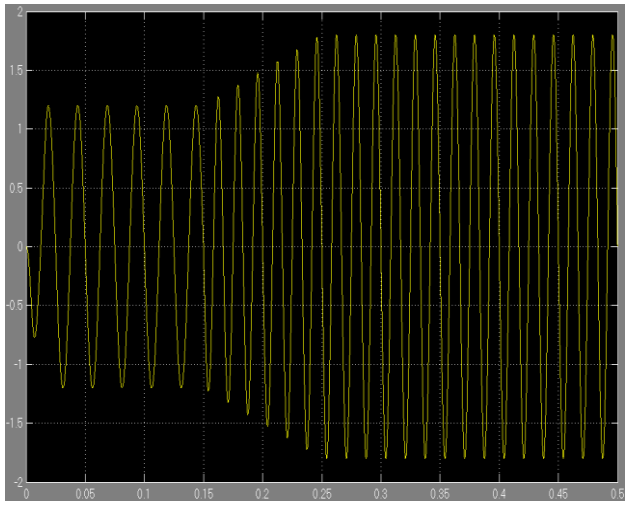
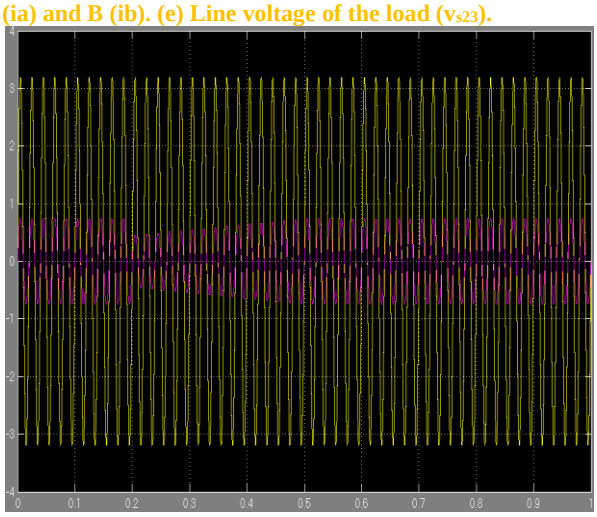
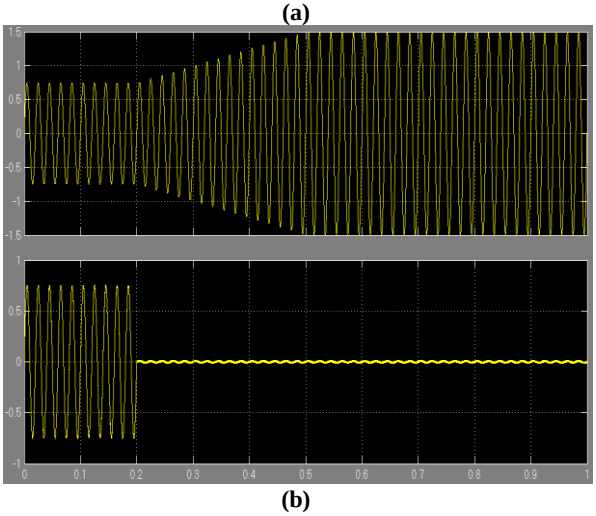


(e)

Fig. 10: Experimental results for a volts/hertz transient applied to the three-phase motor. (a) Grid voltage (eg) and gird current (ig). (b) Capacitor voltage (vc). (c) Currents of rectifier A (ia and I'a) and circulating current (io). (d) Currents of rectifiers A (ia) and B (ib). (e) Line voltage of the load (v_{s23}).



(a)



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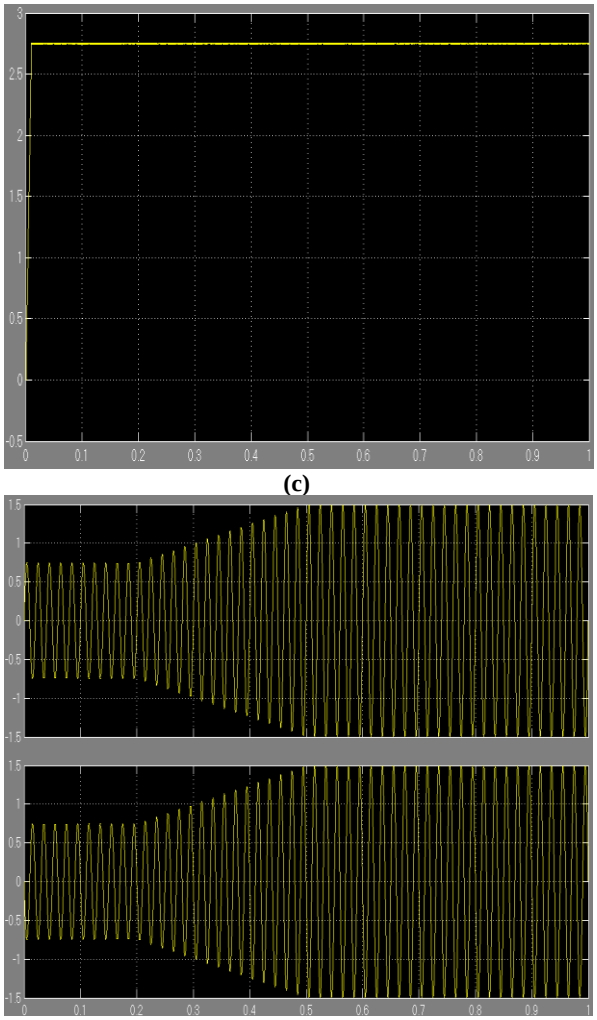
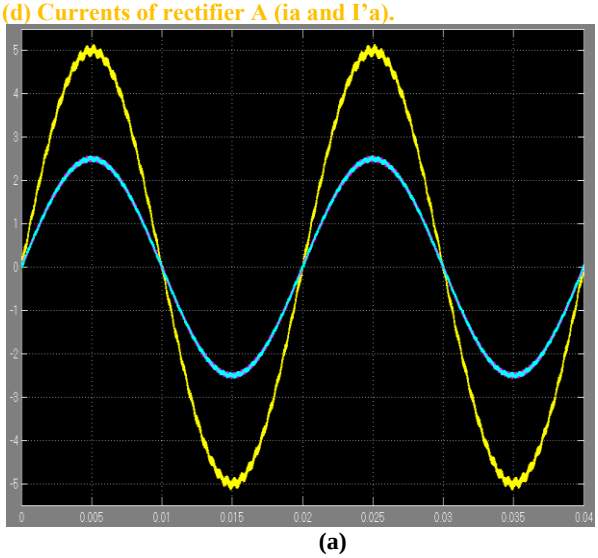


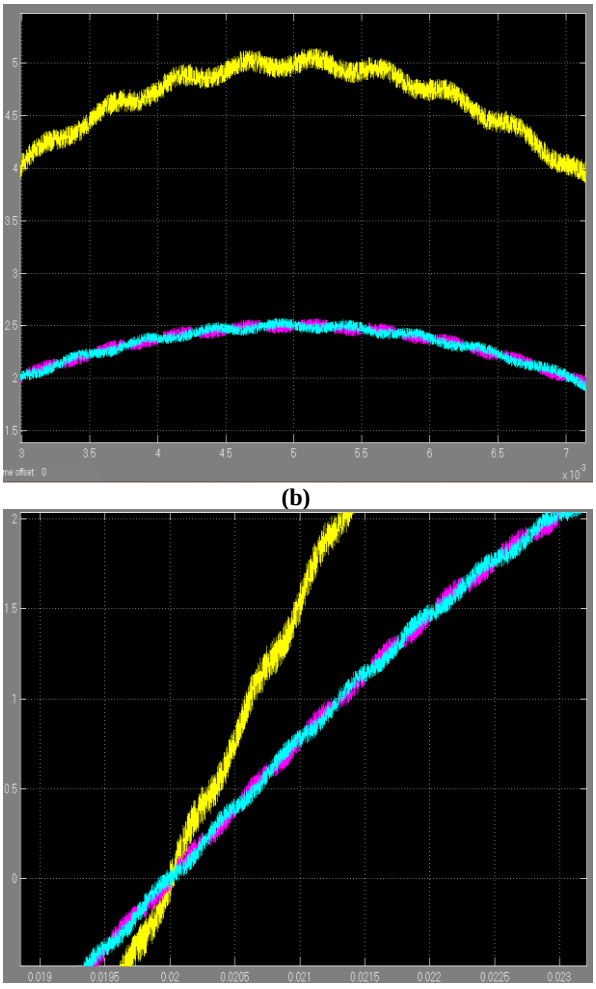
(c)

(d)

Fig.11: Experimental results of the proposed configuration when a fault is identified at the rectifier B. (a) Grid voltage (eg) and grid current (ig). (b) Currents of rectifiers A (ia) and B (I'b). (c) Capacitor voltage (vc).
(d) Currents of rectifier A (ia and I'a).



(a)



(b)

(c)

Fig. 12: Experimental results highlighting the interleaved operation (double carrier PWM). (a) Complete view. (b) Zoom of the point 1. (c) Zoom of the point 2.

CONCLUSION

The complete comparison between the proposed and standard configurations has been carried out in this paper. Compared to the conventional topology, the proposed system permits to reduce the rectifier switch currents, the THD of the grid current with same switching frequency or the switching frequency with same THD of the grid current and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart.

A single-phase to three-phase drive system composed of two parallel single-phase rectifiers, a three-phase inverter and an induction motor was proposed. The system combines two parallel rectifiers without the use of transformers. The system model and the control

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strategy, including the PWM technique, have been developed.

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