

# An Efficient Area and Power Optimization of A Sequential Circuits Using Multi-Bit Flip-Flop

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## Abstract:

In modern VLSI designs, power consumed by clocking has taken a major part of the entire design. In VLSI circuits clock is the most dominating power consuming element. To achieve the optimum power, it is need to reduce the clocking power. This paper describes a method for reducing the power consumption by replacing some flip flops with fewer multi-bit flip flops. Concept of merging flip flops is implemented in a simple storage device. Proposed work will reduce the power when compared to the conventional system.

## Keywords:

latches, flip-flops, verilog.

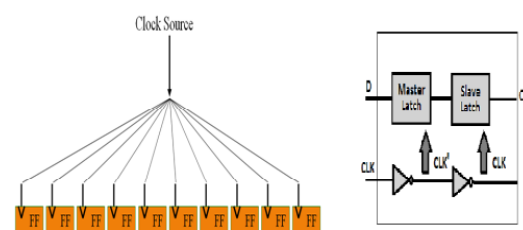
## 1.Introduction:

Nowadays, achieving low power consumption is a tedious one in IC fabrication industries which needs a faster clock which increases power dissipation. The Clock-Tree-Synthesis is the process of insertion of buffers or inverters along the clock path of ASIC design in order to achieve zero/minimum skew or balanced skew Large clock skew can force the designer to use large time period between clock pulses which make the system to perform slower. Usually clock trees are created by using buffers or inverters. Building a inverter clock tree would use less FFT's than building buffer clock tree to urge a similar target clock skew. Thus it might get less power consumption and delay. Hence to reduce the power consumption several low-power design techniques are adopted such as gated clock and making multi-supply-voltage styles, minimizing clock network and dynamic voltage/frequency scaling. With these techniques minimizing clock network is extremely vital in reducing power consumption as a result of it accounts for up to 45% of dynamic power of the chip.

So in this clock system 90% of the power is consumed by the flip-flops themselves and also the last branches of the clock distribution network that directly drives the flipflops. Thus the single bit flip-flop are used and every flip-flop needs a separate clock buffers which consumes large power. The remaining paper is structured as; the Section 2 describes the conventional flip-flop and their drawbacks. The section 3 will explains about the proposed method and section 4 describes the implementation details. Section 5 and Section 6 describes the simulation analysis and conclusion respectively.

## 2.Conventional System:

A flip-flop is a single bit memory storage element, which is very similar to a latch in that it is a bistable device which having two states and a feedback path that allows it to store a one bit of information. The variation between latch and flip-flop is that a latch is level triggered and the flip-flop is edge triggered. Flip-flops are classified into several different types each with its own uses and operations. Flip-flops are of four different types such as SR, D, JK, and T. In conventional type each flip-flop requires a separate clock source which increase the clocking power considerably also the area and clock skew will get increased which is shown in fig:1.



**Fig:1 (a) A path from clock source to clock sink,(b) single bit flip-flop**

Fig: 1(b) shows a single bit flip-flop it has two latches (Master latch and slave latch). The latches need Clk signal to trigger the device. In order to have better delay from Clk to Q we will regenerate Clk from Clk. So it will have two inverters in the clock path.

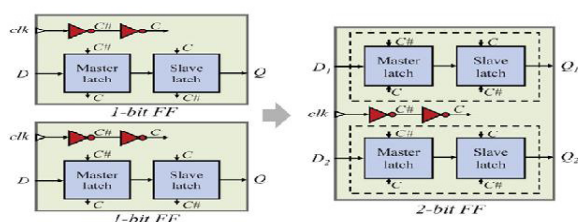
### 3. Proposed System:

The aim of the present work is therefore to propose the Multi-bit flip-flops which merge the single bit flip-flop that share the clock buffers. As CMOS technology improves, the driving capability of an inverter-based clock buffer rises. Thus driving capability of a clock buffer can be evaluated by the number of minimum-sized inverters that it can drive on a given rising or falling time. Due to manufacturing ground rules inverters in flip-flops tend to be increased in size. So as we get into micro technology like 65nm and beyond the least size of clock driver can drive more than single flip-flop.

The advantages of Multi-bit flip-flops :

1. Design area is being small
2. Needs less power and delay
3. Controllable clock skew
4. Improve in routing resource utilization

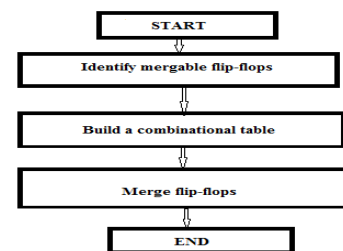
According to section 2, among those flip-flops; D flip-flop is chosen for this project because of low power consumption and its simplicity. The merging of 2 single bit flip-flops have been shown in Fig 2.



**Fig: 2. Merging of flipflops (a) 2 single bit flip-flop(before merging) (b) 2 bit flip-flop(after merging)**

In this section, we introduced the multi-bit flip-flop concept. Before that we will discuss about single-bit flip-flop Fig: 2 shows an example of merging two 1-bit flip-flops into one 2-bit multi bit flip-flop. Fig 2(a) describes replacement of two 1-bit flip-flops by the 2-bit flip-flop as shown in Fig. 2(b) total power consumption can be reduced because the two 1-bit flip-flops can share the same clock buffer.

Merging single-bit flip-flops into one multi-bit flip-flop can avoid additional inverters and reduces the total clock dynamic power consumption. Also the total area occupied by the flip-flops can also be reduced. The Fig 3 shows the flow chart of proposed work. Our proposed work is roughly divided into three steps. First step is identifying merge-able flip-flops, Build a combination table, and Merge flip-flops. In first stage, we have to identify the flip-flops which are supposed to be combined. And in second stage, a combination table can be formed, which defines all possible combinations of flip-flops in order to get a new multi-bit provided by library. In third stage, the flip-flops can be merged with the help of the table.



**Fig: 3. Proposed system flow chart.**

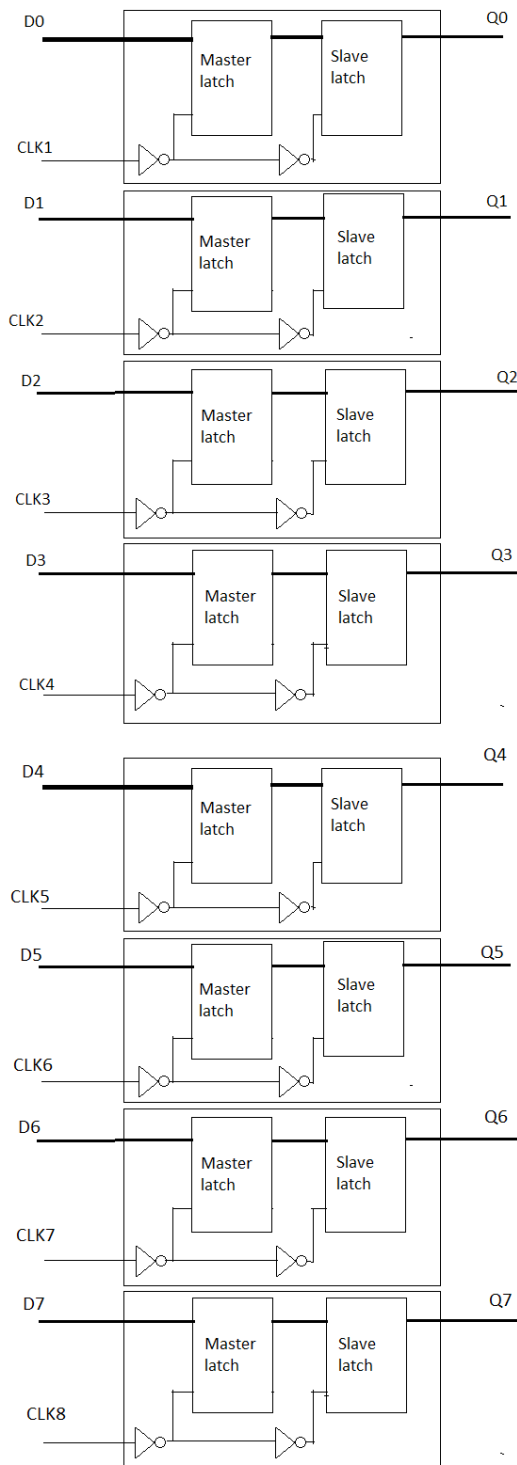
### 3.1 Identifying Merge able Flip-Flops:

Multi-bit flip-flop cells are capable of decreasing the power consumption due to sharing of common inverters internally done in the flip-flop. At the same time they can reduce the clock skew. To obtain these benefits, the ASIC design must meet the following requirements. Thus the single-bit flip-flops want to be replaced with multi-bit flip-flops must have same clock condition and same set/reset condition. We may have so many combinations to form a single multi-bit flip-flop. For example, consider that we have to build a 4-bit flip-flop we may have 3 combinations to setup that, i.e. by merging four 1-bit flip-flops else by merging two 2-bit flip-flops or else it can be formed by merging one 3-bit and one 1-bit flip-flop.

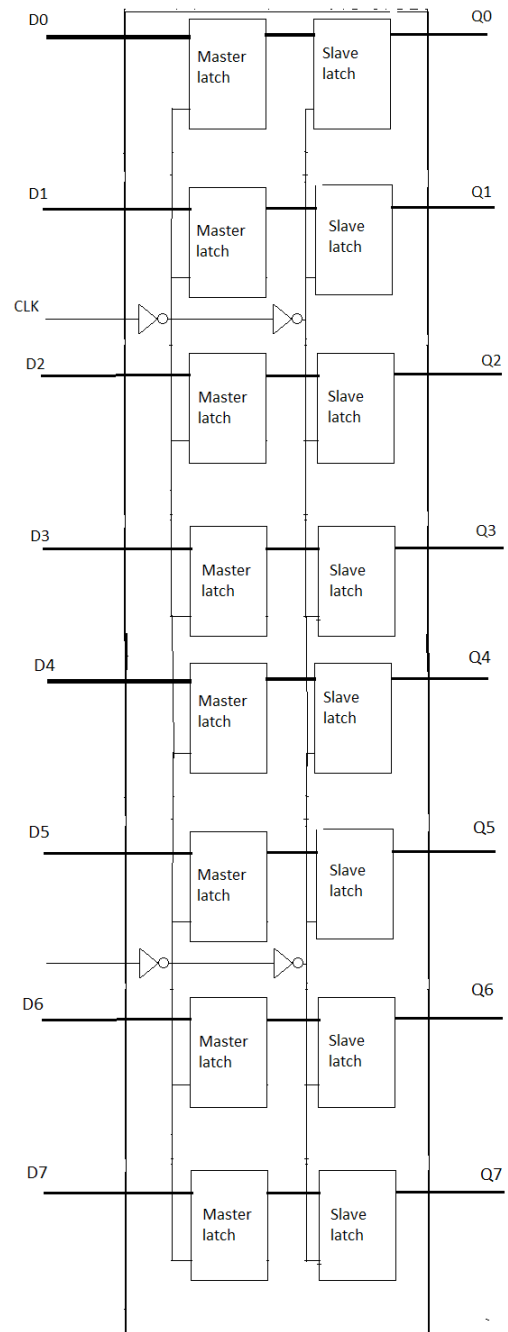
### 4. Implementation Details:

We implemented this concept in a simple 4bit register circuit and also analyzed the power consumption. This as shown in figure.4 and proposed Multibit flip-flop design is shown in figure 5. In this four single bit flip-flops are used, which requires four separate clock drivers.

In our proposed work the multi-bit flip-flop concept is implemented in the register, which requires single clock driver to drive them and the corresponding power consumption is measured.



**Fig. 4. A simple 8-bit register circuit**



**Fig.5. Proposed 8-bit multibit flip-flop**

## 5. Result Analysis:

We implemented the concept in Verilog HDL and are executed by Xilinx ISE Design suit with Modelsim simulator. Results for the power differences between existing system and proposed system is shown in the below figures.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		84
Vccint 1.20V:	28	33
Vccaux 2.50V:	12	30
Vcco25 2.50V:	8	20
Clocks:	9	10
Inputs:	3	4
Logic:	0	0
Outputs:	7	17
Signals:	0	0
Quiescent Vccint 1.20V:	16	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Fig: 6. Power consumption of the existing system.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		72
Vccint 1.20V:	18	22
Vccaux 2.50V:	12	30
Vcco25 2.50V:	8	20
Clocks:	2	2
Inputs:	1	1
Logic:	0	0
Outputs:	7	17
Signals:	0	0
Quiescent Vccint 1.20V:	16	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Fig:7. Power consumption of the proposed system.

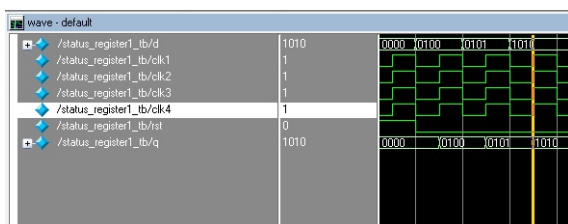


Fig:8. Simulation results obtained for 8-bit register using single bit flipflop.

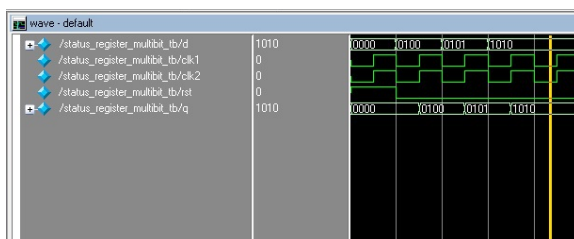


Fig:9. Simulation results obtained for 8-bit multibit flip-flop.

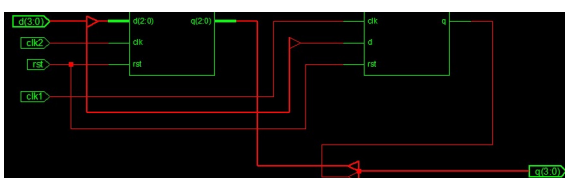


Fig:10. RTL Schematic of Proposed system.

## 6. Conclusion:

In this project, the concept of Multi-bit flip-flops is introduced for the replacement of single-bit flip-flop which achieves the reduced power consumption in a circuit. Simulation and synthesis results have been observed by using Modelsim and XILINX XST tool. The proposed work have achieved the power reduction when compared to the conventional system.

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