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Realization of Zero-Voltage Switching (ZVS) Operation in All Switching Devices Using Six-Switch Three-Phase Inverter with an Additional Switch Based on Space Vector Modulation (SVM) Scheme

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Abstract:
A power inverter, or inverter, is an electronic device or circuitry that changes direct current (DC) to alternating current (AC). The input voltage, output voltage and frequency, and overall power handling depend on the design of the specific device or circuitry. The inverter does not produce any power; the power is provided by the DC source. In a high-power grid-connected inverter application, the six-switch three-phase inverter is a preferred topology with several advantages such as lower current stress and higher efficiency. To improve the line current quality, the switching frequency of the grid-connected inverter is expected to increase. Higher switching frequency is also helpful for decreasing the size and the cost of the filter. However, higher switching frequency leads to higher switching loss. The soft-switching technique is a choice for a high-power converter to work under higher switching frequency with lower switching loss and lower EMI noise. The inverter can realize zero-voltage switching (ZVS) operation in all switching devices and suppress the reverse recovery current in all anti parallel diodes very well. And all the switches can operate at a fixed frequency with the new SVM scheme and have the same voltage stress as the dc-link voltage. In grid-connected application, the inverter can achieve ZVS in all the switches under the load with unity power factor or less. The aforementioned theory is verified in this paper. The reduced switching loss increases its efficiency and makes it suitable for practical applications.

Keywords: ZVS, SVM, Inverter, Switching, PWM, Power-grid.

Introduction:

Three-phase inverters are used for variable-frequency drive applications and for high power applications such as HVDC power transmission. A basic three-phase inverter consists of three single-phase inverter switches each connected to one of the three load terminals. For the most basic control scheme, the operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform. This creates a line-to-line output waveform that has six steps. The six-step waveform has a zero-voltage step between the positive and negative sections of the square-wave such that the harmonics that are multiples of three are eliminated as described above. When carrier-based PWM techniques are applied to six-step waveforms, the basic overall shape, or envelope, of the waveform is retained so that the 3rd harmonic and its multiples are cancelled. To construct inverters with higher power ratings, two six-step three-phase inverters can be connected in parallel for a higher current rating or in series for a higher voltage rating. In either case, the output waveforms are phase shifted to obtain a 12-step waveform. If additional inverters are combined, an 18-step inverter is obtained with three inverters etc. Although inverters are usually combined for the purpose of achieving increased voltage or current ratings, the quality of the waveform is improved as well.

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Electronic power processing technology has evolved around two fundamentally different circuit schemes: duty-cycle modulation, commonly known as pulse width modulation (PWM), and resonance. The PWM technique processes power by interrupting the power flow and controlling the duty cycle, thus, resulting in pulsating current and voltage waveforms. The resonant technique processes power in a sinusoidal form. Due to circuit simplicity and ease of control, the PWM technique has been used predominantly in today's power electronics industries, particularly, in low-power power supply applications, and is quickly becoming a mature technology. As the semiconductor device switches off an inductive load, voltage spikes are induced by the sharp di/dt across the leakage inductances, On the other hand, when the switch turns on at high voltage level, the energy stored in the device's output capacitances, 0.5 CV2, is trapped and dissipated inside the device. Furthermore, tum-on high voltage levels induces a severe switching noise known as the Miller effect which is coupled into the drive circuit, leading to significant noise and instability.

For the zero current switching technique, the objective is to use auxiliary LC resonant elements to shape the switching device's current waveform at on-time in order to create a zero-current condition for the device to turn off. The dual of the above statement is to use auxiliary LC resonant elements to shape the switching device's voltage waveform at off-time in order to create a zero-voltage condition for the device to turn on. This latter statement describes the principle of zero voltage switching. The recognition of the duality relationship between these two techniques leads to the development of the concept of voltage-mode resonant switches and a new family of converters operating under the zero voltage switching principle.

Zero Voltage Switching Overview:

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's ontime with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converters. During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (Co& has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch.

Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V& equals zero.The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few.

In this paper, We introduce a circuit topology and associated control method suitable for high efficiency DC to AC grid-tied power conversion.In a high-power grid-connected inverter application, the six-switch three-phase inverter is a preferred topology with several advantages such as lower current stress and higher efficiency. To improve the line current quality, the switching frequency of the grid-connected inverter is expected to increase.

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Higher switching frequency is also helpful for decreasing the size and the cost of the filter. However, higher switching frequency leads to higher switching loss. The soft-switching technique is a choice for a high-power converter to work under higher switching frequency with lower switching loss and lower EMI noise.

Objective of Project:

The goal of this paper is to present a power stage design and preliminary results for three-phase grid-connected inverter that is suitable for grid interfacing, reduced switching loss, EMI and increase efficiency.

Scope of Project:

A soft-switchinginverter is a high-efficiency inverter intended, in particular, for use with three-phase drives, as a grid-tie inverter for photovoltaic installations or wind turbines and in power supplies.

Research work contribution:

A six-switch three-phase inverter is widely used in a high-power grid-connected system. However, the antiparallel diodes in the topology operate in the hard-switching state under the traditional control method causing severe switch loss and high electromagnetic interference problems. In order to solve the problem, this paper proposes a topology of the traditional six-switch three-phase inverter but with an additional switch and gave a new space vector modulation (SVM) scheme. In this way, the inverter can realize zero-voltage switching (ZVS) operation in all switching devices and suppress the reverse recovery current in all antiparallel diodes very well.

Existing System
With Demerits brief explanation.

The anti-parallel diodes in the six-switch three-phase inverter topology operate in the hard-switching state underthe traditional control methodcausing severe switch loss and high electro-magnetic interference problems.

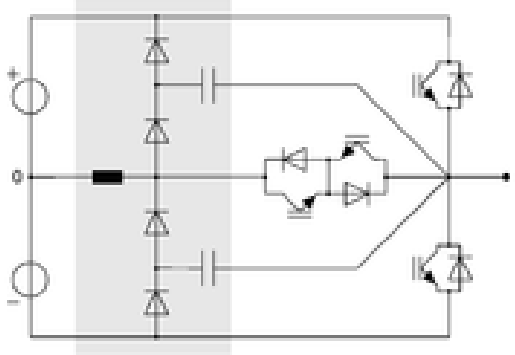
Proposed System

We propose a new topology of the traditional six-switch three-phase inverter with an additional switch and gave a newspace vector modulation (SVM) scheme.

Inverter Topology

Inverters are used for converting DC voltage into AC voltage. Their construction typically makes use of power transistors and diodes. These are operated as electronic switches. In conventional designs using "hard" switching, this gives rise to switching losses which, especially for high values of the switching frequency, cause a reduction in their energy conversion efficiency. To improve their efficiency, high-power inverters (from about 10 kW) frequently make use of a technique referred to as a three-level design (three-level inverter).

Forming the basis of the S3L inverter is a hard-switching three-level inverter of this kind with a T-type topology. This base design is supplemented by a snubber circuit consisting of a few passive components. It prevents the occurrence of simultaneously high values of voltage and current, and hence high power dissipation values, during the switching process. All switching processes therefore take place in a "soft" manner. In this way switching losses are largely avoided. Furthermore, because the snubber circuit functions, in principle, without losses, the conversion efficiency of the inverter remains high even for high values of the switching frequency



Schematic circuit diagram of the S3L inverter. The snubber circuit is highlighted in grey

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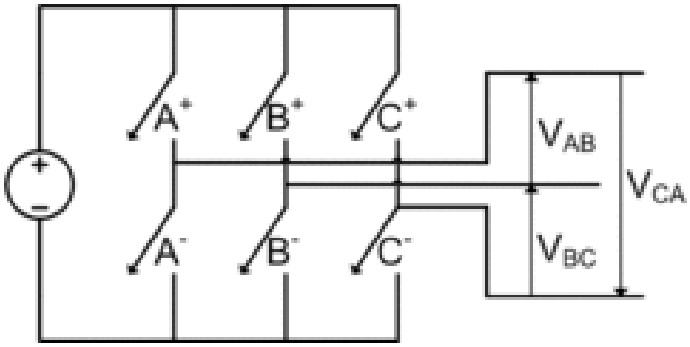
SPACE VECTOR MODULATION SCHEME

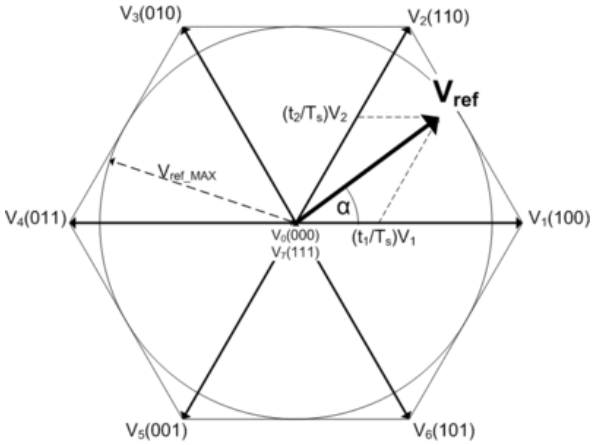
Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM).[1] It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

Principle

Topology of a basic three phase inverter.



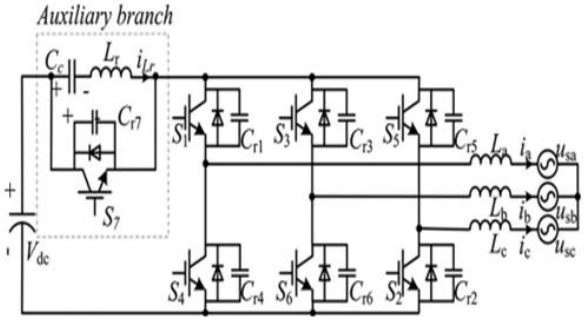
A three-phase inverter as shown above converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor.The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. i.e. if A+ is on then A− is off and vice versa. This leads to eight possible switching vectors for the inverter, V0 through V7 with six active switching vectors and two zero vectors To implement space vector modulation, a reference signal Vref is sampled with a frequency fs (Ts = 1/fs). The reference signal may be generated from three separate phase references using the α β γ transform. The reference vector is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors. Various strategies of selecting the order of the vectors and which zero vector(s) to use exist. Strategy selection will affect the harmonic content and the switching losses.



All eight possible switching vectors for a three-leg inverter using space vector modulation. An example V_{ref} is shown in the first sector. V_{ref_MAX} is the maximum amplitude of V_{ref} before non-linear overmodulation is reached.

METHODOLOGY

The topology is composed of a standard PWM inverter and a clamping branch. The clamping branch consists ofactiveswitchS7,resonantinductorLr,andclampingcapacitor Cc.



During most time of operation, the active switch S7 is in conduction and energy circulates in the clamping branch. When the auxiliary switchS7 isturned OFF, the current in the resonant inductor I Lr will discharge the parallel capacitors of the main switch and then the main switch can be turned ON under the zero-voltage condition. When the main switch is turned ON, Lr suppresses the reverse recovery current of an antiparallel diode of the other main switch on the same

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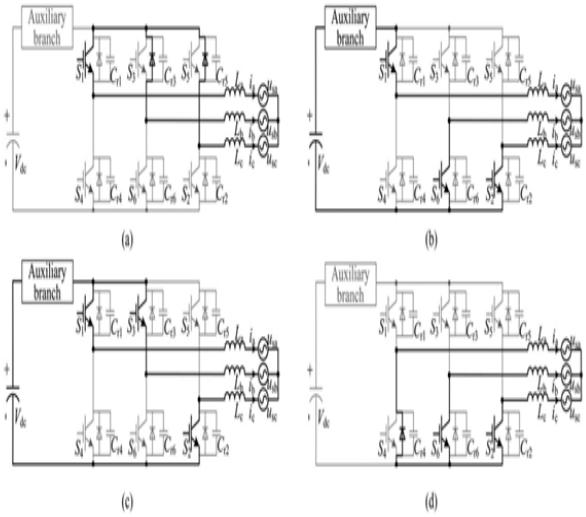
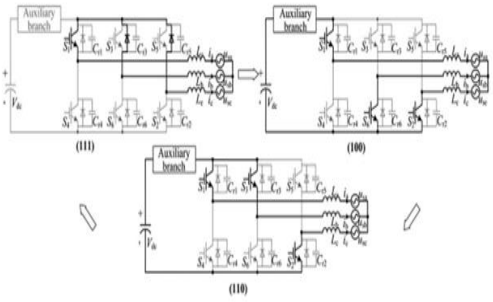
bridge. Since there are three legs in the main bridge, normally the auxiliary switch must be activated three times per PWM cycle if the switch in the three legs is modulated asynchronously. To make the auxiliary switch having the same switching frequency as the mains witch, a specia lSVM scheme is proposed to control the inverter. Suppose that the grid-connected inverter works with unity power factor; the grid line voltage and the inverter output current wave form; the corresponding voltage sector definition is shown in Fig.



Four switching states in the SECT1-1: (a) state 111, (b) state 100, (c) state 110, and (d) state 000

In voltage SVM, the whole utility cycle can be divided into six voltage sectors, and every grid voltage sector canstill be divided into two different smaller sectors according to the maximum value of the phase current in the inverter. For example, the grid voltage sector SECT1 can be divided into SECT1-1 and SECT1-2.InSECT1-1,theabsolutevalueofthephase-Acurrent obtainsthemaximumvalue,andinSECT1-2,theabsolutevalue of the phase-C current does the same. Since the operation of the converter is symmetrical in every 30◦, assume that the inverter is operating in SECT1-1. If the grid-connected inverter works with unity power factor, ia> 0 and ic<ib< 0 in SECT1-1. The phase voltage and phase current in phase A obtains the maximum value; there exist four switchingstates:111,100,110,and000. If the switching sequence in SECT1-1 is 111-100-110-111, , then the zero vector will always be 111 and switch S1 will always be in conduction. When the switching state changes from 111 to 100, switches S6 and S2 will be turned ON simultaneously. The auxiliary branch needs to act in this transition process to suppress the reverse recovery currents ofantiparalleldiodesofS3 andS5 andcreatetheZVScondition for S6 and S2. During the state from 100 to 110, the current in S6 at first will flow into the antiparallel diode of S3. During the state from 110 to 111, the current in S2 will flow into the antiparallel diode of S5. These two transitions are normal soft switching. Thus, the auxiliary branch only needs to act once in one switching cycle to resonant the dc bus to zero, creating the ZVS condition for the switches and suppressing the diode recoveries in two phases. The auxiliary switch can work at the same frequency as the main switch. And the main switch can be turned ON or OFF at the exact time decided by the SVM control. The resonant process equivalent circuits in the state change from 111 to 100. The key waveform of the inverter equivalent circuit in SECT1-1.



Switching sequence in SECT1-1: 111-100-110-111

ALGORITHMS FOR PROJECT DESIGN

The following assumptions are made to simplify the analysis of the ZVS inverter:

1) switches S1–S7 are considered as an ideal switch with its antiparallel diode;

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2) capacitances Cr1–Cr7 paralleled with switches S1–S7, respectively, include parasitic capacitance and external capacitance;

3) inoneswitchingcycle,theinductorcurrentrippleissmall and can be considered as a constant current source;

4) the capacitance of the clamping capacitor Cc is large enough, so the voltage ripple across it is small, and thus can be regarded as a voltage source;

5) the resonant frequency of Cc and Lr is much lower than the operation frequency of the converter.

During circuit topological changes, the complete circuit operation can be divided into nine stages:

Stage 1 (t0–t1): Main switches S1,S 3, and S5 and auxiliary switchS7 areON.Thecircuitisinthestate111.Intheauxiliary resonantcell,thevoltageofLr isclampedbyclampingcapacitor Cc, and its current iLr increases at the rate ofdiLrdt=−VCcLr

Stage 2 (t1–t2): In t1,S 7 isturned OFF; theresonant inductor Lr discharges the parallel capacitors Cr4, Cr6, and Cr2 and charges parallel capacitor Cr7 of the auxiliary switch S7.S 7 is turned OFF under the ZVS condition because of the snubber capacitor Cr7.

Stage 3 (t2–t3): In t2, the voltage across S7 reaches Vdc,S 7 is OFF, the voltages across Cr4, Cr6, and Cr2 drop to zero, and the antiparallel diodes of these main switches start to conduct. The resonant between Lr and these paralleled capacitors stops. S2 and S6 can be turned ON under the ZVS condition.

Stage 4 (t3–t4): In t3,S 2 and S6 are turned ON under the ZVS condition. In this stage, the currents in phase B and phase C convert from the antiparallel diodes of S3 and S5 to S2 and S6, respectively. When the main switch transition process completes, the antiparallel diodes of S3 and S5 experience diode reverse recovery. Due to the existence of the resonant inductor Lr, the diode reverse recovery is suppressed and the current in LriLr changes at the rate of

diLrdt= Vdc −VCcLr

Stage5 (t4–t5): Main switches S3,S4, and S5 are OFF at t4;thecircuitreachesthestate100.Lr,Cr3,Cr4,Cr5,andCr7 start to be in resonance. The voltages across S3, S4, and S5 start to increase and the voltage across S7 starts to decrease. At t5, the voltages across S2, S4, and S6 reach to Vdc, the voltage across S7 decreases to zero, and the antiparallel diode of S7 starts to conduct.S7 canbeturnedONundertheZVScondition.Lr,Cr3, Cr4, Cr5, and Cr7 stop to be in resonance. The time between t2 and t5 is the duty cycle loss of S2 and S6. As stages 3–5 are veryshortcomparedwiththewholeswitchingcycle,theim pact of this duty cycle loss on the circuit operation during the whole switching cycle can be ignored.

Stage 6 (t5–t6): At t5, the circuit reaches the state 100. The main switches S1,S 2, and S6 and the auxiliary switch S7 areON. The resonant inductor is charging the clamping capacitor Cc.

Stage 7 (t6–t7): At t6,S 6 is turned OFF. The inductor Lb will charge C6 and discharge C3. Due tothe existence of C3 and C6, S6 is turned OFF under the ZVS condition.

Stage 8 (t7–t8): The circuit reaches the state 110. The main switch S1,S 3, and S2 and the auxiliary switch S7 are ON. The resonant inductor is charging the clamping capacitor Cc.

Stage 9 (t8–t9): At t7,S2 is turned OFF. The inductor Lc will charge C2 and discharge C5. Due tothe existence of C5 and C2, S2 is turned OFF under the ZVS condition. At t9, the voltage on S5 decreases to zero, and the antiparallel diode of S5 starts to conduct. S6 can be turned ON under the ZVS condition. The circuit reaches the state 100. After t9, a new switching cycle starts again.

Matlab – Simulink & Results

MATLAB is a multi-paradigm numerical computing environment and fourth-generation programming language. A proprietary programming language developed by MathWorks, MATLAB allows matrix

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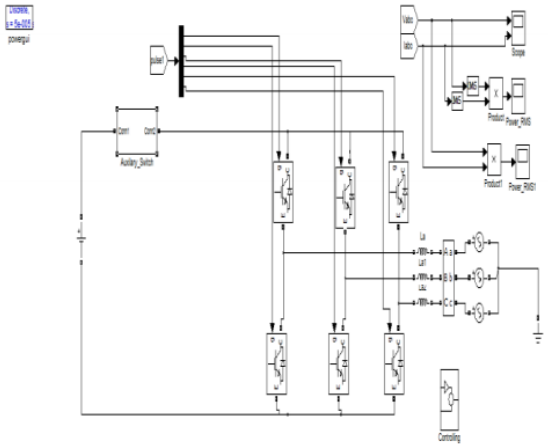
manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, Java, Fortran and Python. Simulink is a block diagram environment for multidomain simulation and Model-Based Design. It supports simulation, automatic code generation, and continuous test and verification of embedded systems. Simulink provides a graphical editor, customizable block libraries, and solvers for modeling and simulating dynamic systems. It is integrated with MATLAB, enabling you to incorporate MATLAB algorithms into models and export simulation results to MATLAB for further analysis.

A. ZVS Three phase inverter



Simulation diagram of ZVS three phase inverter

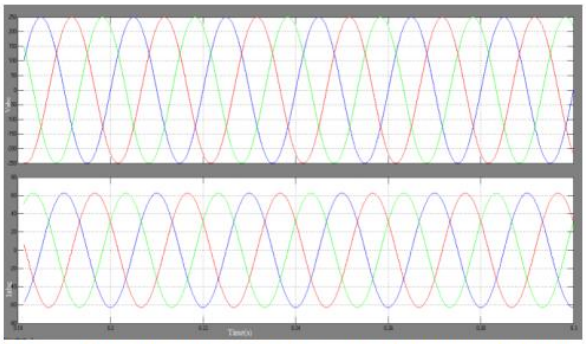


Fig. Output Voltage & Current of Proposed Three Phase ZVS based Grid Connected Inverter.

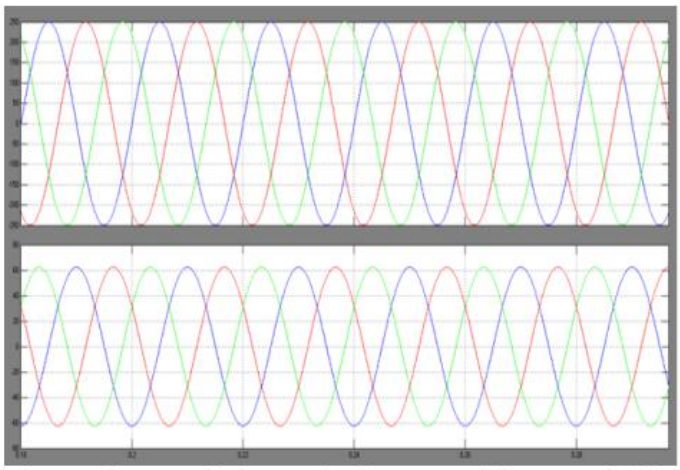


Fig. Output Voltage & Current of Proposed Three Phase ZVS based Grid Connected Inverter at inductance load.

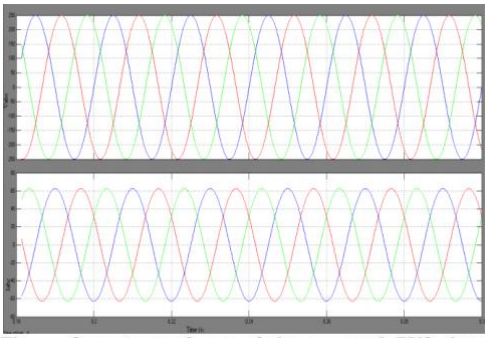


Fig. Output waveforms of the proposed ZVS three phase inverter.

CONCLUSION:

The simulation analysis verified using different power factors with the SVM-controlled three-phase soft-switching grid-connected inverter. It is observed that the ZVS operation for all switching devices, and the reverse recovery current in the anti parallel diodes of all switching devices is suppressed well. SVM can be realized at the fixed switching frequency. And the switching voltage stress across all the power switch devices is the same as the dc-link voltage. The ZVS can be achieved in the gridconnected ZVS inverters under the load with unity power factor or less. The reduced switching loss increases its efficiency and makes it suitable for practical applications. and further paper can be extended using multi level inverter.

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