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16- Bit Vedic Multiplier for Optimized Performance

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ABSTRACT:

Digital signal processing (DSP) is the technology that is omni present in almost every engineering discipline. Multipliers are inevitable components in digital system design and embedded applications. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction [1]. If the power consumption and delay of the multiplier is reduced then the effective processor can be generated; since, the performance of the any processor will depend upon its power and delay. The power and delay should be less in order to get an effective processor. Vedic Multiplication is an ancient methodology of Indian mathematics as it contains 16 SUTRAS (formulae). A high speed complex 16 X 16 multiplier design by using Urdhva Tiryakbhyam sutra is presented in this paper. By using this sutra the partial products and sums are generated in one step which reduces the design of architecture in processor's. By using this sutra we can reduce the time with high extent when compare to array and booth multiplier.

KEYWORDS:

Vedic Multiplier, Urdhva Tiryakbhyam, Power Dissipation, Propagation Delay. Multiplier, Vedic Mathematics.

INTRODUCTION:

The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or aphorisms [2]. These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. In the Vedic system difficult problems or huge sums can often be solved immediately by the Vedic method. These striking and beautiful methods are just a part of a complete system of mathematics which is far more systematic than the modern system. In this paper a simple 16 bit digital multiplier is proposed which is based on Urdhva Tiryakbhyam . Two binary numbers (16-bit each) are multiplied with this Sutra. The "Urdhva Tiryagbhyam" Sutra is a general multiplication formula applicable to all cases of multiplication. "Urdhva" and "Tiryagbhyam" words are derived from Sanskrit literature. "Urdhva" means "Vertically" and "Tiryagbhyam" means "crosswise".

Existing Binary array multiplier

An array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders. [3] This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the Adder array.

The Hardware requirement for an m x n bit array multiplier is given as:

(m x n) AND gates, (m-1).n Adders in which n HA(Half Adders) and (m-2).n FA(full adders). Consider 4x4 multiplications, say A= A3 A2 A1 A0

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and B= B3 B2 B1 B0. The output line for this multiplication is $Q_3Q_2Q_1Q_0R_3R_2R_1R_0$. Using the fundamental of Array Multiplication, taking partial product addition is carried out in Carry save form; we can have the following structure for multiplication as shown in Fig. 1. [1]

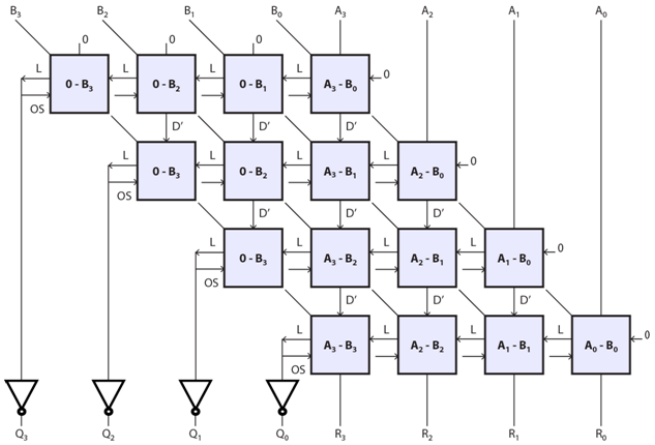

Figure 1. ARRAY MULTIPLIER

The multiplication of two 2-digit decimal numbers 25 and 21 using Urdhva Tiryakbhyam is shown in Figure 2.

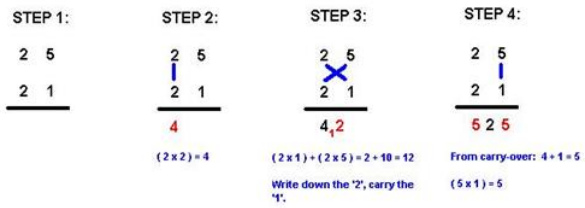

Figure 2. Example of VEDIC MULTIPLICATION

The algorithm can be generalized for n x n bit number [4]. The concurrency while obtaining the partial products and their sums results in the non dependency of the multiplier on the clock frequency of the processor. The usage of this multiplier ascertains that microprocessors need not operate at increasingly high clock frequencies, thereby eliminating the chances of higher power consumption. In addition to this, the drawing of its layout is much easier because of the regularity in its structure.

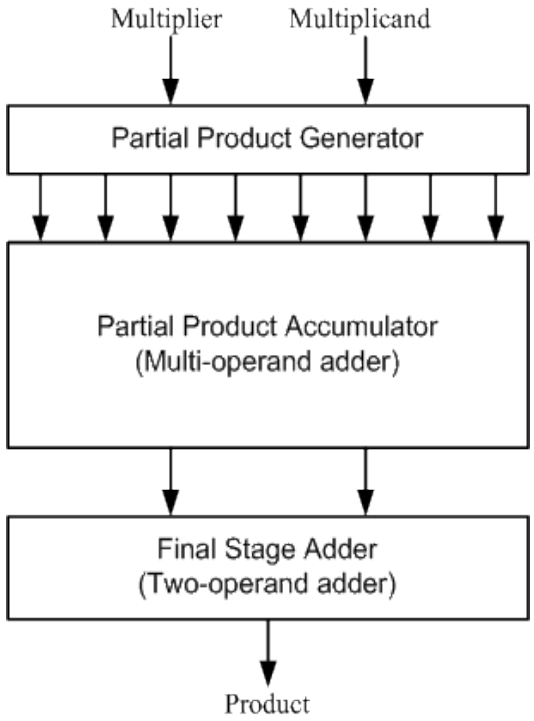

Figure 3. Basic Architecture of VEDIC MULTIPLIER

RESULT:

The synthesis result obtained from proposed Vedic multiplier is faster than Array multiplier. The design of 16x16 multiplier based on vedic multiplication technique have been implemented on QUARTUS II 9.1. The implementation was done in Verilog and ModelSIM

SIMULATION RESULT

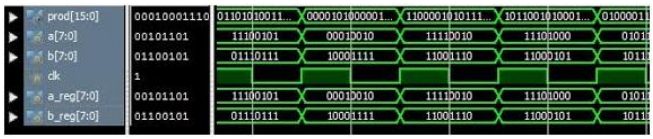

Figure 4.Simulation Result Of 16x16 Bit Vedic Multiplier

CONCLUSION:

Vedic Multiplier is highly suitable for high speed complex arithmetic circuits which are having wide application in VLSI and signal processing.

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This architecture combines the advantages of the Vedic mathematics for multiplication which encounters the stages and partial product reduction. The advantages of this proposed architecture is efficient in speed and area(less resources used, such as less number of multipliers and adders) and is Flexible in design.

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