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An On-Chip AHB Bus Tracer with Real Time Compression and Dynamic Multi Resolution Supports for SoC

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ABSTRACT:

This paper proposes a multiresolution AHB on-chip bus tracer named SYS-HMRBT (AHB multiresolution bus tracer)for versatile system-on-chip (SoC) debugging and monitoring.The bus tracer is capable of capturing the bus trace with differentresolutions, all with efficient built-in compression mechanisms, to meet a diverse range of needs. In addition, it allows usersto switch the trace resolution dynamically so that appropriateresolution levels can be applied to different segments of the trace.On the other hand, SYS-HMRBT supports tracing after/beforean event triggering, named post-triggering trace/pre-triggering trace, respectively. SYS-HMRBT runs at 500 MHz and costs 42 Kgates in TSMC 0.13- m technology, indicating that it is capable ofreal time tracing and is very small in modern SoCs. Experimentsshow that the bus tracer achieves very good compression ratios of79%–96%, depending on the selected resolution mode. As a casestudy, it has been integrated into a 3-D graphics SoC to facilitatethe debugging and monitoring of the system behaviors. The SoChas been successfully verified both in field-programmable gatearray and a test chip.

INTRODUCTION

At the timing dimension, it has two abstraction levels, which are the cycle level and transaction level. The cycle level captures the signals at every cycle.The Event Generation Module controls the start/stop time, the trace mode, and the trace depth of traces. This in-formation is sent to the following modules. Based on the trace mode, the Abstraction Module abstracts the signals in both timing dimension and signal dimension. The abstracted data are further compressed by the Compression Module to reduce the data size. Finally, the compressed results are packed with proper headers and written to the trace memory by the Packing Module.

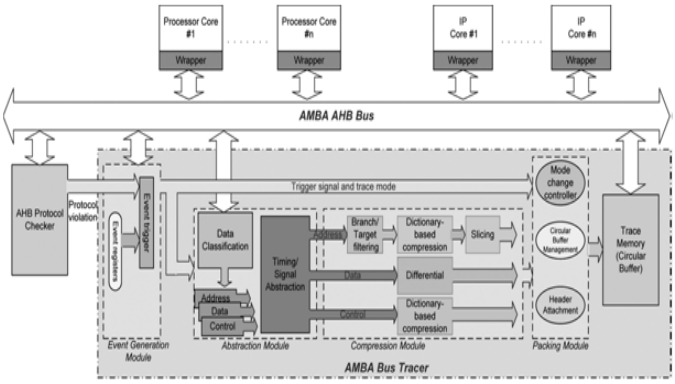

Figure 1: Multi-resolution bus tracer block diagram

The transaction level records the signals only when their value change (event triggering). For example, since the bus read/write control signals do not change during a successful transfer, the tracer only records this signal at the first and last cycles of that transfer. However, if the signal changes its value cycle-by-cycle, the transaction-level trace is similar to the cycle-level trace. Changes its value cycle-by-cycle, the transaction-level trace is similar to the cycle-level trace.

3.2 Architecture of on chip bus tracer:

This section presents the architecture of our bus tracer. We first provide an overview of the architecture for the post-T trace. We then discuss the three major compression methods in this architecture. Finally, we show the extension of the post-T architecture to support the pre-T trace.

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3.2.1 Post-T Tracer Architecture Overview: It mainly contains four parts:

1. Event Generation Module
2. Abstraction Module
3. Compression Modules
4. Packing Module.

The Advanced Microprocessor Bus Architecture (AMBA) defined by ARM is a widely used open standard for an on-chip bus system. This standard aims to ease the component design, by allowing the combination of interchangeable components in the SoC design. It promotes the reuse of intellectual property components, so that at least a part of the SoC design can become a composition, rather than a complete rewrite every time. The AMBA standard defines different groups of busses, which are typically used in a hierarchical fashion. The Figure 2.1 shows a schematic overview of a typical microprocessor design. The design usually consists of a system bus; either the older version the Advanced System Bus (ASB), or the more performant Advanced High-performance Bus (AHB). All high performance components are connected to the system bus. Low speed components are connected to the peripheral bus, the Advanced Peripheral Bus (APB).

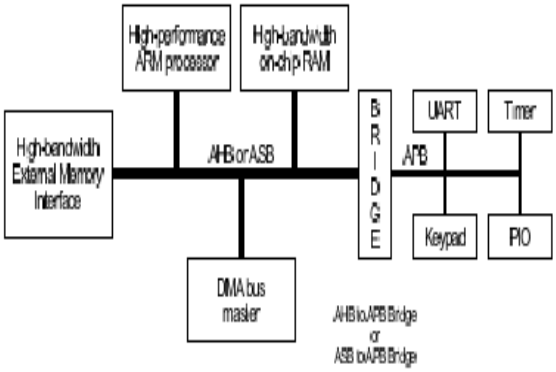

Figure 2: AMBA hierarchical bus architecture.

The system busses ASB and AHB are designed for high performance connection of Processors, dedicated hardware and on chip memory. They allow:

- Multiple bus masters
- Pipelined operation
- Burst transfers

The peripheral bus APB on the other hand is designed for low power peripherals with a low complexity bus interface.

The APB can be connected via a bridge to both system busses AHB and ASB. The APB bridge acts as a master on the APB bus and all peripheral devices are slaves.

The bridge appears as a single slave device on the system bus; it handles the APB control signals, performs retiming and buffering.

Between the two system busses the AHB delivers a higher performance than its older Counter Part ASB. The AHB features:

- Retry and split transactions
- Single clock edge operation
- Non-tristate implementation
- Allows wider data bus configuration (e.g. 64 bits and 128 bits)

Retry and split transactions are introduced to reduce the bus utilization. Both can be used in case the slave does not have the requested data immediately available. In case of a retry transaction, the master retries the transaction after and own arbitrary delay. On the other hand in a split transaction the master waits for a signal from the slave that the split transaction can be completed.

One major factor for the high performance of the AMBA system busses is the pipelined.

Access For that, each bus access is executed in three separate stages, which can overlap between Masters. The three phases for the pipelined bus access are:

Arbitration Phase

A master requests a bus access to the arbiter. The arbiter grants the access within an arbitrary number of bus cycles (at least one). Multiple masters may request the bus at the same time, however only a single master is granted at any given point in time.

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Address Phase

The granted master applies the address and control signal to the bus. The address and control signals determine the activity for the next phase.

Data Phase

Depending on the control signals from the previous phase (e.g. write direction) either the granted master or the selected slave writes the data to the data bus.

The AHB standard defines a non-tristate bus interface, which simplifies the design of the bus interfaces. It furthermore simplifies simulation of the bus system, since the costly three or four value logic - necessary for simulating a tristate interface - is not required. On the other hand, a non-tristate bus interface increases the number of connection for each bus interface; read and write bus have to be handled separately. This however is not a limiting factor, since the bus
system is targeted for on-chip connections. It does, however, require an interconnection network, in which multiplexers select the bus access for each device.

SIMULATION RESULTS:

MODE FC

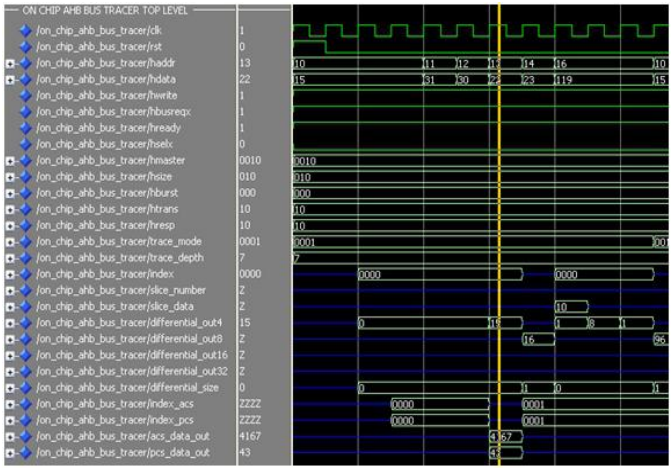

Fig 3 Simulation results of Mode FC

Simulation results of On-Chip AHB Bus Tracer with Mode FC (Mode Full Signal, Cycle by cycle) as shown in Figure .3Input signal for On-Chip AHB Bus Tracer are AMBA-AHB Bus signals which includes program address, Address /Data value and Control signals(ACS,PCS).

MODE FT

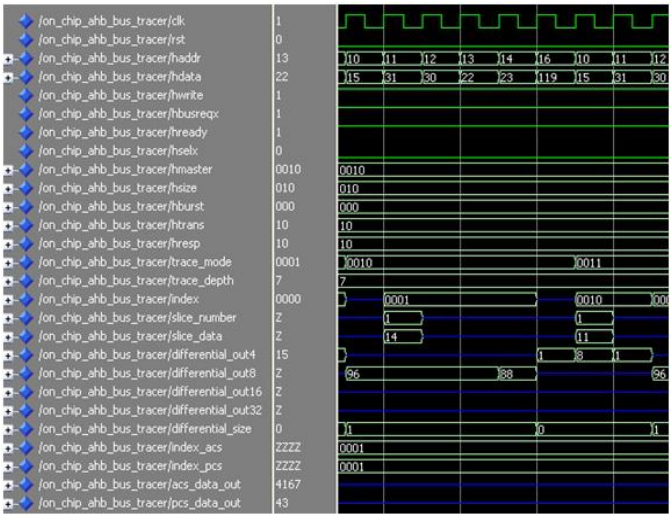

Fig 4.Simulation results of Mode FT

Simulation results of On-Chip AHB Bus Tracer with Mode FT (Mode Full Signal, Transaction level) as shown in Figure 4.Input signal for On-Chip AHB Bus Tracer are AMBA-AHB Bus signals which includes program address, Address /Data value and Control signals. Control signals includes Access Control Signals-ACS, Protocol Control Signals –PCS.

MODE BC

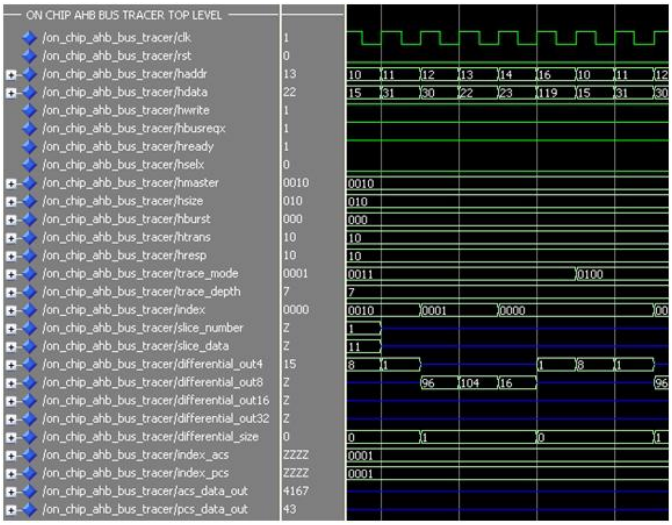

Fig 5.Simulation results of Mode BC

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Simulation results of On-Chip AHB Bus Tracer with Mode BC (Mode Bus State, Cycle level) as shown in Figure 5.Input signal for On-Chip AHB Bus Tracer are

AMBA-AHB Bus signals which includes
Program address, Address /Data value and Control signals.

Control signals includes
Access Control Signals-ACS, Protocol Control Signals – PCS.

CONCLUSION

The implementation in this paper has one event register. More registers can be added if necessary. Compared with our previous work, the gate count is reduced. The reason is that this paper optimizes the ping-pong architecture by sharing most of the data path instead of duplicating all the hardware components. As for the circuit speed, the bus tracer is capable of running at 198.515 MHz, which is sufficient for most SoC's with a synthesis approach under Xilinx Synthesis technology. If a faster clock speed is necessary, our bus tracer could be easily partitioned into more pipeline stages due to its streamlined compression/packing processing flow.