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Fine Grained CG using Stack Approach Integration of RTPG

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ABSTRACT:

In Integrated circuits a gargantuan portion of chip power is expended by clocking system which comprises of timing elements such as flip flops, latches and clock distribution network. This paper enumerates power efficient design of shift registers using D flip flops along with Clock and Power gating integration. Clock gating and power gating proves to be very effective solutions for reducing dynamic and active leakage power respectively. The two techniques are coupled in such away that the clock gating information issued to drive the control signal of power-gating circuitry. In this paper, an activity driven fine-grained clock and power gating is proposed. First, a technique named Optimized Bus-Specific- Clock-Gating (OBSC) is introduced which reduces the problem of gated flip flop selection by appropriate selection of subset of flip flops. Then another technique named Run Time Power Gating (RTPG) is proposed for power gating the combinational logics performing redundant operations. The proposed shift registers are designed up to the layout level with 1V Power supply in 0.18um technology and simulated using micro wind simulations for different clock frequencies and the performance of the shift registers are evaluated by observing the average power.

Keywords: ***Optimized Bus-Specific-Clock- Gating (OBSC), RunTime Power Gating (RTPG), microwind.***

Introduction:

With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that need to be integrated on a single chip, power density, and total power are increasing rapidly. Also, designing for low-power has become increasingly important in a wide variety of applications. However, creating optimal low-power designs involves trade such as timing versus power and are a versus power at the dierent stages of the design ow. Successful power-sensitive designs require engineers to have the ability to accurately and efficiently perform these trade.

To address these issues directly, it is essential to understand the different types and sources of power dissipation in digital Complementary Metal Oxide Semiconductor (CMOS) circuits. The reason for choosing the CMOS technology is that it is currently the most dominant digital IC implementation technology.

Power dissipation in CMOS digital circuits is categorized into two types: peak power and time-average d power consumption. Peak power is a reliability issue that determines both the chip life time and performance. The voltage drop e_ects, caused by the excessive instantaneous current owing through the resistive power network, a_ects the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and life time of the circuit. Also noise margins are reduced, increasing the chance of chip failure due to crosstalk CMOS digital circuits occurs in two forms: dynamic and static. Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, there by consuming power. Static power dissipation is associated within active logic gates (i.e., notcurrently switching from one state to another). Dynamic power is

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important during normal operation, especially at high operating frequencies, where as static power is more important during stand by, especially for battery-powered devices

For dynamic loss reduction we are using Clock Gating technique and for staticloss reduction we are suing RTPG technique explained below.

Clock Gating and Power Gating

Clockgating isapopulartechniqueusedin many synchronouscircuitsforreducing dynamicpower dissipation. Clock gating saves power by adding more logic to a circuittoprunetheclocktree.Pruningthe clockdisablesportions ofthecircuitryso that theflip-flopsin them do not have to switchstates. Switchingstatesconsumes power. Whennotbeing switched,the switchingpowerconsumptiongoes tozero, and onlyleakage currentsare incurred.[1]

Clockgating worksbytakingtheenable conditionsattached toregisters,and uses themtogate theclocks.Thereforeitis imperative thatadesignmustcontainthese enable conditionsinorder touseandbenefit fromclockgating. Thisclockgating process can alsosavesignificantdieareaaswellas power, since it removes large numbers ofmuxesandreplaces them with clock gating logic.Thisclockgating logicis generally intheformof"Integratedclock gating"(ICG)cells.However, notethatthe clockgatinglogicwillchangetheclocktree structure, since theclock gating logic will sit in the clock tree.

Power gating is a technique used in integrated circuitdesign to reducepowerconsumption, by shutting off the currenttoblocksofthecircuitthatare notinuse.Inadditiontoreducingstand-by orleakage power,powergatinghasthe benefit of enablingIddq testing.

Integrated Clock and Power Gating

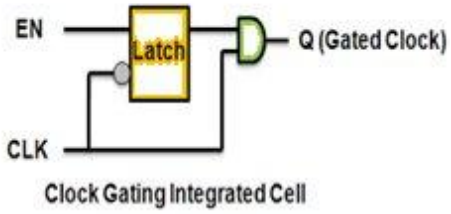
Clock GatingandPower Gatingare two most commonly used design methods to savedynamicandleakage power respectively.Howaboutintegrating thetwo solutionssuchthattheycomplement each other?Inthispost,I willtalkaboutasimple way to do so.

Clock Gating is accomplished by using ClockGatingIntegratedCell(CGIC)which gates theclocktothesequential elements present initsfan-outwhentheenablesignal islogic0.PowerGatingstructuresmaybe of two types: Simple Power Gating andState RetentionPower Gating. Using the former technique,theoutputofthelogic gatesslowly leaksthechargeattheoutput andtherebywhenthe SLEEPsignalisde-asserted,onecannotpredictthelogicvalue attheoutput.Thelattertechnique isableto retain thestateattheoutputwhichwaslast present before asserting theSLEEPsignal.

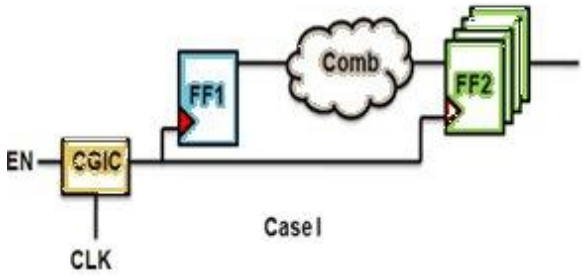
Let's take up a few plausible scenarios:

Case I

Normal Case: Whichemploys only conventional clockgating.Itisdepictedin the figure.



Clock Gating Integrated Cell



Case I

Case II

Whenonedoesnotneedtoretain thestatesofthecombinatorial cellsorthe sequential elements. One possiblescenario could be in the case of a standalone IP, whichisnotcomunicating withanyotherIP ontheSoC.Here onecanusetheesimple powergatingwhere

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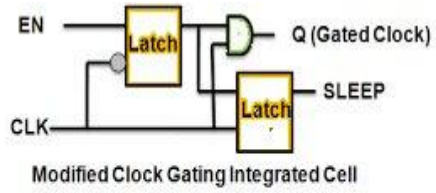
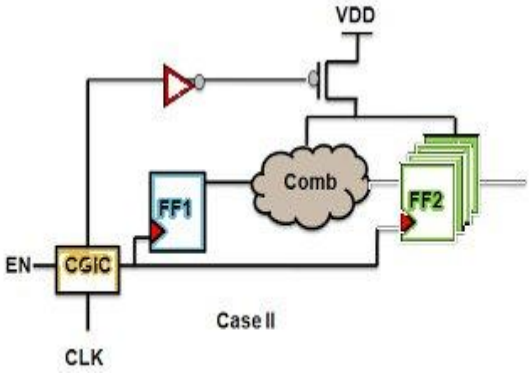
theSLEEPsignalis derivedfromtheCGICitselfusingalatch, asdepictedinthefigurebelow.Doingso, we wouldsavebothdynamicandleakage powers.



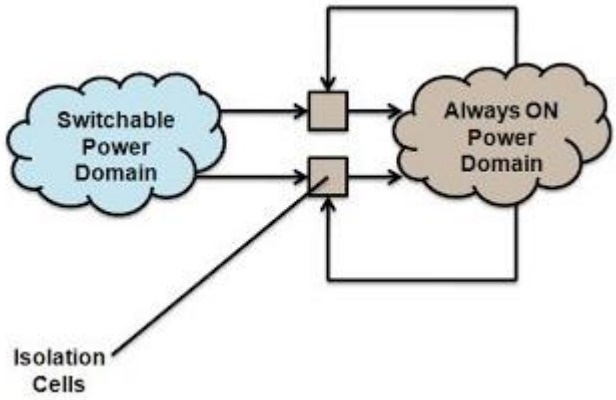


Case IIII

Whenonedoesnotneedtoretain thestatesofthecombinatorialcells,but the sequential outputsneedtobe safe-stated. Possibleuse-case couldbewhereonlythe sequentialoutputscommunicate withother IPsontheSoC.Thiscanbeaccomplished byusingStateRetentionFlipFlopsinstead of the conventional flip-flops.

Case IV

Whenboththecombinatorial cells andthesequentialcellsinteract withother IPs.But thepreviousvalue neednotbe required. Sinceitisaclassiccaseof interaction between "switchable power domain" with" always ON", it entailsthe use of isolation cells between such power domaincrossings.It mustbenotedthatin suchacase,isolationcellwouldalways be presentinthealways ONpowerdomain, i.e.,itwouldreceiveit'sVDDsupply from thealwaysONpowerdomainsupply.This isbecause,whentheswitchable power domain in OFF, the isolation cell can function only if receives the power supply!



Isolation CellscanbesimplecellslikeAND oranORgate, whichreceiveoneinputina waythat, irrespective of the second input coming fromtheswitchablepowerdomain, the value would be controllable. For example,logic0forANDgate andlogic1 foranORgate.I willtrytotakethisupina separate post.

Here weclassifiedtheshiftregistertothree places

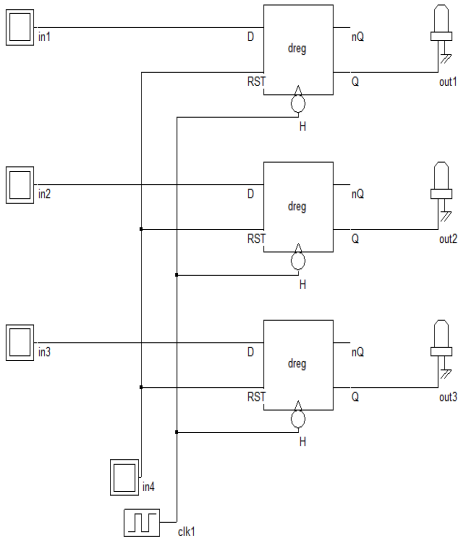


Fig: Non Clock Gating Circuit.

PROPOSED OBSC

Optimized Bus Specific Clock Gating is very effective techniquetomaximize dynamic powerreductionas showninfig.3. It choosesonlyasubsetofflip-flops(FF)to be gated selectively,and theproblem of gatedFFselectionisreduced from exponentialcomplexity intolinear.It works by comparingtheinputsandoutputsand gatestheclockwhentheyare equal[11]. Considering

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NFFsinthenon-CGcircuit, each FF can be chosen as gated or nongated. Hence,2NCGsolutionsare possibleand theexponentialcomplexity problemis reduced intolinear. Assumethat alltheFFs arechosentobegatedinitially, thentheproblem isindeterminingwhich FFs shouldbeexcludedfromgating [1]. Heuristically, theFFwiththemaximum outputdatatoggle rateshouldbeexcluded from gating first. This is because that maximumoutputdata togglerateindicates thatminimumclocktoggles willbegated, thus power willreduce least or even increase iftheFFisgated.Moreformally,theFF with themaximumoutputtoggle rateis excludedfromgating first,thentheFFwith thesecond largestoutputtoggle rateis excludedandsoon untilall theFFs are excluded(i.e., the original nonCGcircuit). Apparently, duringtheprocessofexclusion, therewillbeN+1possible CG solutions which is linear complexity.

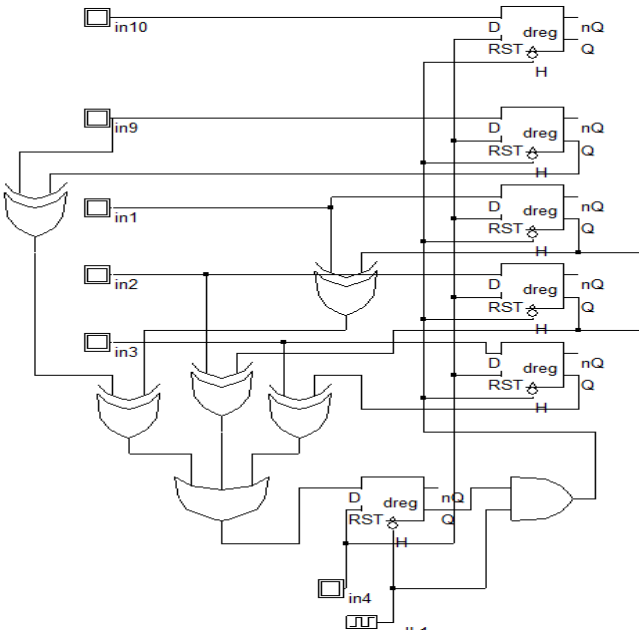

Fig: PBSC circuit

InordertoachieveintegrationofCGand RTPG, apply OBSC technique to the design, thenasubsetofFFsisclockgated. During theclockgated period,theoutputsofthe gatedFFsarestable.Consequently, those combinationallogicswhose inputsonly dependongated FFoutputswillbeinactive andcanbe power gatedasshown in Fig 6.(a).Foreachoutputof thepowergated cell,whetheraconnectiontoprimary output presence hastobechecked.A holderlogic shouldbe addedinordertoavoidsignal floating. Suppose thatfouroutoffive FFs areclockgated. Thecircledcells are completely dependentonthe stablegated FF outputs,sotheyare notactiveandcanbe powergatedintosleep[1]. However,one inputof theXORgateiistheoutputof ungatedFFA,andoneinputoftheAND gate histheprimary input.Sinceboththe ungatedFFoutputandPI maynotbestable during the clock gated period, the XOR gate iandtheANDhmaybeactive. Sothey should not be power gated. In order to avoid floating signal,aholdershouldbeplaced at theoutputofeachpowergated cell ifthat outputconnects tononpowergatedcellsor primary outputs (Pos)

If RTPGhastobeapplied,afooter(high-VthCMOStransistor)between theactual ground and virtual ground of the power gatedcellsshouldbeadded.After the integration of CG and RTPG, the low powerdesignshouldlooklikeFig.6 (b).The enable signalgenerated fromOBSCisused as thesleep signalfor thePG.The cells that aretotallydependenton gatedFFoutputs are power gated. Holdersare placed between thepowergatedcellsandthe nonpower gated cellssothatthenonpowergatedcells can function properly

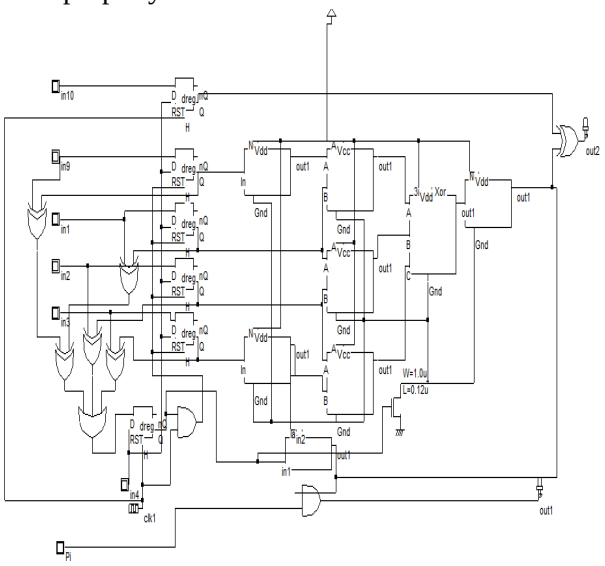

Fig: Integration of OBSC and RTPG

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Stack approach:

This is another new leakage reduction technique, which we call the stack approach.

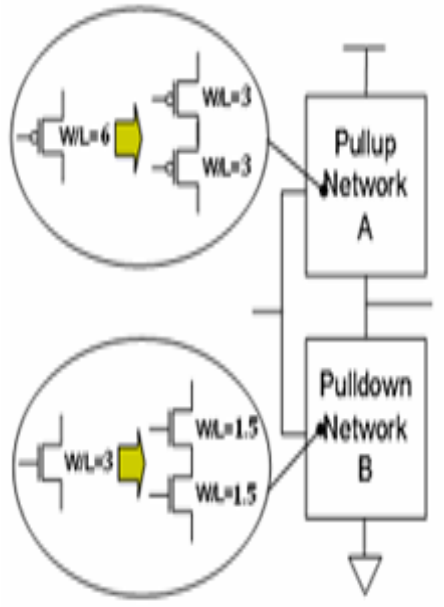

Fig: Structure ofvariablebodybiasing techniquewith sleep method

Another technique for leakage power reduction is thestack approach, which forces a stack effect by breakingdown an existing transistor into two half size transistors. When the two transistors areturned off together, induced reverse bias between the twotransistors results in sub-threshold leakage current reduction.However, divided transistors increase delay significantly andcould limit the usefulness of the approach. It divides the w/l ratio into two equal parts.

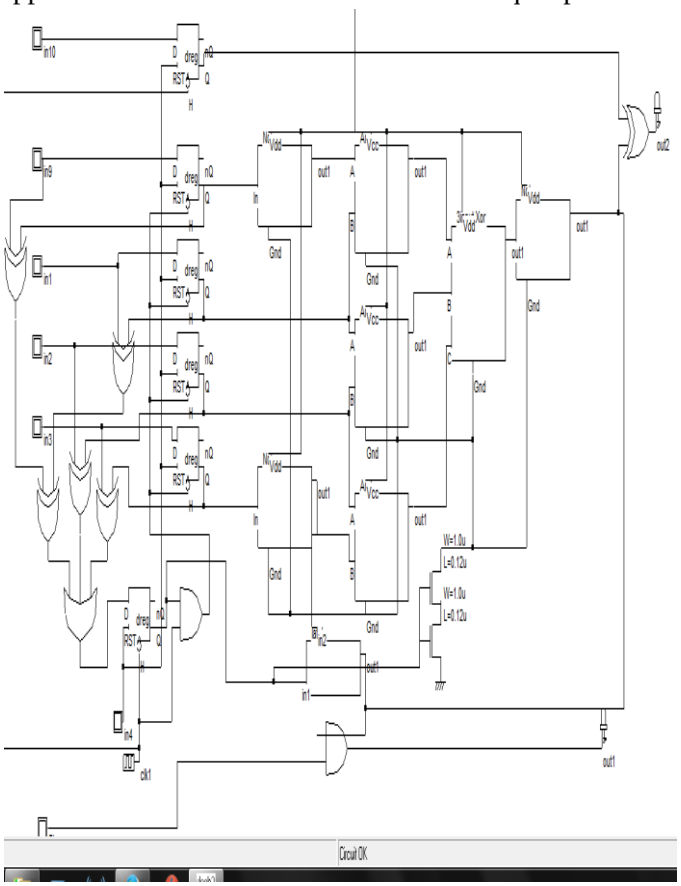

Fig: Integration of OBSC and RTPG with Stack approach

Tabulation

Circuit	Power Dissipaion
Integration of OBSC and RTPG with sleep	0.305mW
Integration of OBSC and RTPG with Stack approach	0.163mW

Conclusion:

In thisPaper,afine-grainedCGandRTPG integration isachievedinsequentialcircuits. First,anactivitydrivenfine-grained OBSC technique isevaluatedthatselects only a subsetofFFstogate.Moreover, theclock enable signalgeneratedintheOBSCcircuit canbeusedasthe

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sleepsignalinRTPG. Following this,Sequentialcircuitsthat implementsbothOBSC andRTPGis considered andtheirperformances are evaluated withsleepandstack technique.

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