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Time optimization of spread spectrum clock generator using glitch free NAND based DCDL

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Abstract:

This paper presents power optimisation of SSCG using glitchfree nand based DCDL. The recently proposed NAND-based digitally controlled delay-lines (DCDL) present a glitching problem which may limit their employ in many applications. In this proposed system we presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications.The proposed NAND based DCDL is designed by using two delay controls.Proposed DCDLs have been designed in a 90-nm CMOS technology and compared, in this technology, to the state-of-the-art. Simulation results show that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with the lowest delay. Simulations also confirm the correctness of developed glitching model and sizing strategy. As example application, proposed DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The employ of proposed DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs.

Introduction:

In deep-sub micrometer CMOS processes, the time-domain resolution of a digital signal is higherthan voltage resolution of analog signals.It leadstowards a new circuit design in which the analogsignal processing is expected to be progressivelysubstituted by the processing of times in thedigital domain. Digitally controlled delay lines(DCDL) should play the role of digital-to-analogconverters in traditional, analog-intensive,circuits.identical sub-circuit,each providing 1/N of the totaldelay.

Glitching is a common design problem insystems using DCDLs. In the most commonapplications, DCDLs are used to process clocksignals , therefore a glitch –free operation is required. A necessary condition to avoid glitching is designing a DCDL which have no –glitch inpresence of a delay control-code switching.In this paper we are going to discuss about glitch frreNAND based DCDL and its implementation on SSCG. The rest of this paper is organized in the following manner: Section II Previously Proposed NAND-Based DCDL. Section III Proposed NANDBasedDCDL. Section IV. Application to All-Digital SSCG. Section VI. SSCG Architecture.

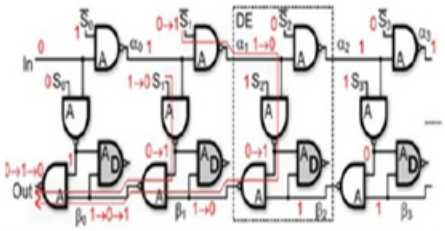

Figure1: Glitching problem of NAND-based DCDL, glitching when the delay control-code increases by one

Fig. 1 shows the NAND –based DCDL. The circuit is composed by a series of equal delay –elements (DE), each composed by four NAND gates . In the figure "A" denotes the fast input of each NAND gate. Gates marked with "D" are dummy cells added for load balancing. The delay of the circuit is controlled through control-bits Si , which encode the delay control-code c with athermometric code Si=0 : for i<c, and Si=1 fori>=c . By using this encoding, each DE in Fig. 1can be either in pass-state (Si=0) or in turn-state(Si=1). In Fig. 1(a) all NAND gates present thesame load and, therefore, in a first orderapproximation, present the same delay. This consideration allows to write the delay _ , from In to Out, as follows:_=2tNAND + 2tNAND . C (1) Where tNAND =(tNAND LH + tNAND HL) /2while tNANDLH and tNAND HL represent the delay ofeach NAND gate for a low-to-high and high-tolowoutput

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commutation, respectively.Equations(1) suggests that tmin=2tNAND and tR=2tNAND.To avoid DCDL output glitching, the switchingof delay control-bits is synchronized with the switching of In input signal. Glitching is avoided if the control- bits arrival time is lower than the arrival time of the input signal of the first DE which switches from or to the turn-state.

Let us name S=[S0,S1,….] the vector of the control-bits of the DCDL. In Fig. 1 it is assumed that In =0 and that the control-code c of the DCDL is switched from 1 (S=[0,1,1,1…]) to 2 S=[0,0,1,1,….]) .The switching of S1 and S1 bar results in two different paths that generate an output glitch. It can be easily verified that the same glitching behavior exists when input In is 1.

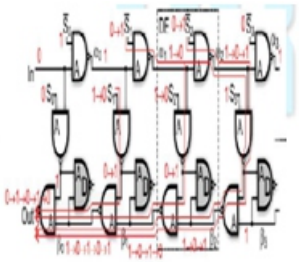

Figure2 Glitching problem of NAND-based DCDL, glitching when the delay control-code increases by Two

Fig.2 shows that the structure exhibits a more severe glitching problem when the delay controlcode is increased by more than 1. The Fig. 2 shows the case in which control-code of the DCDL is switched from 1 (S=[0,1,1,1,….]) to 3(S=[0,0,0,1,…]). The analysis of the figure, in this case, reveals that, four paths propagate within the DCDL structure and may create a multiple-glitch at the delay-line output.

The glitching problem of NAND-based DCDL grows up because, for a control-code equal to c, all _i and _i signals in figure 1 and 2 with i_c, areat stuck- at 1, while for i<c the logic state of _i and _i signals depends on the input In.

When the control-code is increased, the logic state of the output becomes dependant on a portion of the DCDL for which _i and _i switch from 1 to a logic state dependant on In. This switching may determine output glitches. This consideration also demonstrates that no glitching can occur when the control-code is decreased.

3. Proposed NAND-Based DCDL:

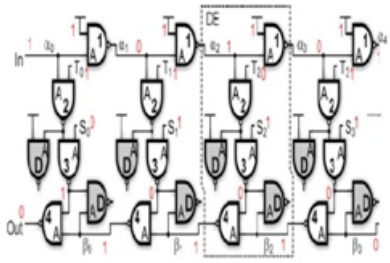

Figure3 Proposed glitch-free NAND-based DCDL (inverting topology).

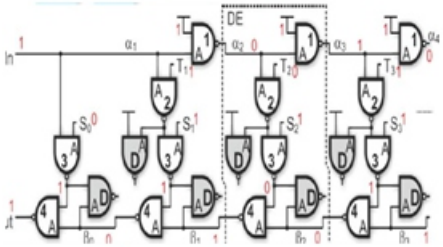

Figure 4 Proposed glitch-free NAND-based DCDL (non-inverting topology.

The structure of proposed DCDL is shown in Fig. 3 and 4. In this Figure , “A” denotes the fast input of each NAND gate. Gates marked with “D”, represents dummy cells added for load balancing. Two sets of control-bits, Si and Ti, control the DCDL. The Si bits encode the control-code c by using a thermometric code Si =0: for i<c and Si =1 for i _c . The bits Ti encode c again by using a one-cold code: Tc+1=0, Ti =1 for i_c+1.The Fig. 8 shows the state of all signals in the case In=1,c=1. According to the chosen control-bits encoding, each delay-element (DE) can be in one state.

Logic-States of Each De in Proposed DCDLS

S_i	T_i	Delay Element State
0	1	Pass
1	1	Turn
1	0	Post-Turn

The DEs with i<c are in pass-state (Si=0 ,Ti=1). In this state the NAND “3” output is equal to 1 and the NAND “4” allows the signal propagation in the lower NAND gates chain.

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The DE with i=c is in turn-state (Si=Ti=1). In this state the upper input of the DE is passed to the output of NAND "3" . The next DE (i=c+1) is in post-turn-state (Si=1 ,Ti=0) . In this DE, the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4".

All remaining DEs (for i>c+1) are again in turn-state (Si=Ti=1). The three possible DE states of proposed DCDL and the corresponding Si and Ti values are summarized in Table I. The circuit of Fig. 3 is an inverting DCDL. In this circuit the first DE is never in post-turn state, therefore to is always 1. The Fig 4 shows a non-inverting DCDL by modifying only the first DE. In this circuit the NAND gates "1" and "2" of the first DE have been deleted, together with signal To . The signal α1 of the second DE is now equal to In, therefore the whole behavior of the DCDL is non-
inverting. This topology maintains the same tR of previous solution.

4. Application to an All-Digital Spread Spectrum Clock Generator:

To verify the usefulness of proposed solutions in a real application, the All-digital spread-spectrum clock generator (SSCG) has been redesigned by using proposed DCDL. Spread spectrum clocking is an effective solution to reduce the electromagnetic interference produced by digital chips, using a clock signal with a frequency that is intentionally swept(frequency modulated) within a certain frequency range, with a predefined modulation profile.

There duction of the electromagnetic interference produced by digital chips has become nowadays an important design issue, due to the widespread use of digital processing techniques in consumer applications and due to the steadily increase of their operating frequency.

The clocks employed in digital chips, in fact, radiate electromagnetic noise over a wide frequency band, which may interfere with other electronic equipments in the neighborhood. Spread spectrum clocking (SSC), also known as "clock dithering", is an established, cost effective, technique to reduce the EMI level.

generates a clock signal with a frequency that is intentionally swept (frequency modulated) within a certain frequency range, with a predefined modulation profile. SSC does not actually reduce the total power of the harmonic noise but, instead, it spreads the energy of each clock harmonic evenly over a dedicated bandwidth. In this way the peak power level at each clock harmonic is reduced as much as 10–20 dB, depending on the modulation depth and the modulation profile.A spread spectrum clock generator (SSCG) is commonly implemented with a phase-locked loop (PLL), with an appropriate frequency-modulated output. This approach use many analog blocks, which require major redesign when the technology scales down. Moreover, analog techniques do not fully exploit the speed and power improvements of CMOS processes. Finally, the bandwidth of PLL based techniques is usually limited and does not easily allow the generation of clocks with a large modulation frequency.

5. SSCG Architecture:

The top-level block diagram of the all-digital spread spectrum clock generator is shown in Fig 12. The system has an input clock signal (CLK) having a constant period TCK=1/fCK. and generates an output clock waveform , whose instantaneous period is given by TOUT(t)=TO +_T . h(fmt)

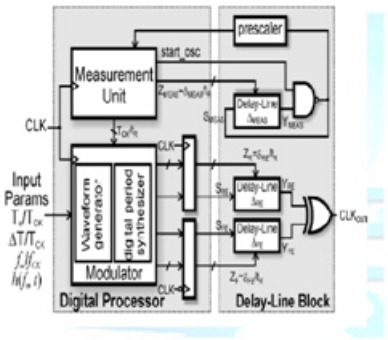

Figure 5 Architecture of spread spectrum clock generator.

Where TO is the nominal output period ,_T is the modulation amplitude, fm is the modulation frequency and the function h(fmt) represents the modulation profile. The function is user defined and is given by o_ h(fmt) _ 1 (3)The instantaneous frequency of the output waveform, for an ideal down spreading modulation, is given by fideal(t) = fo- _f .

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h(fmt) (4)The SSCG in Fig. 5 is generally composed of a digital processor and a delay-line block, includingtwo digitally controlled delay-lines (DCDLs), named_RE and _FE . A third replica DCDL_MEAS ,closed in a ring-oscillator topology, drives ameasurement unit and is employed to compensateprocess, voltage, and temperature (PVT) variations.Each DCDL is driven by an input S signal andproduces an output signal Y . The delay between Yand S is controlled through a digital input Z. The digital processor receives as inputs: the period of output signal normalized to the clock period.

The digital processor receives as inputs: the period of output signal normalized to the clock period (TO/TCK) , the normalized modulation frequencyfm/fCK , the normalized modulation amplitude_T/TCK and also the user defined modulation profile h(fmt).We are using the input clock signalwhich has 50% duty-cycle and the SSCG is able to generate a clock signal with a frequencyfo_ fCK .The output waveform signal is generated in the delay-line block.

The delay-line_RE is driven on the rising edge of the input clock and can generate an output edge in a timing window of length TCK/2 starting from the input clock rising edge. The delay-line_FE can generate an output clock edge ina timing window of length TCK/2 starting from the falling edge of the input clock signal. The XOR gate merges the two wave forms produced by the two delay lines and generates the output signal CLKOUT. In this way the modulator is able to position the output clock edges anywhere in the time axis.

A.Modulator:

1)Wave formGenerator:

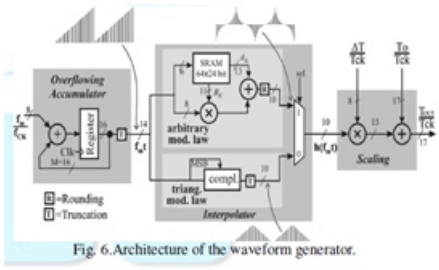


Fig. 6.Architecture of the waveform generator.

Fig. 6 shows the architecture of the waveform generator.

It is used to compute the desired instantaneous period of the output waveform, normalized to the clock period: TOUT /TCK. An M-bit overflowing accumulator is used to generate a saw tooth waveform with a frequency fm. accumulator corresponds to the argument fmt of the function h, and is truncated to 14 bits to simplify the interpolator implementation. From a practical point of view, there is no use to have a modulation frequency much larger than the maximum Resolution Bandwidth (RBW-1 MHz) considered in EMI standards. So the number of input bits used for fm/fCK is limited to 8. The interpolator in Fig. 6 is able to generate anarbitrary waveform h(fmt).It is to be noted that interpolator can be largely simplified if only triangular modulation profile is required. In this case, in fact, the SRAM, the multiplier and the adder can be eliminated from the circuit and replaced by a 1's complementer. 2.Digital Period Synthesizer: The digital period synthesizer generates the input signals for the two delay lines _RE and _FE. It is obtained with the help of a finite state machine (FSM). The outputs of the FSM (WF and WR) drive the two delay lines _RE The modulation frequency is set with a precision of fCK /2Mby using the control word fm/fCK . In this design M=16.The output of the overflowing.

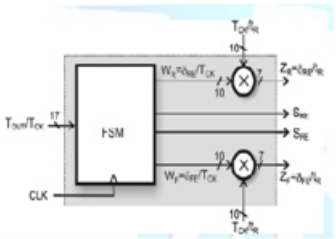
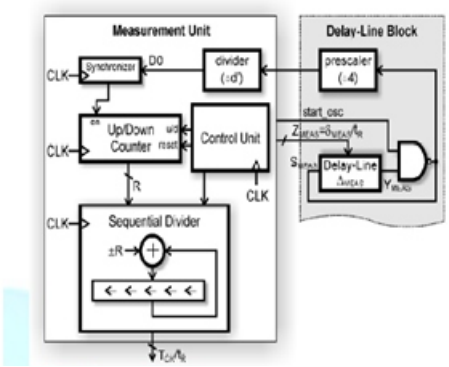


Fig. 7.Arcl synthesizer.

B. Measurement Unit:

The actual resolution of the DCDLs (tR) depends on process, voltage, and temperature. In order to compensate PVT variations, the measurement unit



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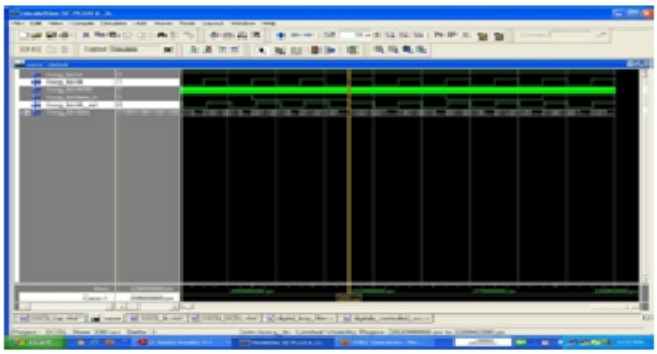
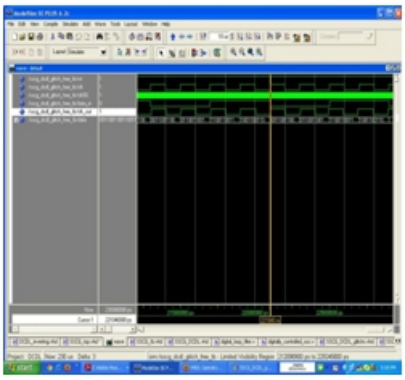
ontinuously measures the ratio TCK/ tR and sends the value of this parameter to the modulator block The measurement unit is shown in Fig. 8.The DCDL _MEAS is a replica of the DCDLs _RE and _FE employed to generate the output waveform. When the Signal start_oscis high, _MEAS becomes part of a ring oscillator including also the NAND gate. The oscillation period can be written as TOSC= 2(tmin +ZMEAS .tR +tNAND) (5) where tmin is the minimum delay through _MEAS and tNANDis the delay of the NAND gate. Delay

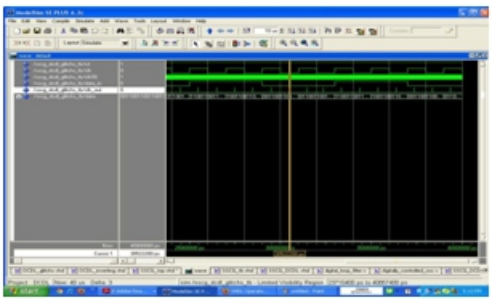
1.SSCG DCDL GLICTH FREE:



2. SSCG DCDL GLICTH FREE 1:

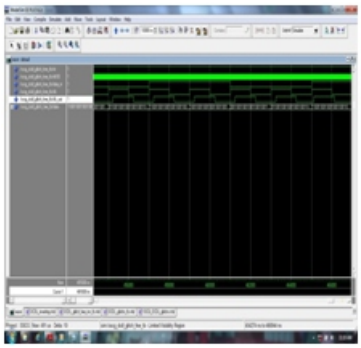


3. SSCG DCDL WITH GLITCH:



4. SYCHRONISED WITH INPUT CLOCK :

5. UNSYCHRONISED :



6. Conclusion:

A glitch free NAND-based DCDL avoids the glitching problem of previous circuit .It also provides the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. This DCDL is used to realize an all-digital SSCG. The use of proposed DCDL in this circuit allowed to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to an SSCG

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