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Hardware Implementation of OFDM Transmitter and Receiver Using FPGA

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ABSTRACT:

Orthogonal frequency division multiplexing (OFDM) Will be the majority of guaranteeing modulation method. It has been adopted by most remote and wired correspondence models. The prospect is to use several carriers, spread frequently over a frequency band; to the extent therefore the particular accessible bandwidth is used to maximal efficiency. The specific objective with this document is typically to handle an efficient implementation of the OFDM frame (i.e. at the transmitter and receiver) utilizing "Field Programmable Gate array (FPGA)" and discover the actual result by means of simulating all of the blocks utilized in suggested challenge employing QuartusII & Modelsim simulation tool.

Keywords:

OFDM, FPGA,MODELSIM.

1.INTRODUCTION:

The particular OFDM is the modulation strategy possessing multicarrier signal techniques. Below this obtainable spectrum is actually split in to a lot of carriers as well as everyone becoming modulated at the low rate data stream. This removing between the carriers is actually close up and the carriers are orthogonal to each other keeping this interference between the nearly spaced carriers. As a result OFDM is actually a combination of modulation as well as multiplexing methods. Every single carrier in the OFDM signal provides extremely narrow bandwidth. Therefore the resulting symbol rate is low. That is the signal provides large tolerance to be able to multipath delay spread minimizing the possibility inter symbol interference (ISI). This can be need in now day's communication systems.

OFDM is actually quite similar seeing that FDM however a lot more spectrally effective by using spacing ones sub-channels quite definitely deeper with each other (until these are with genuinely overlapping). This can be performed by using discovering frequencies which may be orthogonal, implying they are perpendicular with respect in the mathematical sense, letting this spectrum of each and every 1 sub-channel to be able to overlap yet another devoid of interfering about it. Inside fig 1.1 the end result with this is viewed, since the necessary bandwidth is actually automatically decreases caused by removing guard bands (which seen in FDM) as well as allow signals to overlap.

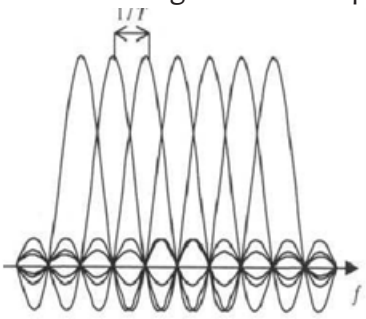

Figure 1.1 spectrum overlap in OFDM

The genuine secret to OFDM could be keeping orthogonality while using carriers. if the important associated with a result of 2 signals is going to be actually zero crossing an time span, along these kinds of traces both the of the signals are usually regarded as orthogonal to one another. A couple sinusoids using frequencies which were integer multiples of any common frequency can easily match this specific qualifying criterion. so, orthogonality can be seen as an.

$$\int_0^T \cos(2\pi nfot)\cos(2\pi mfot)dt=0 \qquad (n\neq m)$$

In which n along with m tend to be the two unequal integers;fo can be the standard frequency ;T could be the time period over that the integration can be obtained. Regarding OFDM, T can be the one symbol period and fo set to 1/T for maximum effectiveness.

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B. Field programmable gate array (FPGA):

These days a logic circuit along with 20000 gates can be regular. In order To execute huge circuits, it can be advantageous to utilize a kind of processor which has a huge logic capability. A field-programmable gate array (FPGA) is a programmable logic device that will support usage of moderately huge logic circuits. FPGA is not quite the same as different logic systems similar to CPLD along with SPLD. Fact that FPGA will not include AND as well as OR planes. Rather, FPGA includes logic obstructs with regarded to executing necessary characteristics.

A FPGA includes 3 fundamental verities of methods: logic obstructs, I/O obstructs to be able to plug towards pins in the package, in addition to interconnection wire connections in addition to switches. The logic blocks tend to be sorted inside a two-dimensional array, as well as the interconnection wires tend to sorted side by side and up and down routing channels between lines and segments of logic obstructs [5].

The routing channels contain wires and programmable switches that will enable the logic obstructs for being interconnected in numerous points. FPGA can be utilized to logic circuits of more than a couple of hundred thousand equivalent gates in size [5]. Figure 1.2gives a clear picture of the FPGA outline stream.

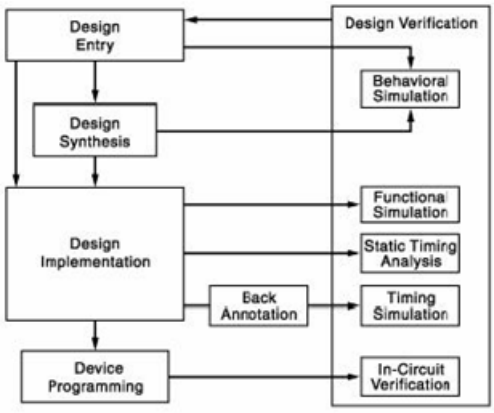

Figure 1.2 FPGA design flow

II. PROPOSED SYSTEM

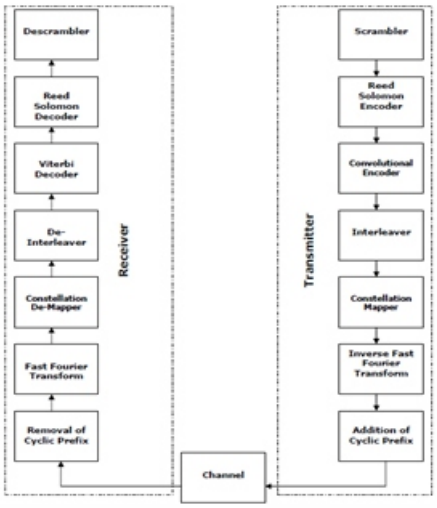

Fig.1.3.Complete OFDM system

1. SCRAMBLER/DESCRAMBLER:

Data bits pick up towards the transmitter while inputs. Most of these bits move across a scrambler in which randomizes the particular little series. It is carried out to make the data series much distributed in order that the reliance associated with info signal's energy range around the real sent information could be wiped out. For the receiver conclusion descrambling would be the final stage. De-scrambler essentially recuperates unique data bits from the scrambled bits.

2 .REEDSOLOMON ENCODER/DECODER:

The scrambled parts are subsequently maintained towards Reed Solomon Encoder a section of forward Error correction (FEC). Reed Solomon code is definitely a miscalculation modification code procedure. Enter files can be over-sampled in addition to parity representations are determined that appended with original data to be [3]. Like this repetitive chunks tend to be included with the specific message which gives protection opposition to extreme channel circumstances. A new Reed Solomon code can be spoken for you to within the framework RS (n, k), exactly where

$$n = 2m-1 \qquad 1.1$$

$$k = 2m-1-2t \qquad 1.2$$

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right Here m will be the amount of chunks for every symbolic representation, k can be the amount of input information symbols (to be encoded), n may be the final amount connected with symbols (data + parity) in the RS codeword along with t will be the greatest amount of information symbols that can be rectified. At the receiver Reed Solomon coded symbols are de-coded by eliminated parity symbols.

3. CONVOLUTIONAL ENCODER/ DECODER:

Reed Solomon error-coded parts tend to be even more coded through Convolution encoder. This kind of contributes included with repetitive chunks also. Throughout this coding approach every m little symbol will be developed straight into a good n little symbol; m/n is recognized as your code rate. That change associated with m bit symbol straight into tad symbol relies on the final k information symbols; consequently k is called as the constraint length of the Convolution code Viterbi algorithm is used for you to decode convolutionaly encoded bits at the receiver side. Viterbi decoding formula will be best option for Convolution codes along with k ≤10.

4. INTERLEAVER/ DE-INTERLEAVER:

Interleaving is completed to ensure the information through burst errors throughout transmitting. Thoughtfully, the particular in-coming tad flow will be re-arranged to ensure that surrounding chunks tend to be no longer next to one another. The information will be damaged straight into obstructs and also the chunks inside a obstruct are re-arranged. Discussing as far as OFDM, the chunks inside an OFDM symbol are re-organized in such a manner thus, to the point that nearby bits are put on non-adjacent sub-carriers. The extent that De-Interleaving is involved; the idea once more rearranges the particular chunks straight into unique style throughout reception.

5. CONSTELLATION MAPPER/ DE-MAPPER:

The particular Constellation Mapper essentially routes the approaching (interleaved) bits up on distinctive sub-carriers. Distinctive modulation strategies may be utilized, (for example, QPSK, BPSK, QAM and so on.) with regarded to distinctive sub-carriers. The De-Mapper basically removes chunks from the modulated symbols at the receiver.

6. INVERSE FAST FOURIER TRANSFORM/ FAST FOURIER TRANSFORM:

It is the most promising obstruct over OFDM frame. Because IFFT that fundamentally provides OFDM its orthogonality [1]. The IFFT transform is a range (amplitude and phase of each component) into a time domain signal. It changes over various complex data points into the same number of points in time domain. Essentially, FFT at the receiver part works the opposite assignment.

7. ADDITION/ REMOVAL OF CYCLIC PREFIX:

As a way to sustain the sub-carrier orthogonality plus the independence associated with succeeding OFDM designs, a new cyclic guard time period can be launched. This guard time period can be indicated regarding the particular portion associated with the amount of the samples comprise an OFDM designs. The cyclic prefix includes a copy of the end of the approaching symbol addition of cyclic prefix brings about circular convolution between the transmitted signal and the channel impulse response. Removal of cyclic prefix is then fed at the receiver end.

III. SPECIFICATION OF TRANSMITTER & RECEIVER:

Figure 1.3 shows a complete OFDM correspondence frame work.. Output of the transmitter is fed to the host PC via the serial port and also to the OFDM receiver. Specifications are listed below:

- OFDM with 64 sub-carriers (all data sub-carriers)
- All the sub-carriers are modulated using QPSK
- IFFT: 64-point. Implemented using FFT radix 22

Algorithm:

- Channel coding: Reed Solomon code + Convolution code
- Reed Solomon Encoder: RS (15, 9)
- Convolution Encoder: m=1, n=2, k=7. Code rate = ½

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• Block Interleaver and 1/8 Cyclic Prefix

IV.RESULTS

A.SCRAMBLER

To verify proper functioning of the Scrambler was initially fed with a seed value of 1110101 and the following input bit stream was given to the Scrambler:

In: 0110101000

The output was:

Out: 1101110001

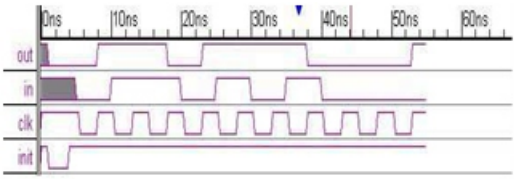

Fig 1.4. Simulation result of scrambler

After a dry run of the scrambler using high-level modeling in Verilog it was verified that the output was correct.

B.REEDSOLOMON ENCODER

In order to check the proper functioning of Reed Solomon Encoder a test bench was written in Verilog. The input given to the encoder through the test bench was a string of alternating 36 (9 symbols) bits starting with 0. Such that:

In: 555555555H

It is well known in the art that if all the input symbols to a Reed Solomon encoder are identical, then the parity symbols will all be identical as well and will be equal to the input symbols. Therefore, the output turned out to be

Out: 555555555555555H

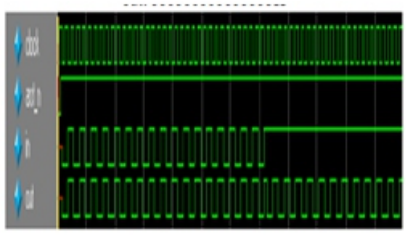

Fig 1.5 simulation result of reedsolomon encoder

Other input combinations were also given and desired results were achieved that verified proper functioning of the Encoder.

C.CONVOLUTIONAL ENCODER:

After simulation of the above shown Verilog code the following waveform was generated. It can be seen that first of all a low pulse was given to the arst_n (reset) input in order to initialize the shift register with all zeroes. Next the following bit stream was given at the input,

In: 1011101

The output turned out to be,

Out: 11010001011100

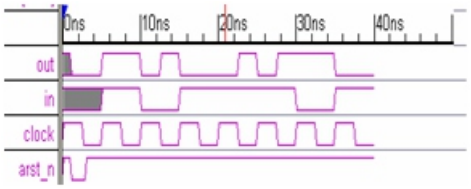

Fig 1.6 simulation results of convolution encoder

For a 7 bit input a 14 bit output is generated. Once again this circuit was taken through a dry run using high level modeling in Verilog and the results were verified.

D.INTERLEAVER:

The waveform for the interleaver goes up to 128 clock cycles. Therefore, it is not shown here. For an input block of data containing alternate 1s and 0s the output was

Out: 00000000111111110000000011111111000000000……..so on

This clearly shows how bit positions have been changed.

E.CONSTELLATION MAPPER:

Following wave form shows that when an input of 10 was given to the Constellation Mapper the output was,

Out: 00b504ff4afch

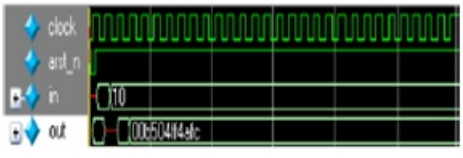

Fig 1.7 simulation results of constellation mapper

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F.IFFT:

The IFFT was tested by giving the following 64 complex data points,
h00b504000000,h030000000000,h00b504000000,…, h00b504000000 which is equivalent to 0.707, 3, 0.707,…, 0.707

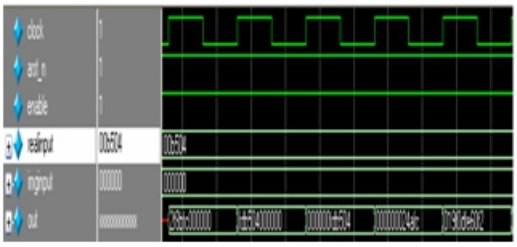

Fig 1.8 simulation results of IFFT.

The outputs were h2f8bc000000, h5db504000000, h0000005db504 and so on. On verification with mat lab the results turned out to be correct.

G.CYCLIC PREFIX ADDER:

The inputs given to the cyclic prefix adder were
47'h000001001 01, 47'h000010100001, 47'h001110100101, 47'h110010100101, 47'h000010100101,47'h010101000101, 47'h011110100101, 47'h000011100101. . .
47'h000011100101
The outputs turned out to be
47'h000011100101, 47'h000011100101, 47'h000011100101, 47'h000011100101, 47'h000011100101, 47'h000011100101, 47'h000001001 01, 47'h001110100101, 47'h110010100101, 47'h000010100101,47'h010101000101, 47'h011110100101, 47'h000011100101. . .
47'h000011100101
Note that the first eight outputs are actually the last eight inputs and the rest of the output points are same as the inputs. The following waveform shows the same.

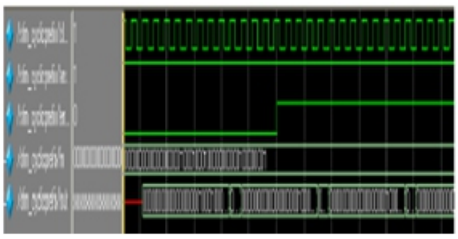

Fig1.9 simulation results of cyclic prefix adder

H.CONSTELLATION DE-MAPPER:

The constellation de-mapper basically maps the incoming QPSK constellation points to actual data. On the following inputs:
h00b50400b504 (which is 0.707 + j0.707)
And hFF4AFC00B504 (which is -0.707 + j 0.707)
The outputs turned out to be, 00 and 01

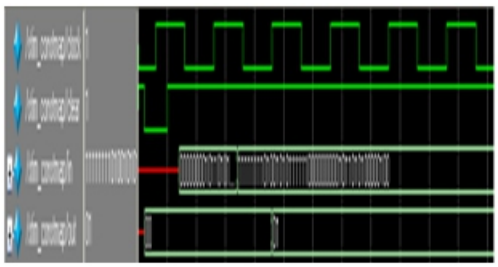

Fig1.10 simulation results of constellation de-mapper

I.DE-INTERLEAVER:

Just like the interleaver the simulation waveform of de-interleaver extends to 128 cycles so can't be shown here.

J .DE-SCRAMBLER:

The inverse of scrambling is done by the De-Scrambler. For the input,

b111111111000000000

The output was,

b110111111111000010

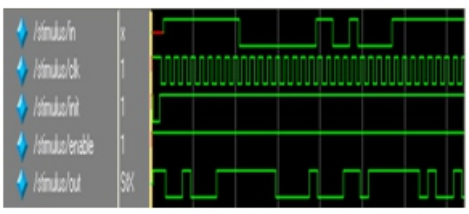

Fig 1.11 simulation results of de scrambler

V. CONCLUSION:

Orthogonal Frequency Division Multiplexing (OFDM) both transmitter as well as receiver have been design utilizing Quartus II tool as well as Simulation carried out` using Altera Modelsim simulation tool..

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Verilog is utilized to Hardware Description Language (HDL) to program each and every component of the OFDM Transmitter as well as Receiver and verification of functionality of all components has done by giving different input and output is verified. It is also found out that how many number of logic elements and memory bits are required to design each component.

REFERENCES:

[1] Ahmed R. S. Bahai and Burton R. Saltzberg, 'Multi Carrier Digital Communication". Kluwer Academic Publishers, 2002.

[2] G.M. Bhat, M. Mustafa, Shabir Ahmad and Javaid Ahmad "modelling and simulation of data scrambler and descrambler for secure data communication", Indian Journal of Science and Technology 2009.

[3] Dapeng Hao, Pin Yao, and Peter Adam Hoeher "Analysis and Design of Interleaver Sets for Interleave-Division Multiplexing and Related Techniques" 5th International Symposium on Turbo Codes and Related Topics 2008".

[4] Doelz, M.L., Heald E.T. and Martin D.L. "Binary Data Transmission Techniques for Linear Systems." Proc. I.R.E., 45: 656-661, May 1957.

[5] Aseem Pandey, Shyam Ratan Agrawalla & Shrikant Manivannan, "VLSI Implementation of OFDM", Wipro Technologies, September 2002.