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A Novel Design for carry skip adder using purity preserving reversible logic gates

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Abstract:

The reversible logic is a most popular and emerging field in low power consideration. It will be having many applications in quantum computing, nanotechnology and optical computing etc. This proposes the design of efficient fault tolerant carry skip adder/subtractor. Design of carry skip adder/subtractor requires full adder/subtractor and parallel adder/subtractor those designs also included in this paper. In this paper all the designs are efficient in terms of gate count, constant input, garbage output and quantum cost.

Keywords:

Reversible Logic Gates, Parity Preserving Reversible Logic Gates.

I. INTRODUCTION :

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Part of the problem of energy dissipation is related to technological non- ideality of switches and materials. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The other part of the problem arises from Landauer's principle [1] for which there is no solution. Landauer's principle states that logic computations that are not reversible necessarily generate kT * log 2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. For room temperature T the amount of dissipating heat is small (i.e. 2.9 * 10 Joules), but not negligible. This amount may not seem to be significant, but it will become relevant in the future. Consider heat dissipation due to the information loss in modern computers. First of all, current processors dissipate 500 times this amount of heat every time a bit of information is lost.

Second, assuming that every transistor out of more than 4 * 10 for Pentium-4 technology dissipates heat at a rate of the processor frequency, for instance 2 GHz (2*10Hz), the figure becomes 4 * 10 * kTln 2 J/sec. The processor's working temperature is greater than 400 degrees Kelvin, which brings us to 24 * 10 k ln 2. Although this amount of heat is still small (k ≈1.38 * 10), i.e. only around 0.1 W, Moore's law predicts exponential growth of the heat generated due to the information loss, which will be a noticeable amount of heat loss in the next decade. A more accurate (verified in parts with Intel's principal engineer Jason C. Stinson) heat dissipation due to the information loss calculation for the Madison Itanium-2 processor showed the figure of at least 0.147 W when the processor is fully loaded. Design that does not result in information loss is called reversible.

It naturally takes care of heating generated due to the information loss. Bennett [2] showed zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Quantum computations are known to solve some exponentially hard problems in polynomial time. All quantum computations are necessarily reversible. Therefore research on reversible logic is beneficial to the development of future quantum technologies: reversible design methods might give rise to methods of quantum circuit construction, resulting in much more powerful computers and computations. Most gates used in digital design are not reversible. For example the AND, OR and EXOR gates do not perform reversible operations. Of the commonly used gates, only the NOT gate is reversible. A set of reversible gates is needed to design reversible circuits. Several such gates have been proposed over the past decades. Among them are the controlled-not (CNOT) proposed by Feynman [4], Toffoli, and Fredkin [5, 6] gates. These gates have been studied in detail. However, good synthesis methods have not emerged.

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Shende suggest a synthesis method that produces a minimal circuit with up to 3 input variables. Iwama describe transformation rules for CNOT based circuits. These rules may be of use in a synthesis method. Miller uses spectral techniques to find near optimal circuits. Mishchenko and Perkowski suggest a regular structure of reversible wave cascades and show that such a structure would require no more cascades than product terms in an ESOP (exclusive or" sum of products) realization of the function. In fact, one would expect that a better method can be found. The algorithm sketched in has not been implemented. A regular symmetric structure has been proposed by Perkowski to realize symmetric functions.

The reversible logic design algorithms will be considered in the Literature Traditional design methods use, among other criteria, the number of gates as a complexity measure (sometimes taken with some specific weights reflecting the area of the gate). From the point of view of reversible logic we have one more factor which is more important than the number of gates used, namely the number of garbage outputs.

Since reversible design methods use reversible gates, where the number of inputs is equal to the number of outputs, the total number of outputs of such a network will be equal to the number of inputs. The existing methods use the analogy of copying information from the input of the network, therefore introducing garbage outputs information that we do not need for the computation. In some cases garbage is unavoidable. For example, a single output function of n variables will require at least n-1 garbage outputs, since reversibility necessitates an equal number of outputs and inputs.

II. REVERSIBLE LOGIC GATES Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. More formally, a reversible logic gate is a k-input, k-output (denoted k*k) device that maps each possible input pattern into a unique output pattern. While constructing reversible circuits with the help of reversible gates, some restrictions should be strictly maintained [3, 4]:

- Fan-out is not permitted.

- Loops are not permitted. In reversible logic we have one more factor, which is more important than the number of gates used, namely the number of garbage outputs. The unutilized outputs from a reversible gate/ circuit are called "garbage".

Though every synthesis method engages them producing less number of garbage outputs, but sometimes garbage outputs are unavoidable. For example, a single output function of n variables will require at least n-1 garbage outputs, since the reversibility necessitates an equal number of outputs and inputs. Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions. 1. Firstly, in reversible logic circuit the number of inputs must be equal to the number of outputs. 2. Secondly, for each input pattern there must be a unique output pattern. 3. Thirdly, each output will be used only once, that is, no fan out is allowed. 4. Finally, the resulting circuit must be acyclic.

A. Parity Preserving Reversible Logic Gates BehroozParhami [7] proposed that reversible hardware computation, that is, performing logic signal transformations in a way that allows the original input signals to be recovered from the produced outputs, is helpful in diverse areas such as quantum computing, lowpower design, nanotechnology, optical information processing, and bioinformatics. In a parity preserving reversible logic gates the output parity will matches with the input parity (i.e. ex-or's of outputs is equal to the ex-or's of input). There exist several parity preserving reversible logic gates in literature Fredkin gate, Feynman double gates are few among them. In this paper Fredkin gate, Feynman double gate and Modified Islam gates are used. By using these parity preserving reversible logic gates it is easy to design fault tolerant circuits.Fredkin Gate (FRG): Fredkin Gate (FRG) [5] is a 3*3 gate shown in Figure 1. It has A, B and C input vector and output vector as P=A, Q=A'B AC and R=A'C AB. Quantum cost of Fredkin gate is 5.

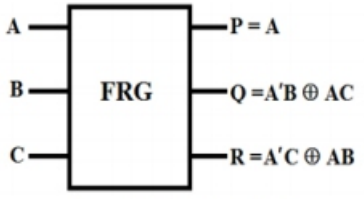

Figure 1 Fredkin Gate (FRG)

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Feynman Double Gate (F2G): Feynman Double Gate (F2G) [4] is a 3*3 gate shown in Figure 2. It has A, B and C input vector and output vector as P = A, Q = A⊕B, and R = A C. Quantum cost of Feynman double gate is equal to 2.

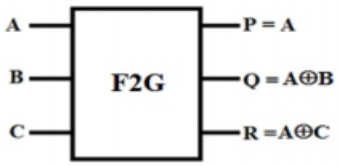

Figure 2 Feynman Double Gate (F2G)

Modified Islam Gate (MIG): Modified IG Gate (MIG) [8] is a 4*4 gate shown in Figure 3. It has A, B, C and D input vector and output vector as P = A, Q = AB, R = ABC and S = AB'D. Quantum cost of MIG gate is 7.

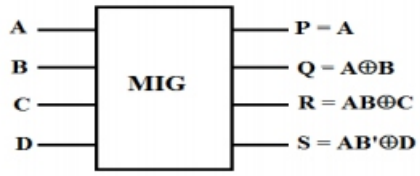

Figure 3 Modified Islam Gate (MIG)

III. PROPOSED WORK:

This paper proposes the efficient fault tolerant carry skip adder/subtractor.

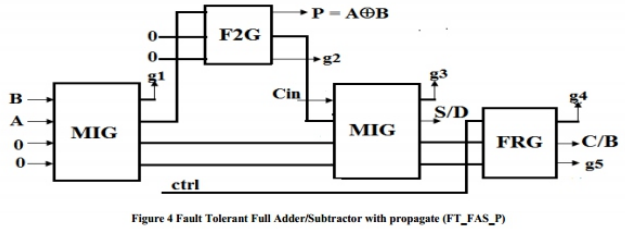

Figure 4 Fault Tolerant Full Adder/Subtractor with propagate (FT_FAS_P)

The proposed design work singly as a unit which consist both adder and subtractor, according to the control logic input it can act adder or subtractor. The below section covers Full adder/subtractor and Parallel adder/subtractor design required for the construction of Carry skip adder/subtractor. B. Fault Tolerant Full Adder/Subtractor with propagate (FT_FAS_P) The Figure 4 shows the fault tolerant full adder/subtractor (with propagate). It can be designed using Two Modified Islam Gate (MIG), One Fredkin Gate (FRG) and One Feynman Double Gate (F2G).

C. Fault Tolerant 4-bit Parallel Adder/Subtractor The basic building block of Parallel adder/subtractor is full adder/subtractor. The Figure 5 shows the 4-bit fault tolerant Parallel adder/subtractor. It can be designed using four fault tolerant full adder/subtractor. D. Fault Tolerant 4-bit Carry Skip Adder/Subtractor In the carry skip adder, delay is reduced due to the carry computation. In the full adder/subtractor operation, if either Input is a logical one, the cell will propagate the carry/borrow input to its carry/borrow output. Hence, the nth full adder/subtractor carry/borrow input (C/B)n, will propagate to its carry/borrow output, (C/B)n+1, when Pn= A B. In addition, the multiple full adders/subtractors, making a block can generate a —block propagate signal P to detour the incoming carry/borrow around to the block‘s carry/borrow output signal. Figure 6 shows the proposed four bit fault tolerant carry skip adder/subtractor block. It is quickly determined by each block, that whether the block‘s carry/borrow input is propagated to its carry output. If the block propagate P is one, the block carry/borrow input Cin is propagated as the block carry/borrow output Cout [10].

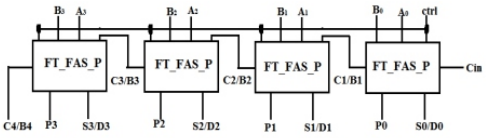

Figure 5 Fault Tolerant 4-bit Parallel Adder/Subtractor

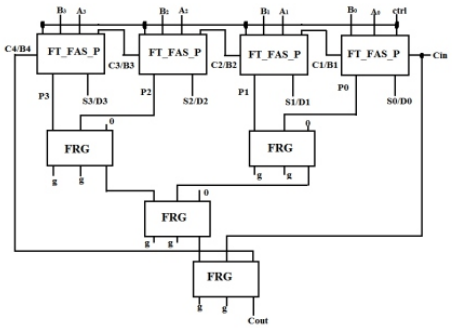

Figure 6 Fault Tolerant 4-bit Carry Skip Adder/Subtractor

IV. SIMULATION RESULTS :

The entire architecture is modeled using Verilog coding. The coding is done on Cadence Virtuoso tool and simulation is done on cadence SimVision tool. The Figure 7 and Figure 8 shows simulation results of proposed fault tolerant full adder and full subtractor with propagate, Figure 9 and Figure 10 shows simulation results of proposed fault tolerant 4-bit parallel adder and parallel subtractor and Figure 11 and Figure 12 shows simulation results of proposed fault tolerant 4-bit carry skip adder and carry skip subtractor respectively

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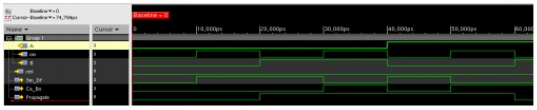

Figure 7 Simulation result of Fault Tolerant Full Adder with propagate

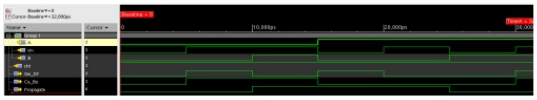

Figure 8 Simulation result of Fault Tolerant Full Subtractor with propagate

Figure 9 Simulation result of Fault Tolerant 4-bit Parallel Adder

Figure 10 Simulation result of Fault Tolerant 4-bit Parallel Subtractor

Figure 11 Simulation result of Fault Tolerant 4-bit Carry Skip Adder

Figure 12 Simulation result of Fault Tolerant 4-bit Carry Skip Subtractor

V. COMPARATIVE RESULTS AND DISCUSSION:

The Table 1, Table 2 and Table 3 gives comparative study of different Fault tolerant full adder/subtractor with propagate, 4-bit parallel adder/subtractor and 4-bit carry skip adder/subtractor.

TABLE I: COMPARATIVE RESULTS OF DIFFERENT FAULT TOLERANT FULL ADDER/SUBTRACTOR WITH PROPAGATE (FT_FAS_P)

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	9	9	10	30
Existing Work [12]	6	7	8	28
Proposed Work	4	4	5	21

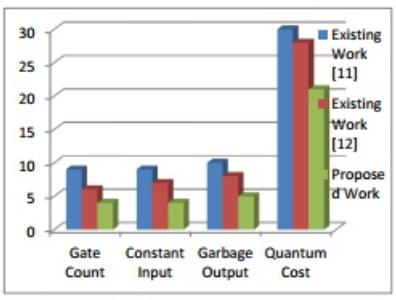

Figure 13 Graphical representation of Different Fault Tolerant Full Adder/Subtractor with Propagate (FT_FAS_P)

From Table 1 and Figure 13 it can be seen that proposed fault tolerant full adder/subtractor with propagate is efficient in terms of gate count, constant input, garbage output and quantum cost.

TABLE II: COMPARATIVE RESULTS OF DIFFERENT FAULT TOLERANT 4-BIT PARALLEL ADDER/SUBTRACTOR

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	36	36	40	120
Existing Work [12]	24	28	32	112
Proposed Work	16	16	20	84

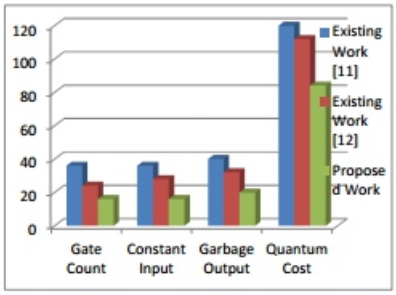

Figure 14 Graphical representation of Different Fault Tolerant 4-bit Parallel Adder/Subtractor

From Table 2 and Figure 14 it can be seen that proposed fault tolerant 4-bit parallel adder/subtractor is efficient in terms of gate count, constant input, garbage output and quantum cost.

TABLE III: COMPARATIVE RESULTS OF DIFFERENT FAULT TOLERANT 4-BIT CARRY SKIP ADDER/SUBTRACTOR

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work [11]	40	39	48	140
Existing Work [12]	28	31	40	132
Proposed Work	20	19	28	104

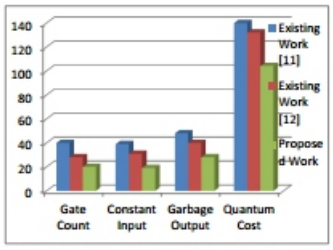

Figure 15 Graphical representation of Different Fault Tolerant 4-bit Parallel Adder/Subtractor

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From Table 3 and Figure 15 it can be seen that proposed fault tolerant 4-bit carry skip adder/subtractor is efficient in terms of gate count, constant input, garbage output and quantum cost.

VI. CONCLUSION:

Design of efficient fault tolerant carry skip adder/subtractor can be done and reversible computations can be done efficiently. This proposed design can work singly as a unit which can act as adder or subtractor depending on control logic.

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