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Design and Performance Analysis of 1 bit Full Adder in 45nm Technology Using Multiplexer Based GDI Logic

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Abstract:
This paper proposes a new method for implementing a low power full adder by multiplexer based Gate Diffusion Input (GDI) and Pass Transistors using 90nm and 45nm technology. Full adder is a very common example of combinational circuits and is used widely in Application Specific Integrated Circuits. It is always advantageous to have low power action for the sub components used in VLSI chips.

The explored technique of realization achieves a low power high speed design for a widely used subcomponent full adder. Simulated outcome using state-of-art simulation tool shows power and speed comparison between conventional and proposed full adders also presented. All simulations have been performed on 90nm and 45nm standard models on Tanner EDA tool.

Index terms:
Conventional full adder, 2-Transistor GDI MUX, 18-TFA and PASS Transistor.

1.INTRODUCTION:

Most SOC design teams now regard power as one of their top design concerns

• Why low-power design?

i. Battery lifetime (especially for portable devices)
ii. Reliability

• Power consumption:

i.Peak power
ii. Average power

Low Power Strategies:

• OS level : Partitioning, Power down
• Software level : Regularity, Locality and Concurrency
(Compiler technology for low power, instruction scheduling)
• Architecture level : Pipelining, Redundancy and Data Encoding
(ISA, architectural design, memory hierarchy, HW extensions, etc)
• Circuit/logic level : Logic styles, Transistor sizing and Energy recovery
(Logic families, conditional clocking, adiabatic circuits, asynchronous design)
• Technology level : Threshold reductions and multi-threshold devices etc...

The challenge that has been faced by VLSI designers is to find effective techniques and their efficient applications to get minimum power dissipation without any compromise on their performance evaluation parameters. Thus, the design of low power circuits with improved performance is a major concern of modern VLSI designs.

The combination of certain logic styles and low power modules with low leakage circuit topologies may greatly reduce the limitations of deep-sub-micro-meter technologies. At the system level, in synchronous implementation of microprocessors, adder cells are the basic modules in a variety of arithmetic units such as arithmetic logical units, ripple carry adders , multipliers etc. Now a days, as growing applications, speed and portability are the major concerns of any smart device it demands small-size, low-power high

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throughput circuitry. So, sub circuits of any VLSI chip needs high speed operation along with low-power consumption. So that logic circuits are designed using pass transistor logic techniques. [1]. It reduces the number of MOS transistors used in circuit, but it suffers with a major problem that output voltage levels is no longer same as the input voltage level. Each transistor in series has a lower voltage at its output than at its input.

II. RELATED WORK:

A. CONVENTIONAL CMOS FULL ADDER:

The full adder operation[2] can be stated as follows:
Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where
Sum = (A **XOR** B) **XOR** Cin
Cout = A **AND** B + Cin (A **AND** B)
Accordingly to the functions can be represented by CMOS logic as follows in fig 1

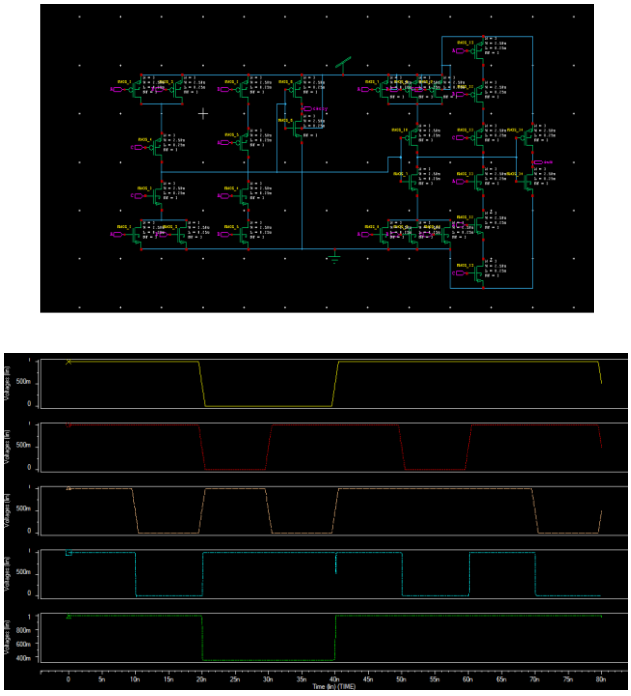


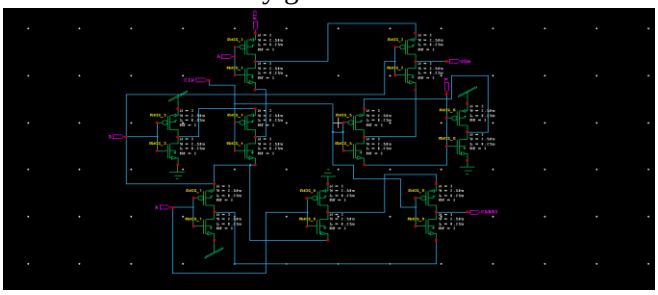
Fig1. Conventional 28-T 1 bit full adder

TABLE I. TRUTH TABLE OF FULL ADDER

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B. 18TRANSISTOR LOGIC:

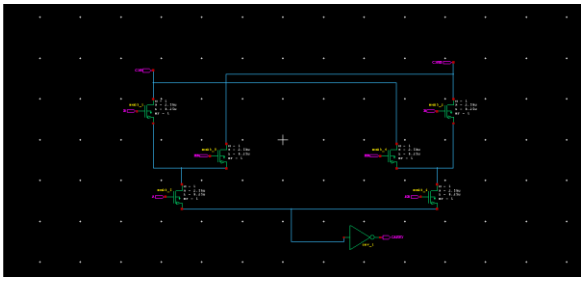
18T are used in the design. 10 Transistors are used to make five 2-1 multiplexer[3]. Among them four are used to generate Sum and one is used to generate Carry out. 4 transistors are used to invert A and B another 4 transistors are used to make AND and OR gate. All of the gates (except inverter) are designed with GDI technique where only two transistor are needed to construct any gate.



C. PASS TRANSISTOR LOGIC:

The basic difference of pass-transistor logic[4] compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads.

CARRY LOGIC:



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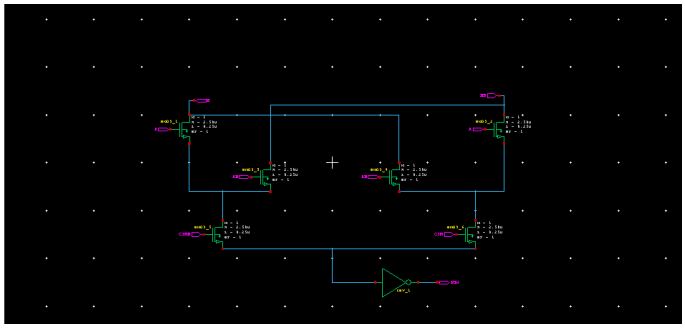
SUM LOGIC:

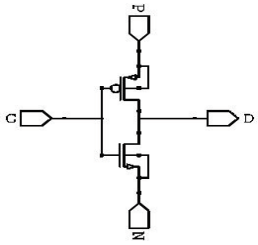


III. PROPOSD DESIGN USING 45nm TECH:

The basic architecture of the 2:1 MUX using GDI method is shown in fig 1. In this configuration we have connected PMOS and NMOS gate along with a SEL line 'A', as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SELECT input is low (0) then the PMOS get activated, and show the input 'B' in the output and due to low input (0) the NMOS stands idle, as it is activated in high input. Same for the case, while the G input is high (1) then the NMOS get activated, and show the input 'C' at the output. Thus this circuitry behaves as a 2-input MUX using 'A' as SEL line, and shows the favourable output as 2:1MUX. Now it's implemented the low power full adder circuit with the help of 2T MUX, made by GDI technique. It require total 6 numbers of 2T MUX having same characteristics to design a 12T full adder[6].

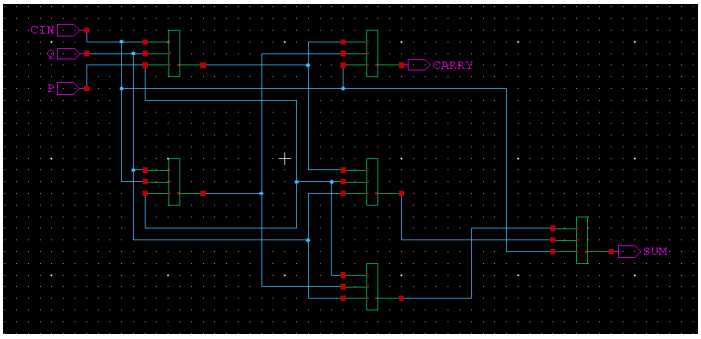
A. Gate Diffusion Input Technique:

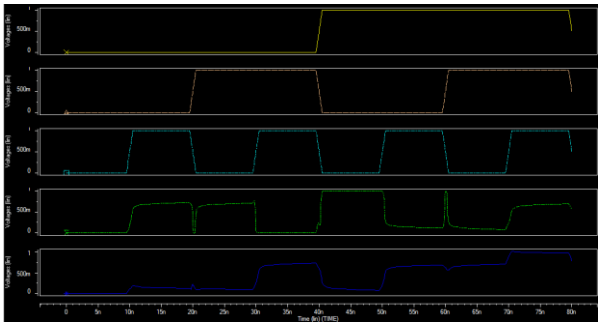
The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below



1. The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2. It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].





B. Logic Analysis:

The digital circuit [5] can be analyzed logically with the help of simple Boolean algebra. The outputs of each MUX can be analyzed to get the sum & carry.

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MUX1= ($B\bar{A}$+CA)

MUX2= ($C\bar{A}$+BA)

MUX3= [($C\bar{A}$+BA)$\bar{C}$+($B\bar{A}$+CA)C]

= AB$\bar{C}$+$\bar{A}$BC+AC

= AB$\bar{C}$+$\bar{A}$BC+AC(B+$\bar{B}$)

= AB$\bar{C}$+$\bar{A}$BC+ABC+A$\bar{B}$C

= AB$\bar{C}$+ABC+$\bar{A}$BC+ABC+A$\bar{B}$C+ABC

= AB(C+$\bar{C}$)+BC(A+$\bar{A}$)+AC(B+$\bar{B}$)

= AB+BC+CA= Cout

MUX4= $\bar{A}\bar{B}$+($\bar{A}$B+AC)B

MUX5=($C\bar{A}$+BA)$\bar{B}$+AB

MUX6= [$\bar{A}$B+($\bar{A}$B+AC)B]$\bar{C}$+[($C\bar{A}$+BA)$\bar{B}$+AB]C

= A$\bar{B}\bar{C}$+$\bar{A}$B$\bar{C}$+$\bar{A}\bar{B}$C+ABC= A ⊕ B ⊕ C=Sum

Logic transition, short-circuit current and leakage current are the three main sources of power dissipation in CMOS VLSI circuits [6], [7]. During the transition of output from one logic level to other both the NMOS and PMOS transistors become active and provides a short circuit path directly between supply to ground which increases the power consumption of the circuit. As the proposed 12-T full adder is made of GDI based MUX , it does not provide direct connections between supply and ground, so the probability of a getting short circuit current during switching can be considerably reduced; i.e, the power consumption due to short circuit current is considerably small. Again, in the proposed 12T full adder, all the select line of the MUX i.e. the G nodes of the GDI cells are directly connected with the input signals, results a much faster transition (less delay) in its output signals. As a result, the power consumption of the final pad out stage is low and it can provide faster Sum and Cout outputs.

C. POWER CONSUMPTION:

There are three main components of power consumption in digital VLSI circuits.

i. Switching component:

consumed in charging and discharging of the circuit capacitances during transistor switching.

ii. Short-circuit component:

Created by short-circuit current flowing from supply voltage to ground during transistor switching.

iii. Static power component:

Existence of static and leakage currents in stable state of circuit cause this component of power consumption. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states [8]. Dynamic power accounts for the majority of the total power consumption in digital VLSI circuits The average power dissipation for a CMOS circuit is given by

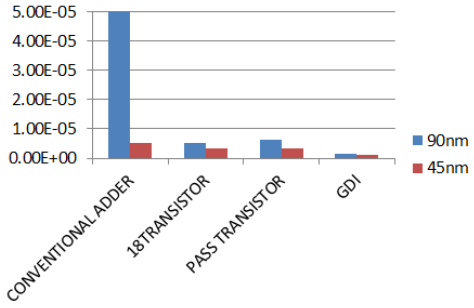
Pavg = Pdynamic+ Pshort circuit + Pstatic ……..(1)

= Vdd .fclk .Σ(Vi swing .Ci load . αi) + Vdd.ΣIi sc +Vdd. Il .

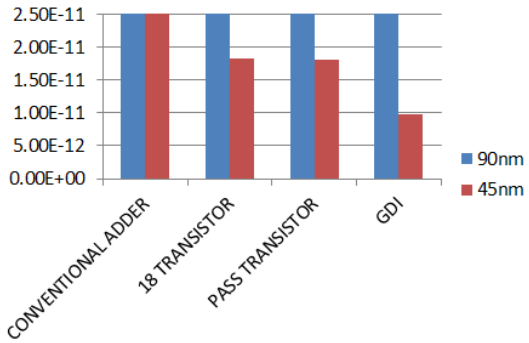
IV. SIMULATIONS AND COMPARISIONS:

In order to test the performance of proposed adder cells, all schematic have performed on Tanner EDA tool version 13.0v and Simulations have carried out using HSPICE to measure the power consumption, propagation delay and power delay product of the full adders using 90nm and 45nm technology with same input conditions of 1.0 V 0.7V supply and the maximum frequency of 100 MHz. Simulation results are shown in figures.

Power Analysis



Propagation Delay Analysis



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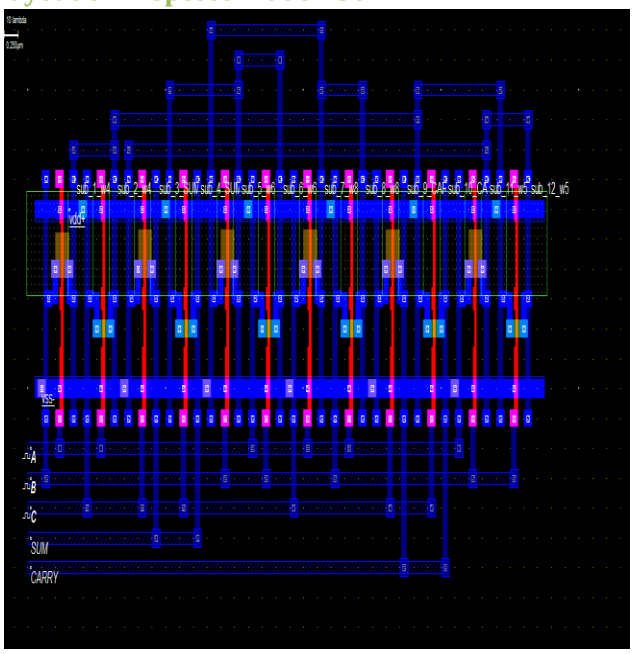
Comparison tables with Conventional Full Adder using 90nm and 45nm Technologies

90nm TECHNOLOGY	POWER	DELAY	PDP	TRANSISTOR COUNT
CONVENTIONAL ADDER	15.8 mW	20.02 ns	319.16pJ	28
18 TRANSISTOR	5.365E-03 mW	5.970 ns	32.02E-03pJ	18
PASS TRANSISTOR	6.325E-03 mW	0.776 ns	4.90E-03 pJ	16
GDI	1.335E-03 mW	0.252ns	0.33E-03 pJ	12

45nm TECHNOLOGY	POWER	DELAY	PDP	TRANSISTOR COUNT
CONVENTIONAL ADDER	5.25 uW	0.298 ns	15.64E-04 pJ	28
18 TRANSISTOR	3.37 uW	0.0185ns	6.143E-05 pJ	18
PASS TRANSISTOR	3.25 uW	0.0180 ns	5.866E-05 pJ	16
GDI	1.18 uW	0.0097 ns	11.54E-06 pJ	12

Layout of Proposed Adder Cell



VII. CONCLUSION:

From the above results it can be concluded that 1 bit CMOS full adder designs has got better performance in delay, power and area consideration in comparison with conventional full adder. It shows that in contrast to other conventional techniques, this approach is better and it will be more appropriate for industrial practice in complex process technologies.

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