ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Multi Band Hysteresis Modulation Based Current Control Technique for Seven Level Grid Connected Voltage Source Inverter

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Abstract:

This paper deals with the multiband hysteresis control technique which tracks the desired reference current and provide desired voltage and current waveform with less distortion for grid connected systems. Cascaded H bridge multilevel inverter is used in high power and medium power applications. Multiband tracks the desired reference current and is used for evaluating the performance of multilevel inverters.

This control technique is based on time domain formulation. The efficiency of the controller in reducing total harmonic distortions and switching losses based on the instantaneous switching frequency, system parameters and number of levels is studied. The simulation results are obtained for seven level cascaded H bridge multilevel inverters.

Key Words:

Hysteresis control technique, Cascaded H bridge, Multiband tracks, multilevel inverters.

I.INTRODUCTION:

Two level inverter such as square wave & quasi square wave inverters are facing major problem of the lower order harmonics. Lower order harmonics are more dominant in nature while compare to higher order harmonics because of high harmonic distortion in waveform.

These inverters are limited to low and medium power applications because of their limitations in increasing frequency [1]. To obtain minimum ripple content in waveform, we require high switching frequency along with PWM [2].

For high power high voltage applications two level inverters have some limitations in operating at high frequency mainly due to harmonics and switching losses. Multilevel inverters placed big role in high power high voltage applications of electric motor drives [4], which provides stair case or stepped/PWM output voltage which is approximately sinusoidal ac output voltage with less distortion.

MLIs provide better harmonic profile, reduced stress on semiconductor power electronic devices. With advancement in power semiconductor devices and converter topology, the issue of power quality becomes more significant multilevel inverters have a solution problems faced by the conventional two level inverters.

III. MODELLING OF THE MULTILEVEL CASCADED INVERTER:

The basic building block for cascaded H bridge inverter is shown in fig 1.For a N level cascaded H bridge inverter separate DC source is connected to single phase full bridge and H-bridge inverter.

Each inverter bridge is cascaded depending on the levels required and generates seven output voltage levels +3Vdc,+2Vdc, +Vdc, 0,-Vdc, -2Vdc,-3Vdc for a three level inverter using different combination of switches S1,S2,….Sn.

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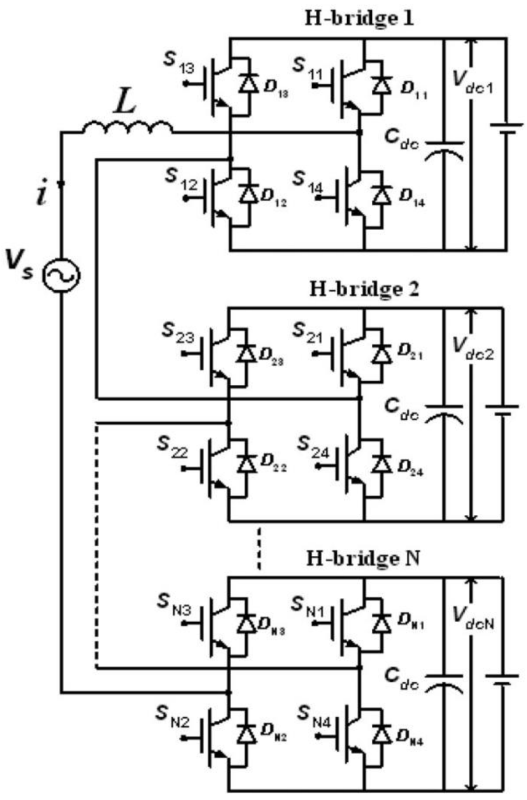

Fig1. Cascaded H bridge n level inverter

Fig. 2 is added which shows the power circuit of a 7 level cascaded inverter composed of three full bridge inverters connected in series on each phase.

For each full bridge inverter the output voltage is given by [5] :

$$V_{oi} = V_{dc}(S_{1i} - S_{2i}) \quad (1)$$

And the input dc current is:

$$I_{dci} = I_a(S_{1i} - S_{2i}) \quad (2)$$

where:

- i =1…5 (number of full bridge inverters employed) for the 11 level cascaded type and i =1…3 (number of full bridge inverters employed) for the 7 level type.

Ia is the output current of the cascaded inverter.

S1i and S2i are the upper switch of each full bridge inverter.

Now the output voltage of each phase of the multilevel cascaded inverter is given by:

$$V_{on} = \sum_{i=1}^{n} V_{oi} \quad (3)$$

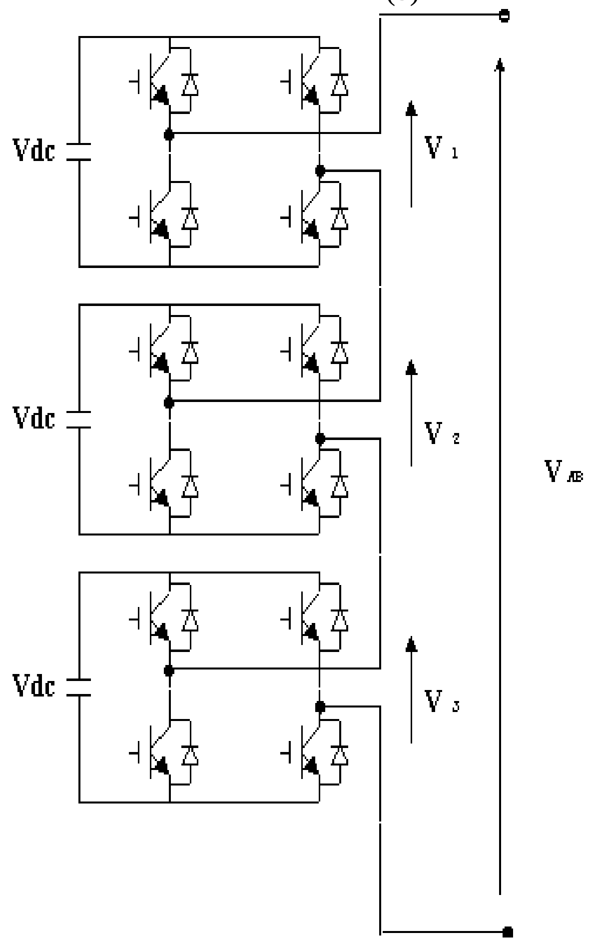

Fig.2 Power circuit of a 7 level single phase cascaded inverter

The switching states for Cascaded H bridge inverter is given in table 1

Switching States:

Table 1: Switching states for CMLI

Voltage (Vo)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	1	0	1	0	1	0	1	0	1
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$3V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$-V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$-2V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-3V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

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The number of output phase voltage levels is m=2s+1, s being the number of dc sources. Multilevel inverters are used for applications like static var generation an interface with renewable energy sources and for battery based applications. The inverter can be used to regulate the power factor of current and voltage of the system. Cascaded inverters are ideal for usage of renewable energy sources with an ac grid. Cascaded inverters are used as a main traction drive in electric vehicles. The cascaded inverter serves as a rectifier or charger for the batteries of electric vehicles when connected to ac supply. The cascaded inverter acts like a rectifier during regenerative braking.

III. MULTIBAND HYSTERESIS MODULATION:

The graphical representation for multiband hysteresis modulation is shown in fig 3. The basic building block for cascaded H bridge inverter is shown. The switches IGBT with an anti parallel diode. Cascaded H bridge inverter require N=(n- 1)/2 H bridges. Voltage and power stress is distributed among the switches. The output voltage of n level inverter is V0= uVdc.

The voltage stress on the semiconductor switches and the dc link voltage is 1/N times the net dc link voltage Vdc for n level inverter. The generalized multiband hysteresis modulation tracks the desired reference current in the load side in current controlled operation mode h – net hysteresis band, – dead zone introduced to prevent overlapping between loops.

The inverter is made to track the desired output current i to reference value i ref. Multiband hysteresis controller modulates the signal with N number of bands and compares the current error e=(iref –i) with sector based hysteresis bands h and switching signals are generated for the power switches S11,S12,…..SN4 of the various H bridges of the inverter.

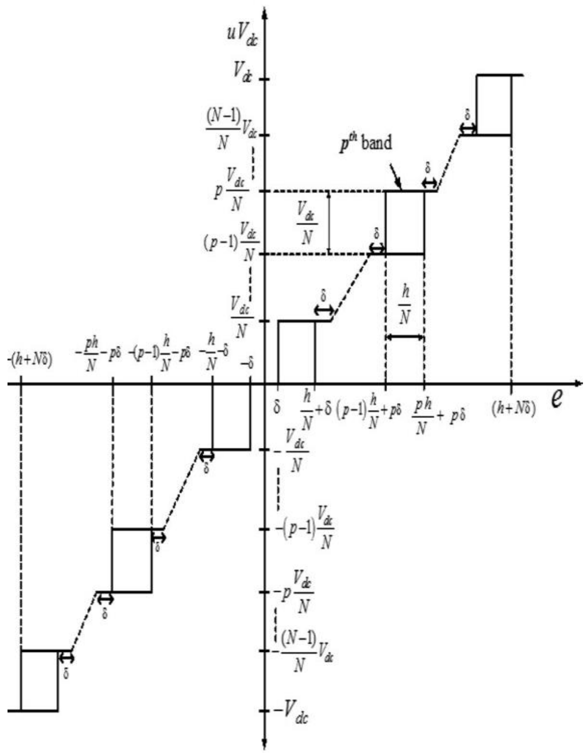

Fig. 3 Generalized multiband hysteresis modulation for N level inverter

The multiband hysteresis modulation scheme for the multilevel inverters uses symmetrical hysteresis bands called upper band and lower band to control the switching over to the adjacent level. When the error signal crosses the inner boundary level 1, the output of the inverter is increased or decreased by one level depending on the upper or lower boundary limit which it has crossed.

The change in the voltage level will cause current error (e) to reverse its direction within the band limit to track its own path before reaching the next higher boundary limit. If the error does not reverse its direction then the error may reach the immediate next boundary limit (outer boundary 2). At the next higher boundary limit the next voltage level of multilevel inverter will be switched. This process continues only till the current error reverses. The voltage level applied at the each boundary level of the current error should be sufficient enough to force the current error back within the respective band limit.

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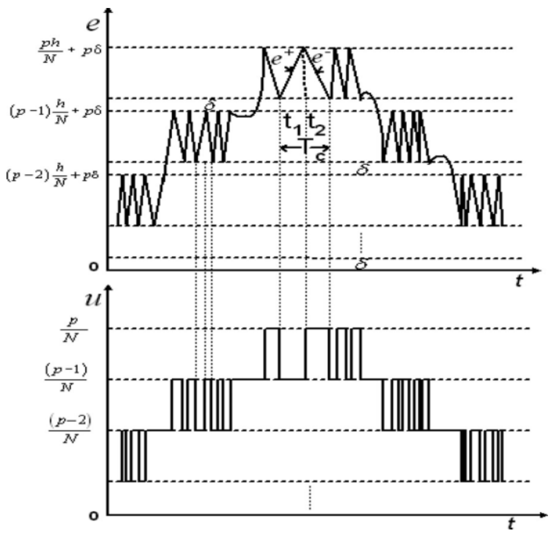


Fig.4Tracking error characteristics in various hysteresis bands

GENERALISED SWITCHING ALGORITHM:

Let us consider that the five level inverter is operating in the pth band. The Hysteresis band starts from [(p-1) h/N+p] and ends at [ph/N+p] level for the pth band corresponding to the (p-1) Vdc/N and pVdc/N voltage levels. The length of the net effective hysteresis band is h/N and voltage Vdc/N is the difference between the net operating voltage levels for the particular band. The voltage levels (p- 1)Vdc/N and pVdc/N is the output for the switching algorithm.

GENERALISEDDERIVATION OF SWITCHING FREQUENCY:

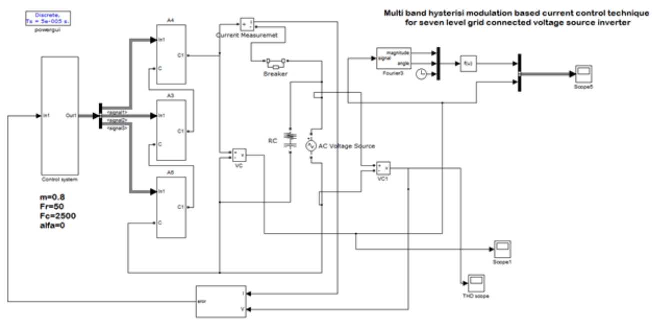
The time domain representation of the current tracking error e(t) The time-domain representation of the current tracking error e(t) and corresponding switching logic u(t) for positive half cycle using the multiband hysteresis algorithm. When the current error e touches the hysteresis band limit ((p–1)h/N+ pδ)) before start of the duration t1 , then the switch Sp3 gets turned ON and u=(p–1)/Nin the interval t1 , satisfying the switching algorithm condition ii-(b) for positive half cycle given in Table I for the condition “Ife < ((p-1)h/N+pδ)”. As a result the actual current (i–) starts to decay with the negative slope until the increasing current error e+ exceeds the upper hysteresis band limit (ph/N+ pδ), before the start of duration t2 .

After which the switch Sp2 gets turned ON and u = p/Nin the interval t2 , satisfying the switching algorithm condition ii-(b) for the condition As a result the current (i+) starts to increase with the positive slope until the decreasing current error (e–)crosses the lower hysteresis band limit(p-1)h/N+pδ).

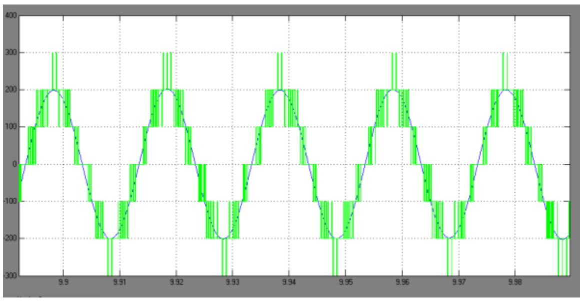
IV. SIMULATION RESULTS:

Simulation is performed using MATLAB/SIMULINK software. Simulink liabrary files include inbuilt models of many electrical and electronics components and devices such as diodes, MOSFETS, capacitors, inductors, motors, power supplies and so on. The circuit components are connected as per design without error, parameters of all components are configured as per requirement and simulation is performed.

CIRCUIT:



TRACKING CHARACTERISITICS:



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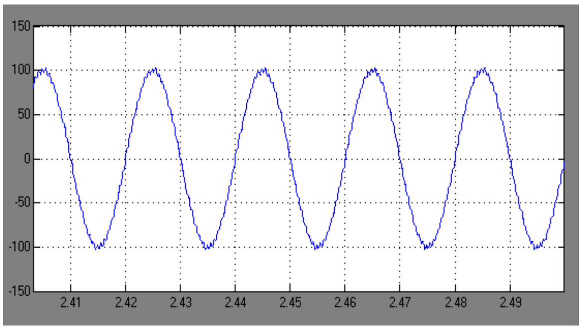
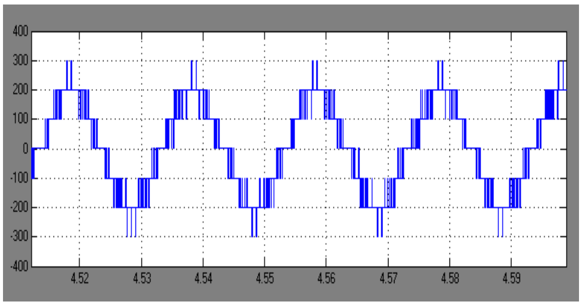
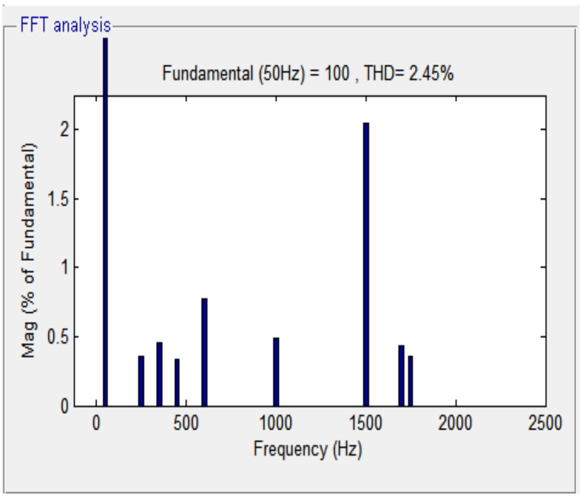
GRID SIDE VOLTAGE:



INVERTER OUTPUT:



THD VALUE:



V. CONCLUSION:

This paper is the study of a multiband hysteresis control technique based on time domain formulation for cascaded H bridge multilevel inverter application. The generalized switching frequency in time domain formulation is used for the design of multiband hysteresis controller for tracking the desired reference current and to track the error signal for the inverters within the band range. The simulation results are obtained for seven level cascaded H bridge multilevel inverter using multiband hysteresis controller. The results are useful in determining the total switching losses, total harmonic distortions and the efficiency of the controller's operation.

VI. FUTURE WORK:

The work presented here is just the multiband hysteresis modulation technique for Cascaded H bridge 7 level inverter and neutral point clamped inverter. The design of these inverters as filter DVR will be useful to improve the power quality. The Simulink model of these inverters can be used for the design of DVR.

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