

Multilevel Inverters Implementation with Voltage Restore Process

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Abstract:

For High power, high voltage applications modern ages multilevel inverters are widely used. They provide better operation as well as effective efficiency rather than conventional two level inverters which differs in harmonic distortion, lower electromagnetic interference with large dc link voltage ratings. In multilevel inverters have problems in the sequence of number of components, complex pulse width modulation control method and voltage balancing problem. In this paper new topology is discussed which compensate the disadvantages by reversing voltage component. Where this method need of few more components other than conventional inverters, require fewer carrier signals and gate drives. Especially for High power output voltage levels the overall cost and complexity are reduced greatly. A prototype of seven level inverter is discussed with simulation of MATLAB which tested with simulation results.

Key Words:

Multilevel inverter, power electronics, SPWM topology.

I. INTRODUCTION:

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps.

There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns [1]. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.

One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in the cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors.

Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2]. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices. However, for a complete solution to the voltage-balancing problem, another multilevel converter may be required [3].

In recent years, there has been a substantial increase in interest to multilevel power conversion. Recent research has involved the introduction of novel converter topologies and unique modulation strategies. However, the most recently used inverter topologies, which are mainly addressed as applicable multilevel inverters, are cascade converter, neutral-point clamped (NPC) inverter, and flying capacitor inverter. There are also some combinations of the mentioned topologies as series combination of a two-level converter with a three-level NPC converter which is named cascade 3/2 multilevel inverter [4].

There is also a series combination of a three-level cascade converter with a five-level NPC converter which is named cascade 5/3 multilevel inverter [5]. Some applications for these new converters include industrial drives [6], flexible ac transmission systems (FACTS) [7]–[9], and vehicle propulsion [10], [11]. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers [12]. Some new approaches have been recently suggested such as the topology utilizing low-switching-frequency high-power devices [13]. Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics.

It is also unable to exactly manipulate the magnitude of output voltage due to an adopted pulse width modulation (PWM) method [14]. In [15] and [16], the multilevel output is generated with a multi winding transformer. However, the design and manufacturing of a multi winding transformer are difficult and costly for high-power applications. A novel four-level inverter topology is also proposed, and it is valid for inverters with even number of voltage levels and not capable of outputting a zero-voltage state.

As a result, the inverter output phase voltage for zero modulation indexes is a bipolar waveform taking two distinct values and exhibits high rms value and considerable harmonic energy concentrated at the switching frequency. This is a disadvantage of the proposed inverter, particularly when it should output low or zero voltage to a load [17]. Another approach is selection based on a set target which can be either the minimum switches used or the minimum used dc

voltage. It also requires different voltage source values which are defined according to the target selection [18]. However, this approach also needs basic units which are connected in series, and the basic units still require more switches than the proposed topology. Another disadvantage of the topology is that the power switches and diodes also need to have a different rating which is a major drawback of the topology. In [19], the voltage sources are not used efficiently in generating output voltage levels. For example, the topology in [19] can generate only five output levels with four dc sources, while conventional multilevel inverters can generate up to nine levels with the same number of power supplies.

The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. However, there are asymmetrical topologies [20] which require different voltage sources. This criterion needs to arrange dc power supplies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies [21]–[23], while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage products.

In [24], a new approach has been proposed that decreases the number of required dc supplies and inserting transformer instead. The main disadvantage of the approach is adding so many transformer windings which will add up to the overall volume and cost of the inverter. There is also another topology which requires more switches than the proposed topology for the same number of levels [25].

Some of the proposed topologies suffer from complexities of capacitor balancing [26]–[28]. In [26], the capacitor values used in the topology are proportional to the load current, and as the load current increases, a larger capacitor should be selected. In [27], the capacitor voltage will affect the output voltage when modulation index reaches near its extreme values, i.e., zero or one. This paper presents an overview of a new multilevel inverter topology named reversing voltage (RV). This topology requires less number of components compared to conventional topologies.

It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter. This paper describes the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. The simulation and experimental results of the proposed topology are also presented.

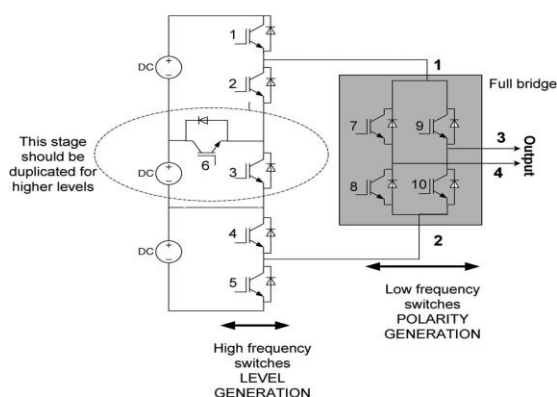


Fig. 1. Schematic of a seven-level inverter in single phase.

II. New Multilevel Topology:

A. General Description:

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity.

This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output.

In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities. The RV topology in seven levels is shown in Fig. 1. As can be seen, it requires ten switches and three isolated sources.

The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage. This part, which is named polarity generation, transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.

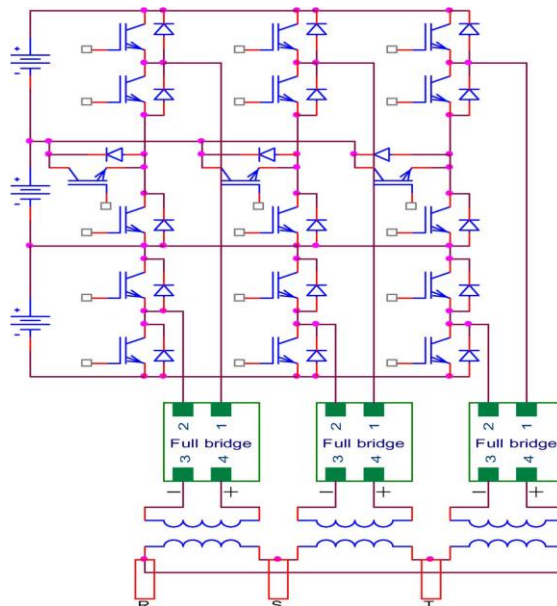


Fig. 2. Three-phase RV multilevel topology.

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 1. Therefore, this topology is modular and can be easily increased to higher voltage levels by adding the middle stage in Fig. 1. It can also be applied for three-phase applications with the same principle. This topology uses isolated dc supplies.

Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. In Fig. 2, the complete three-phase inverter for seven levels is shown with a three-phase delta connected system. According to Fig. 2, the multilevel positive voltage is fed to the full-bridge converter to generate its polarity. Then, each full bridge converter will drive the primary of a transformer. The secondary of the transformer is delta (Δ) connected and can be connected to a three-phase system. This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient.

The reason is that, according to Fig. 1, the multilevel converter works only in positive polarity and does not generate negative polarities. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation, while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method which needs several modulation signals [29]. Another disadvantage of this topology is that all switches should be selected from fast switches, while the proposed topology does not need fast switches for the polarity generation part. In the following sections, the superiority of this topology with respect to PWM switching and number of components is discussed.

Table I: Switching Sequences For Each Level

Level Mode	0	1	2	3
1	2,3,4	2,3,5	1,4	1,5
2		2,4,6	2,6,5	

B. Switching Sequences:

Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control.

Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements. This topology is redundant and flexible in the switching sequence. Different switching modes in generating the required levels for a seven-level RV inverter are shown in Table I. In Table I, the numbers show the switch according to Fig. 1 which should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter.

It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work. In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation. According to the aforementioned suggestions, the sequences of switches (2-3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in Fig. 3. As can be observed from Fig. 3, the output voltage levels are generated in this part by appropriate switching sequences.

The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in Fig. 4. In this paper, PD SPWM is adopted for its simplicity [30]. Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other. The modulator and three carriers for SPWM are shown in Fig. 4.

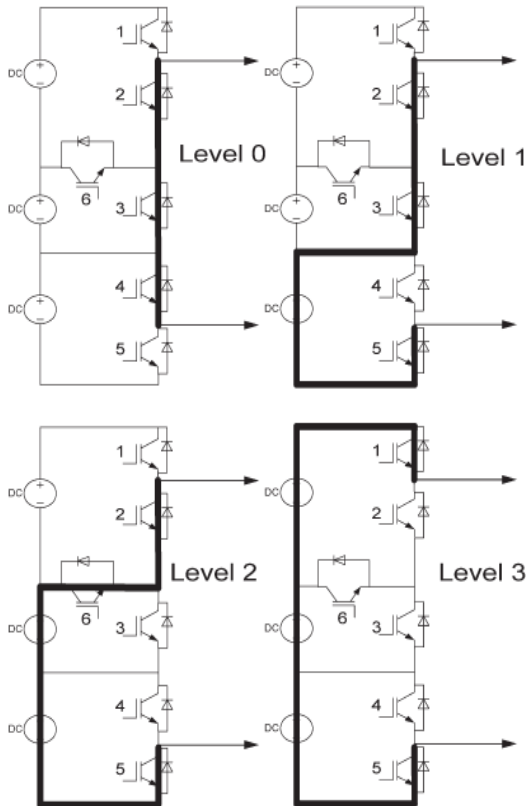


Fig. 3. Switching sequences for different level generation.

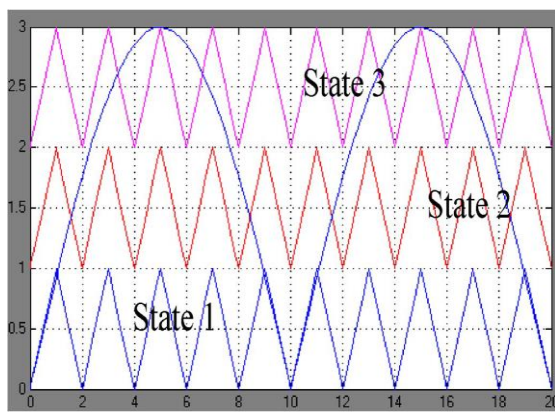


Fig. 4. SPWM carrier and modulator for RV topology.

Table II: Switching Cases In Each State According To Related Comparator Output

States	One		Two		Three	
	+	-	+	-	+	-
Compare	+	-	+	-	+	-
Mode	2-3-5	2-3-4	2-5-6	2-3-5	1-5	2-5-6

According to Fig. 4, three states are considered. The first state is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in Table II. Table II shows the relation between the right comparator output according to the current state and required states for switching to meet the voltage requirements. The right comparator here refers to the comparator output of the current state.

As illustrated in Table II, the transition between modes in each state requires minimum commutation of switches to improve the efficiency of the inverter during switching states. The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. For example, a seven-level cascade topology [31], [32] has 12 switches, and half of them, i.e., six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.

Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascade [33] inverter, and hence, it has a better efficiency. The same calculation is true in a topology mentioned in [34]. The least number of switches in the current path for a seven-level inverter according to [34] is five (for generating level 3), which requires one switch more in the current path compared to the proposed topology which requires only four conducting switches. These switching sequences can be implemented by logic gates or DSP.

The signal stage should be isolated from the power stage by optocouplers for control circuit protection. The drive circuit is also responsible to generate the dead time between each successive switching cycle across the dc source. The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse

modes. In the forward mode, switches 8 and 9 as in Fig. 1 conduct, and the output voltage polarity is positive. However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency. The resulting PWM waveforms for driving the high frequency switches in the level generation part are illustrated for one complete cycle in Fig. 5. According to Fig. 5, high frequency switches can be adopted in this stage based on the required frequency and voltage level. However, low-frequency polarity generation part drive signals are generated with the line frequency (50 Hz), and they only change at zero-voltage crossings.

C. Number of Components:

As mentioned earlier, one of the promising advantages of the topology is that it requires less high-switching-frequency components. High-frequency switches and diodes are expensive and are more prone to be damaged than low-frequency switches. According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components. Therefore, as the number of high-frequency switches is increased, the reliability of the converter is decreased.

In the proposed converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved. The number of required three-phase components according to output voltage levels (N) is illustrated in Table III [35]. It can clearly be inferred that the number of components of the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels. Fig. 6 shows the required components versus different voltage levels as mentioned in Table III.

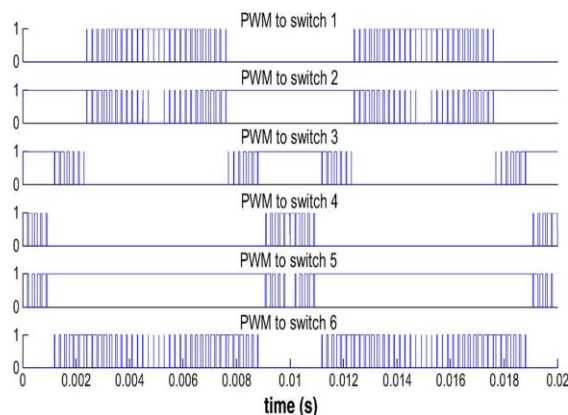


Fig. 5. Complete gate signals for level generation part.

Table III: Number Of Components For Three-Phase Inverters

Inverter type	NPC	Flying capacitor	Cascade	RV
Main switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
main diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
Clamping diodes	$3(N-1)(N-2)$	0	0	0
DC bus capacitors/ Isolated supplies	$(N-1)$	$(N-1)$	$3(N-1)/2$	$(N-1)/2$
Flying capacitors	0	$\frac{3}{2}(N-1)(N-2)$	0	0
Total numbers	$(N-1)(3N+7)$	$\frac{1}{2}(N-1)(3N+20)$	$\frac{27}{2}(N-1)$	$(13N+35)/2$

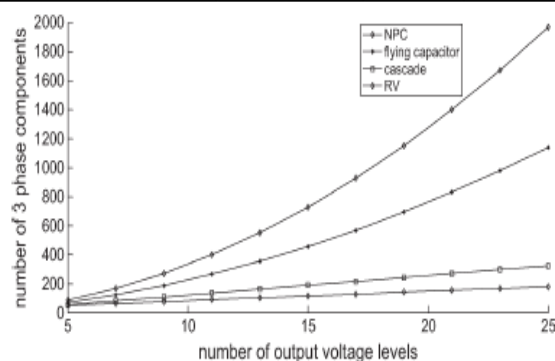


Fig. 6. Components for multilevel inverters.

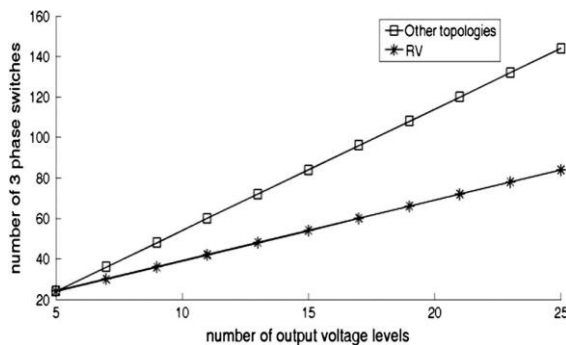


Fig. 7. Required switches for multilevel inverter.

As the most important part in multilevel inverters is the power semiconductor switches which define the reliability and control complexity, the number of required switches against the required voltage levels is shown in Fig. 7 for the new topology as well as other topologies. According to Figs. 6 and 7, the new topology requires fewer components and also fewer switches compared to others. Therefore, it should have the potential of finding widespread applications in high-voltage power devices and apparatus that includes FACTS and HVDC.

It also requires less number of components as to conventional inverters that use phase shift transformers for increasing the output voltage levels. STATCOM, which is a type of FACTS apparatus and has been widely developed in recent years, can be a good candidate for applying the topology. In order to fulfill the stringent voltage harmonic standards such as IEEE519, a STATCOM of the conventional 48-pulse inverter is normally used [36]. The topology requires eight three-phase transformers and eight full-bridge inverters requiring 48 switches. However, the proposed topology is superior compared to this conventional topology since it requires 84 switches for implementing similar output voltage waveform with the same quality while omitting eight bulky transformers.

III. EXPERIMENTAL RESULTS:

In this section, practical results are demonstrated for a single phase seven-level inverter with the proposed topology as shown in Fig. 8. The PWM controller is implemented by a dSPACE 1104 DSP card. The output LC filter is used to remove high-frequency switching ripples and is a combination of a 2- μ F capacitor and a 10-mH inductor.

The three modules in the level generation part are SKM 50 GB, and the full-bridge module in the polarity generation part is SKM 40 GB. DC power supplies are also adjusted at 50 V. The topology is used to generate seven voltage levels for a resistive and inductive load. The output voltage is 300 VP-P. The switching frequency is 4 kHz. The PWM signals are generated for the inverter by the DSP board according to the PD-SPWM method as mentioned. The control signals are unipolar, and there is no need for generation of bipolar signals in DSP for modulation [25] in the proposed multilevel inverter, and the unipolar modulation presents better results in terms of harmonics [37]. Fig. 9 shows how the output voltage is made in the polarity generation part.

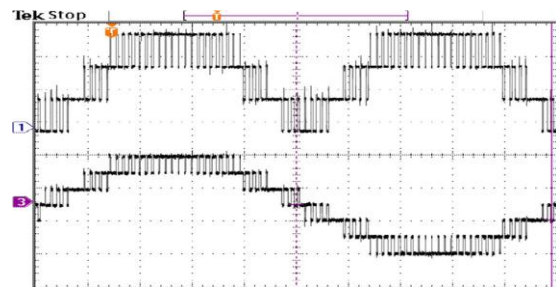


Fig. 9. Waveforms in the proposed topology from top: Output voltage of polarity generating part (50 V/div) and output voltage (100 V/div). Time: 2 ms/div.

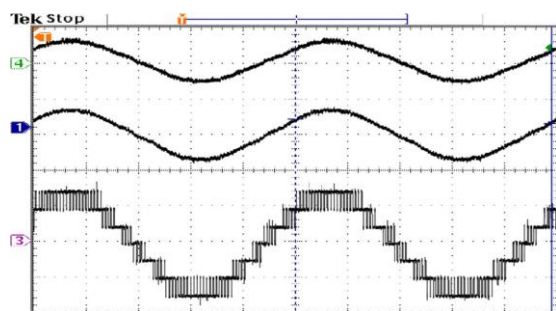


Fig. 10. Waveform of the proposed multilevel inverter with a resistive load from top: Output current (2 A/div), output voltage after filter (200 V/div), and multilevel output before filter (100 V/div). Time: 4 ms/div.

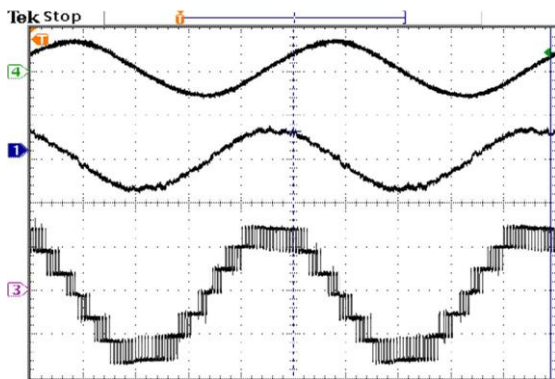


Fig. 11. Waveform of the proposed multilevel inverter with inductive load from top: Output current (2 A/div), output voltage after filter (200 V/div), and multilevel output before filter (100 V/div). Time: 4 ms/div.

IV. CONCLUSION:

In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The PD-SPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control. The experimental results of the developed prototype for a seven-level inverter of the proposed topology are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM.

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