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Low Power 8-Bit ALU Design Using Full Adder and Multiplexer

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ABSTRACT:
Arithmetic logic unit (ALU) is an important part of microprocessor. In digital processor logical and arithmetic operation executes using ALU. In this paper we describes 8-bit ALU using low power 11-transistor full adder (FA) and Gate diffusion input (GDI) based multiplexer. By using FA and multiplexer, we have reduced power and delay of 8-bit ALU as compare to existing design. All design were simulated using DSCH and Microwind 3.5 in 65 nm BSIM4 technology. Performance analyses were done with respect to power and area.

Keywords:
Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor).

I. INTRODUCTION:
Exploitation of very large scale integration (VLSI) technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal oxide semiconductor (CMOS) has been the backbone in mixed signal because it reducing power and providing good mix component for analog and digital design. The mainstays of power consumption in CMOS circuits are static power (P_s), dynamic power (P_d) and short circuit power (P_{sc}). Thus, the total power consumption (P_t) is

$$P_t=P_s+P_d+P_{sc}(1)$$

Ps is caused by leakage current between the diffusion region and the substrate. Pd consumes due to capacitive load and clock frequency and Psc is caused by short circuit current. Increasing number of transistors per chip area and scale down technologies have consumed more power thus the main objective is to reduce the power consumption by using different techniques for improving performance of VLSI circuits. ALU is the section of the computer processor that executes arithmetic and logical operation. ALU is an exclusively combinational logic circuit which means output changes with changing of input response. The ALU is a utile device in microprocessor, performing various logical and arithmetic operations [1].

II. PREVIOUSWORK:
Power can be reduced either architecture level or module level or circuit level. In analog switch technique select input logic as a control logic and passes another input signal from gate terminal [4]. FA is a basic building block for designing ALU, different types of FA designing for minimizing power such as hybrid FA, low power 10 transistors FA and11transistor FA. FA operating in ultra-low mode by using sub threshold current and consumes low power [2]-[3]. FA build using low power XOR gates and 2 is to 1 multiplexer [7]. ALU design using Fin FET technology has two gates which are electrically independent, minimize the complexity of the circuit and also reduce the power consumption due to reducing the leakage current.

In Fin FET technology "Fin" is a thin silicon which mould the body of the device [5]. ALU design using the reconfigurable logic of multi input floating gate metal oxide semiconductor (MIFG-MOS) transistor have multiple inputs, increased the functionality of the circuit. MIFG-MOS transistor gives ON and OFF states of the transistor by observing weighted sum of all inputs. MIFG-MOS transistor reducing the number of transistor and complexity of the circuit, improve the performance of the circuit minimize the delay and reduced the power dissipation [6].

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When channel length is scale down for designing circuits, metal gate and high-k dielectric is to be introduced. Metal gate and high-k dielectric gives extra channel length with output down the leakage current[8].

III. CIRCUIT DESIGN OF ALU:

ALU is a core part of computer or digital processor that executes arithmetic and logical operation, such as increment, decrement, addition and subtraction as an arithmetic operation and AND, OR, XOR, XNOR as a logical operation. ALU is build by using FA and multiplexer.

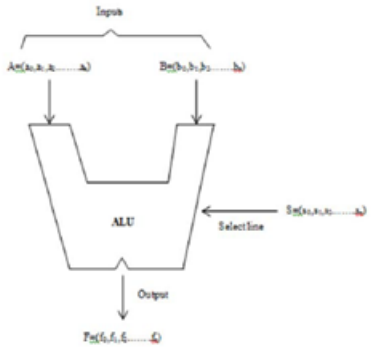

Fig. 1. Symbol of ALU

TABLEI.TRUTHTABLEOFALU

S_2	S_1	S_0	OPERATION
0	0	0	OR
0	0	1	XNOR
0	1	0	XOR
0	1	1	AND
1	0	0	INCREMENT
1	0	1	ADDITION
1	1	0	DECREMENT
1	1	1	SUBTRACTION

A. 11 Transistor Full Adder (11TFA)

FA is basic functional module for designing ALU. 11T used for design of FA, this modern design of FA is minimize the power and reduced the delay. FA depicts in Fig. 2, circuit is operating at power supply (VDD) 0.9V. Inputs A apply to the gate terminal of PMOS_1 and NMOS_1, drain terminal of PMOS_2. Inputs B apply to the gate terminal of PMOS_2 and PMOS_2, drain terminal of NMOS_1.

When source voltage (VS) is greater than threshold voltage (VTH) transistor is ON and pass the signal from gate terminal to drain terminal means pass the gate voltage (VG) to drainterminal.

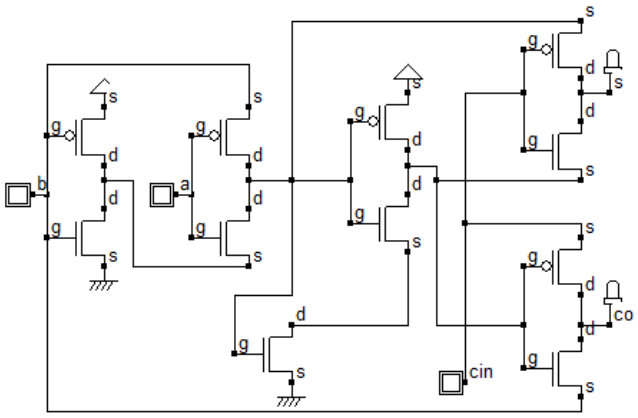

Fig. 2. Schematic of 11T FA

Thus, when input A is high, pass the input B vice versa. FA is build using low power XOR gates and 2 is to 1 multiplexer. XOR gates gives the sum output and multiplexer responsible for carry out (C_{out}). An extra transistor NMOS_6 operates in ultra-low mode using sub threshold current and consumes low power. At strong inversion region gate to source voltage (V_{GS}) is higher than threshold voltage (V_{TH}), majority carriers removed from the area of gate and minority carriers is produced, at weak inversion region V_{GS} is below than V_{TH} less minority carrier is produced, but their presence produce leakage current this current is called sub threshold current. This current can be used when V_{DD} is below then V_{TH} and run the circuit at ultra-low mode and consumes less power. 11T FA is operating at sub threshold mode by adding an extra transistor NMOS_6.

B. GDI based Multiplexers:

GDI technique is area efficient technique which consumes less power with reducing the number of transistor. GDI technique need twin well process or silicon on insulator for chip composition.

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Twin well process gives separate optimization of n-type and p-type transistor and also optimizes gain and V_{TH} of n-type and p-type device. Silicon on insulator combined both MOS and bipolar technologies into a single process. GDI technique providing an extra input for the cell and maintain the circuit complexity. GDI technique solves the problem of poor ON to OFF transition characteristic of PMOS and providing the full swing at internal node of circuit. Fig. 3 depicts the 2 is to 1 multiplexer, select line S is common input for gate terminal of PMOS_1 and NMOS_1. Input A and Input B is connected to the source terminal of PMOS_1 and NMOS_1 respectively. When S is low then PMOS_1 is ON and pass the input A from source terminal to drain terminal, when S is high NMOS_1 is ON and PMOS_1 is OFF. Output is common for drain terminal for PMOS_1 andNMOS_1.

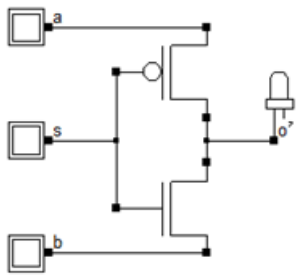

Fig. 3. GDI based MUX 2

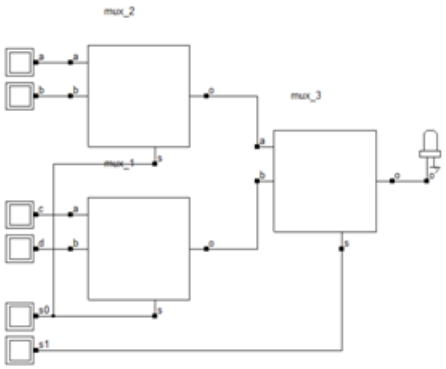

Fig. 4. GDI based MUX 4

Fig. 4 depicts the 4 is to 1 multiplexer, 4 is to 1 multiplexer design using three 2 is to1multiplexer. Select lines S_0 and S_1 is worked as a switching input which is responsible for the high and low states of the transistor, S_0 is common input for gate terminal of PMOS_1, PMOS_2, NMOS_1 and NMOS_2, S_1 is common input for gate terminal of PMOS_3 and NMOS_3. Inputs are connected to the source terminal of transistor.

C. Design of 8-bitALU

FA is mainstays of ALU, 8-bit ALU is design using 8-bit ripple carry adder (RCA). RCA is responsible for arithmetic operation of ALU. Other modules needed for designing ALU are 2 is to 1 multiplexer and 4 is to 1 multiplexer. Logical operation executes by using multiplexer. Fig.5 depicts the1-bit ALU,1-bit ALU design using two 4 is to1multiple xer an done 2isto1multiple xer and FA.

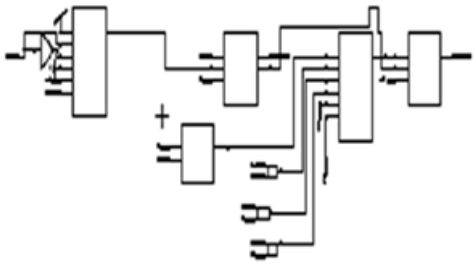

Fig. 5. 1-bit ALU

Fig. 6 depicts 8-bit ALU, RCA is basic building block of 8-bit ALU which is perform arithmetic operation. Input A (a_0,a_1,….a_8) is apply in first input of RCA, Input B (b_0,b_1,…b_8) is apply in first input of 4 is to 1 multiplexer and pass to the second input of RCA from output of 4 is to 1 multiplexer, and executes arithmetic operation. Logical operation executes through the cascading combination of 4 is to 1 multiplexer and 2 is to 1 multiplexer.

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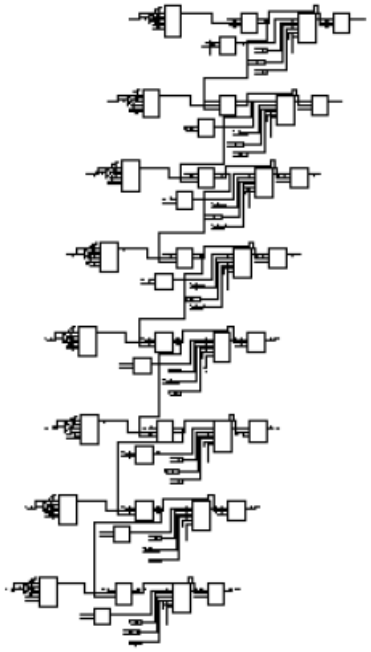

Fig. 6. 8-bit ALU

IV. SIMULATION ANDRESULT:

All the simulations are performed on Microwind and DSCH. The main focus of this work is to meet all challenges faces in designing of Arithmetic and Logic Unit (ALU) using Gate Diffusion Input (GDI) method based Adders and Multiplexers. This work develops a Gate Diffusion Input (GDI) design methodology for Arithmetic and Logic Unit (ALU), combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to CMOS. The simulation results are shown below figures.

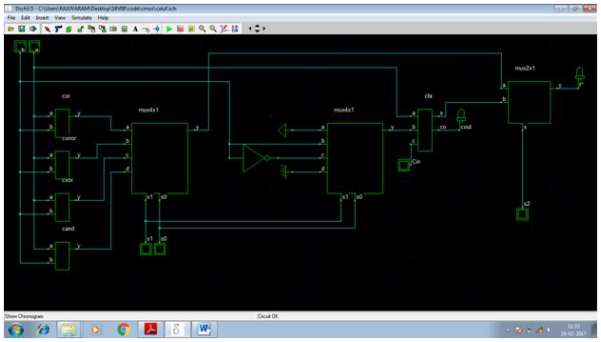

FIG1: Schematic of 1bit ALU using CMOS

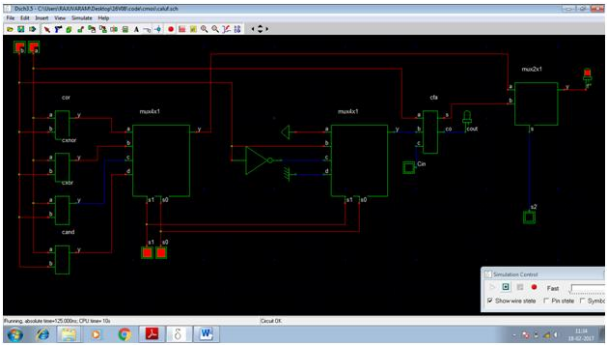

FIG2: Running simulation of 1bit ALU using CMOS

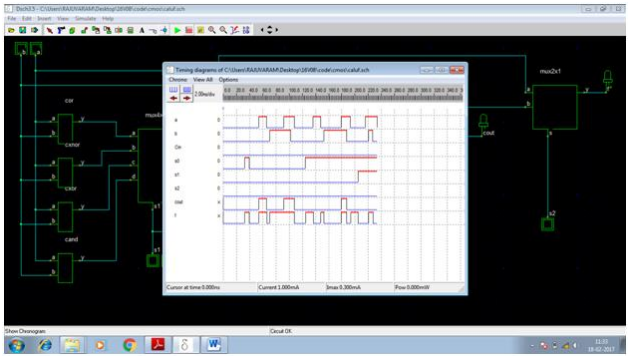

FIG3: Timing diagram of 1bit ALU using CMOS

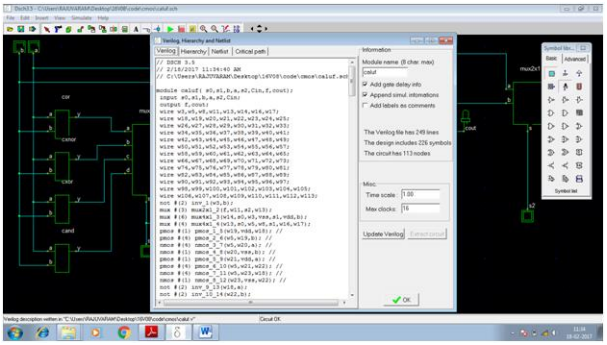

FIG4: Verilog file of 1bit ALU using CMOS

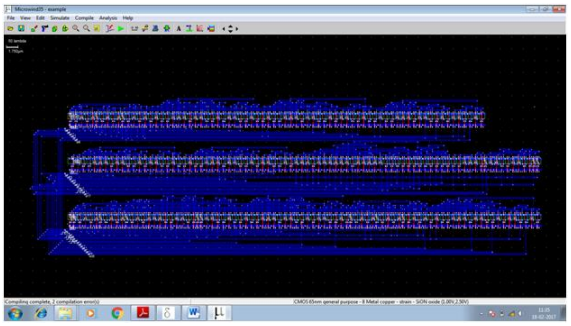

FIG5: Layout of 1bit ALU using CMOS

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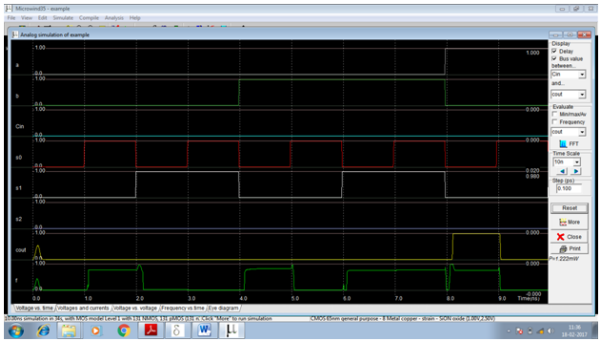

FIG6: simulation results of 1bit ALU using CMOS

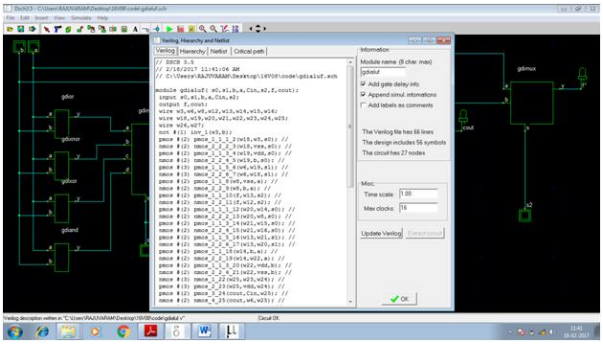

FIG10: Verilog file of 1bit ALU using GDI

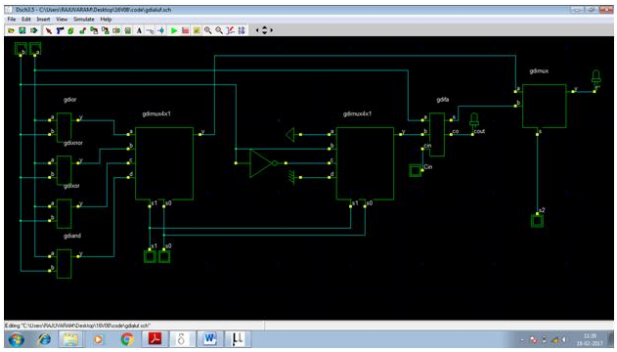

FIG7: Schematic of 1bit ALU using GDI

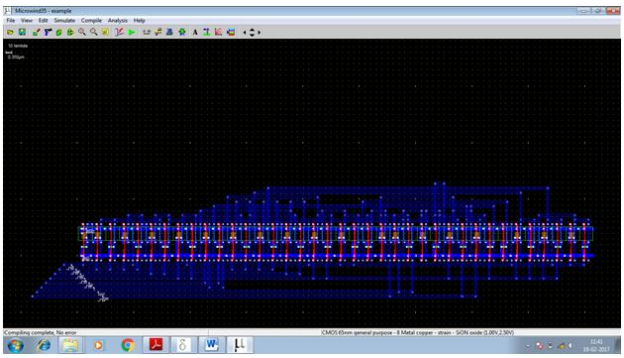

FIG11: Layout of 1bit ALU using GDI

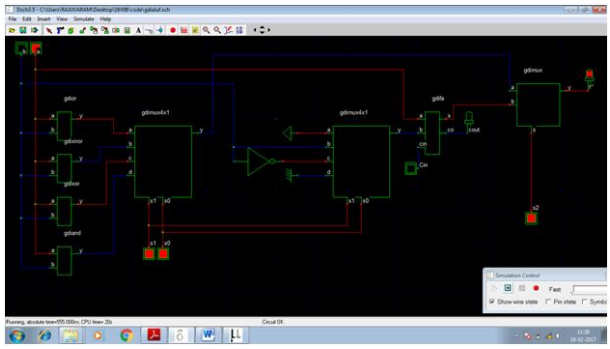

FIG8: Running simulation of 1bit ALU using GDI

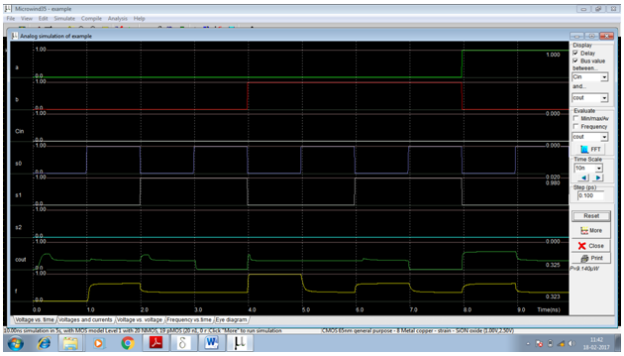

FIG12: simulation results of 1bit ALU using GDI

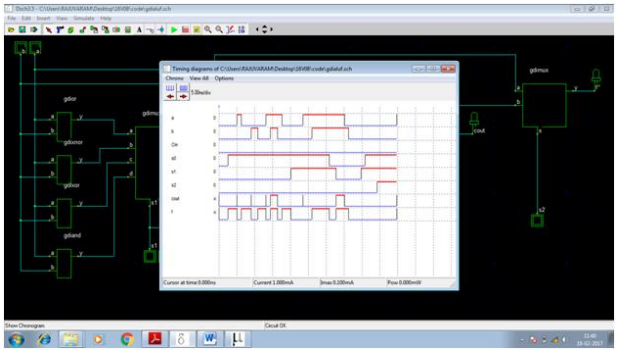

FIG9: Timing diagram of 1bit ALU using GDI

Table II and Table III shows the comparison between CMOS logic based design and proposed design with respect to power, delay and power delay product at 65nm technology. Using proposed logic, 8-bit ALU consumes 31% less power as compare to CMOS logic based 8-bit ALU and also minimizes the delay.

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TABLEII. CMOS LOGIC BASED DESIGN AT 65NMTECHNOLOGY

Design	No of transistors	Area(um^2)	Power(uW)
FA	28T	144.1	6.556
MUX2	20T	84.4	6.335
MUX4	60T	321.5	17.187
1-bit ALU	208T	1826.8	56.252
8-bit ALU	1664T	20748.9	200.10

TABLE III.PROPOSED LOGIC BASED DESIGN AT 65NM TECHNOLOGY

Design	No of transistors	Area(um^2)	Power(uW)
FA	11T	60.6	1.850
MUX2	2T	13.5	0.0
MUX4	6T	39.4	0.0
1-bit ALU	39T	249.8	9.06
8-bit ALU	312T	3763.1	48.205

CONCLUSION:

In this paper, 8-bit ALU design using 11-T FA and GDI based multiplexer at 65nm technology. By using FA and multiplexer, we have reduced power and delay of 8-bit ALU as compare to existing design. All design were simulated using DSCH and Microwind 3.5 in 65 nm BSIM4 technology. Performance analyses were done with respect to power and area. Finally, 8-bit ALU performs better as compare to existing design and consumes low power.

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