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Performance Analysis of an Energy Efficient Level Shifter Using MTCMOS Technology

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ABSTRACT
The level shifters play a crucial role in the circuits and systems with multi supply voltages. In this paper, level shifter is proposed which is energy efficient, in order to achieve the above threshold voltage from the sub-threshold voltage conversion. It is a circuit with hybrid structure consisting of the cross- coupled level shifter and Wilson current mirror circuit. Significantly, the leakage power is reduced by addressing the voltage drop issue of the level shifter based on the Wilson current mirror, with the advantage of wide input voltage range for the Wilson current mirror level shifter. In addition to that, the multi-threshold CMOS (MTCMOS) technology is introduced to provide flexibility for our ultra-low power design. The simulation results were obtained by simulating the design using 65nm CMOS process which validates our proposed implementation and without the need of any intermediate power supply, an ultra-low power consumption of 5.6 uJ per conversion from 0.2 V to 1 V at 1MHz is achieved.

I. INTRODUCTION
Multi-supply voltage domain technique is effective method to reduce power dissipation. In this technique, the design is partitioned into separate voltage domains, where each domain is operating at distinct power supply levels. Voltage level shifter is a circuit which converts the signal from one voltage level to another. To interface various domains in multi-supply voltage design, voltage level shifter is used. At the boundaries of different voltage islands on the system-on-chip (SOC) voltage level shifter is used. Voltage level shifter is a device which converts one voltage level to another. Voltage level shifters are used to interface various circuit blocks operating at different supply voltages. The multi-threshold voltage CMOS technique is used in the design of voltage level shifter in order to reduce delay and power. Low-threshold voltage devices are used to reduce delay and power dissipation is reduced with the use of high threshold voltage devices.

II. CONVENTIONAL METHODS
At present there are two conventional designs that are proposed for the implementation of level shifter: the cross coupled structure and the current mirror structure.

II. I CROSS-COUPLED STRUCTURE:
The cross coupled level shifter in Fig. 1 (a) takes significant advantage of the full output swing generated by a positive feedback. The major limiting issue for this design is that the driving strength for the NMOS pair (MN1 and MN2) is much weaker than that of the PMOS pair, when the input is below the threshold voltage of the NMOS pair. This result in the failure of the output's toggling. Although the driving strength can be improved by greatly upsizing the NMOS pair but results in large area and load capacitance.

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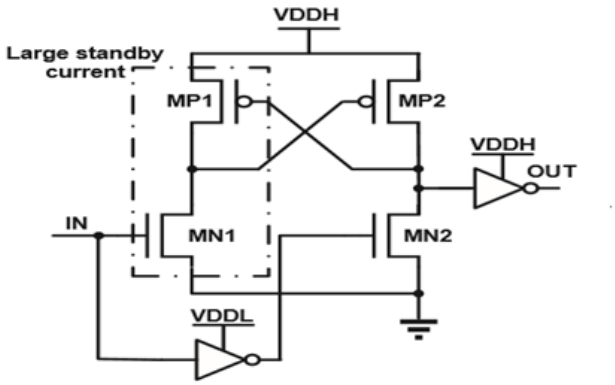

FIGURE 1: CROSS COUPLED STRUCTURE

II.II CURRENT MIRROR CIRCUIT:

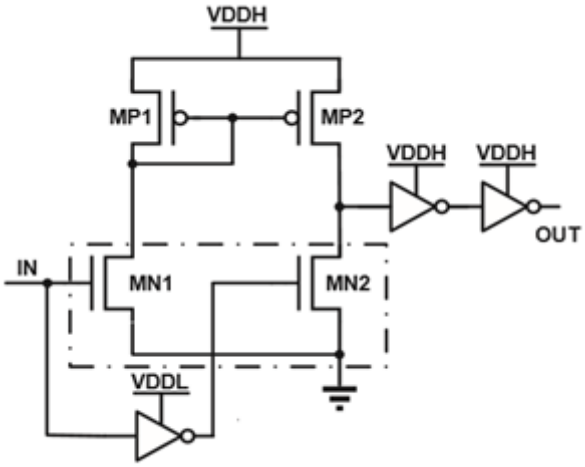

FIGURE 2: CURRENT MIRROR STRUCTURE

Fig: 2 shows a topology that uses a current mirror to level shift before the output buffer. However, the static current flowing through MP1 and MN1 consumes large static power when the input is high. To reduce this static current, the Wilson current mirror based level shifter was proposed.

II.III WILSON CURRENT MIRROR CIRCUIT:

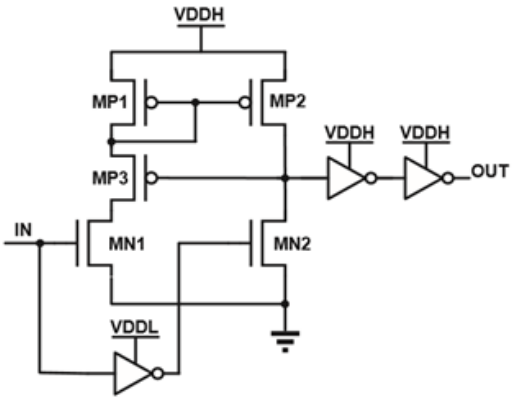

FIGURE 3: WILSON CURRENT MIRROR STRUCTURE

In Wilson current mirror based level shifter a feedback PMOS (MP3) is added to reduce the static current. However, before the output buffer, the feedback by MP3 introduces a voltage drop (i.e. V_{gs} of MP3) below VDDH, which can cause large static current in the buffer. The voltage drop can be reduced by upsizing MP3; nevertheless, it can result in increment of both the delay and power consumption for the high-to-low transition.

III. PROPOSED CIRCUIT:

In this paper, we present an energy-efficient level shifter with a wide input voltage range. It is a hybrid structure of the Wilson current mirror based level shifter and the conventional cross-coupled level shifter. The level shifter based on the Wilson current mirror, the leakage power is significantly reduced; while the advantage of wide input voltage ranges for the Wilson current mirror level shifter is well-preserved. Specifically, the voltage drop of the Wilson current mirror based level shifter before the output buffer is compensated by the cross-coupled level shifter, while the input for the cross-coupled level shifter is raised up near or above threshold to reduce the power dissipation and delay. Additionally, the multi-threshold CMOS (MTCMOS) devices are adopted to further reduce the power consumption.

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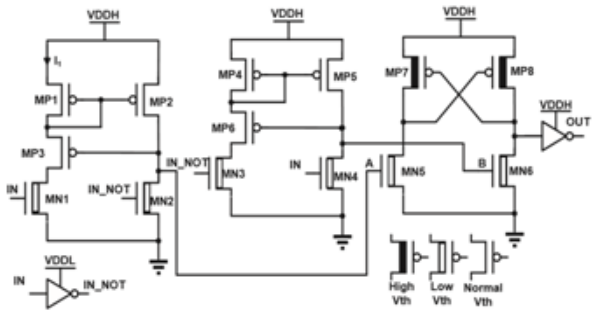

FIGURE 4: HYBRID STRUCTURE

III.I. PROPOSED LEVEL SHIFTER IMPLEMENTATION:

The MTCMOS technique is employed in the design to optimize the delay and the power consumption. The proposed level shifter mainly consists of two Wilson current mirrors as its initial level-up stage, and a cross coupled structure as its output stage. The differential inputs are generated by an inverter with low threshold voltage V^{th}, featuring a shorter delay. Moreover, the Wilson current mirrors raise the input voltage to a voltage near or above the threshold of the NMOS. In order to reduce the power consumption, the lengths of PMOS transistors in the current mirror are larger than the process feature size. The W/L ratios of the output transistors MP2, MN2, MP5 and MN4 for the current mirror can be increased, in order to achieve a higher speed. The full swing of the output is maintained by the following cross coupled structure, and the pull-down strength is improved by using low V^{th} NMOS for MN5 and MN6, while the active current is limited by using high V^{th} PMOS for MP7 and MP8.

III.II OPERATION:

The low supply voltage and the high supply voltage are set to be 0.2 V and 1.2 V, respectively. The differential inputs IN and IN NOT generated from the inverter stage are at the frequency of 1 MHZ. If IN is high and IN NOT is low, MN1 is turned-on. The current I1 can flow through MP1, MP3 and MN1. This current is then mirrored and flows through MP2. AsMN2 is off, the node A will be charged until MP3 is turned-off. If IN is low and IN NOT is high, the MN1 is off and MN2 is on. Since there is no current flow through MP1, MP3 and MN1, the node A will be discharged and the other Wilson current mirror will generate a complementary waveform of node A at node B as shown in Fig. 4. As a result, IN and IN NOT are leveled-up at A and B by the Wilson current mirror stages, with the high voltage level at A or B having a voltage drop due to the off-biased PMOS transistors. In addition, the cross-coupled structure further raises the high level voltage to VDDH (i.e. 1.2 V), as shown in Fig. 4. A and B can easily exceed the drive strength of the corresponding PMOS transistors MP7 and MP8 for successful toggling, resulting from that A or B has a high level voltage of above or near threshold of the NMOS MN5 and MN6. It is noted that the high level voltage at node A and B should be well-determined. If it is too high, the power consumption for the whole level shifter will be large. On the other hand, if it is too low, MP7 and MP8 should be exponentially upsized to enable the successful transition.

TABLE 1

TRANSISTOR TYPES AND SIZES FOR THE PROPOSED LEVEL SHIFTER.

Transistor	Type	W/L (nm)	Transistor	Type	W/L (nm)
MP1	nvt	120/650	MP2	nvt	120/550
MN1	lvt	120/60	MN2	lvt	350/60
MP3	nvt	120/60	MP6	nvt	120/60
MP4	nvt	120/650	MP5	nvt	120/550
MN3	lvt	120/60	MN4	lvt	350/60
MP7	hvt	120/1500	MP8	hvt	120/1500
MN5	lvt	120/60	MN6	lvt	120/60
MP11*	lvt	1200/60	MN11*	lvt	1200/60
MP12*	nvt	120/600	MN12*	nvt	120/600

* *MP11* and *MN11* are for the input buffer. *MP12* and *MN12* are for the output buffer.

III.III DESIGN TOOLS AND IMPLEMENTATION

In order to design a schematic diagram of the circuit we use S-EDIT from the Tanner EDA tool. The highest level entity in the S-Edit schematic database hierarchy is the design. A design contains many cells, some of which may be referenced from a library. Most often a cell will contain a single interface, which contains a single symbol view and a single schematic view. However, a cell can contain any number of interfaces, and each interface can contain any number of symbol views and schematic views.

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The schematic generated in S-EDIT in exported to T-SPICE in order to simulate the design and to get the waveforms. . This T-SPICE generates a net list about the different logic devices used and this Net list is loaded into H-SPICE and model parameters of 90nm technology are added to it and it in run in H-SPICE window. Average power commands are used so as to produce average power dissipation values.

IV. SCHEMATICS AND PERFORMANCE ANALYSIS

The schematics drawn in tanner tools are shown below along with the simulated waveforms obtained using Avan waves in H-spice simulation.

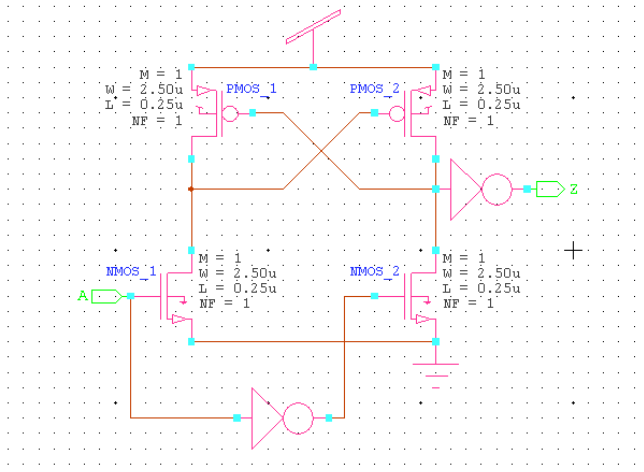

FIGURE 5: SCHEMATIC OF CROSS COUPLED CIRCUIT

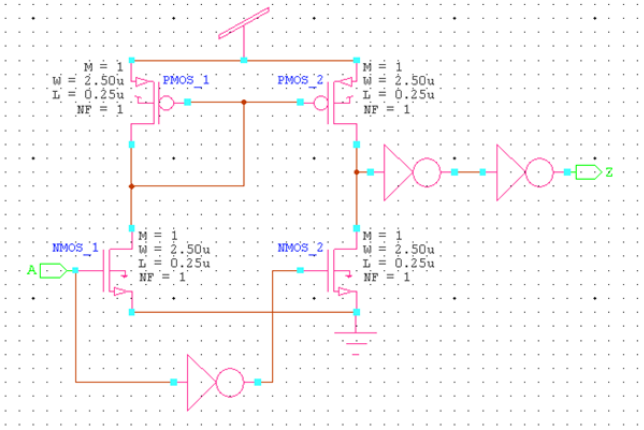

FIGURE 6: SCHEMATIC OF CURRENT MIRROR CIRCUIT

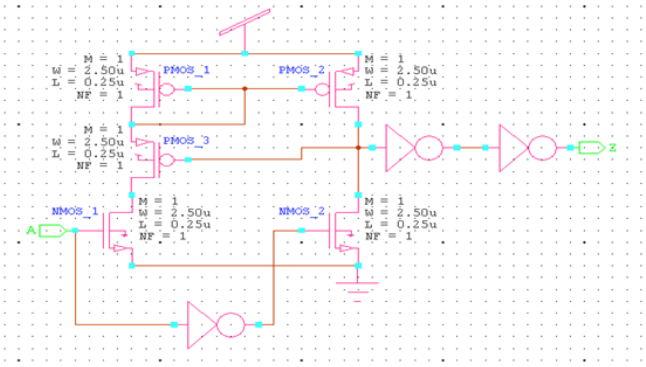

FIGURE7: SCHEMATIC OF WILSON CURRENT MIRROR CIRCUIT

FIGURE8: SIMULATED WAVEFORMS OF WILSON CURRENT MIRROR CIRCUIT

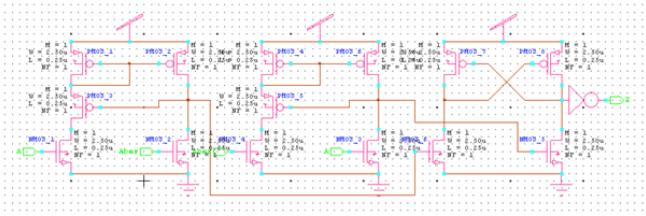

FIGURE 9: SCHEMATIC OF PROPOSED LEVEL SHIFTER

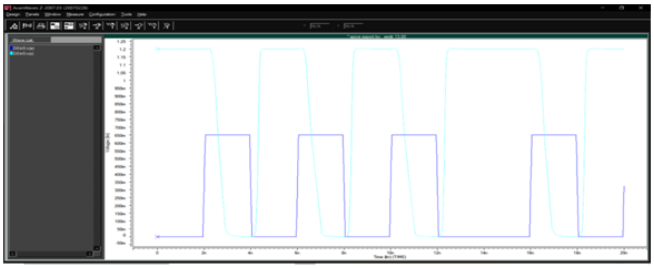

FIGURE10: SIMULATED WAVEFORMS OF PROPOSED HYBRID STRUCTURE FOR 1.2V

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TABLE 2 COMPARISION OF VARIOUS DESIGNS

Average Power(μW) Model/Voltage	0.2V (nW)	0.4V (uW)	0.6V (uW)	0.8V (uW)	1V (uW)
CROSS COUPLED	40.4	1.2	1.5	3.79	12.3
CURRENT MIRROR	70.3	1.4	6.4	13.7	23.9
WILSON CURRENT MIRROR	335.4	2.1	6.9	17.1	44.18
PROPOSED LEVEL SHIFTER	25.58	0.19	1.35	20.03	43.78

V. CONCLUSION:

This paper presents a novel energy-efficient sub-threshold level shifter design. To overcome the drawbacks of the two structures i.e., the Wilson current mirror and cross-coupled level shifter, the proposed hybrid structure combining the Wilson current mirror and cross-coupled level shifter takes the advantages. In addition, MTCMOS devices are applied to achieve low power consumption. The simulation results shows that it only consumes 19.44 fJ per conversion for 0.2 V to 1.2 V conversions at an operating frequency of 1 MHz, with the input high voltage level as low as 85 mV using 65 nm CMOS technology. Schematics using Tanner tools were drawn and corresponding waveforms were simulated in H-Spice and also Average power, delay, power delay product are compared for various designs and among those the proposed level shifter has the least power delay product. As a result, this energy-efficient level shifter with a wide input range can find applications in the interfaces between sub-threshold and above threshold voltage modules.

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