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Synthesis and Simulation of Look-Ahead Clock Gating Technique

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Abstract:

Clock gating is very useful for reducing the power consumed by digital systems. Three gating methods are known. The most popular is data driven-based, latch based and Andgate based. It unfortunately leaves the majority of the clock pulses driving the flipflops (FFs) redundant. A data-driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called and-gate based is simple but yields relatively small power savings. This paper presents a novel method called Look-Ahead Clock Gating Technique, which combines all the three. Latch based FFs computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends.

It avoids the tight timing constraints of Look-Ahead Clock Gating Technique by allotting a full clock cycle for the computation of the enabling signals and their propagation. A closed-form model characterizing the power saving per FF is presented. It is based on data-to-clock toggling probabilities, capacitance parameters and FFs' fan-in. The model implies a breakeven curve, dividing the FFs space into two regions of positive and negative gating return on investment. While the majority of the FFs fall in the positive region and hence should be gated, those falling in the negative region should not.

Simulation process is using modelsim 6.5e and synthesis process is using Xilinx 12.1i. Experimentation on industry-scale data showed 22.6% reduction of the clock power, translated to 12.5% power reduction of the entire system.

Key words:

Clock gating, clock networks, dynamic power reduction.

I.INTRODUCTION:

One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30% to 70% of the total dynamic (switching) power consumption. Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal regardless of whether or not their data will toggle in the next cycle. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals. Clock gating is employed at all levels: system architecture, block design, logic design and gates. Several methods to take advantage of this technique are described, with all of them relying on various heuristics in an attempt to increase clock gating opportunities.

We call the above methods data driven based. Synthesis-based clock gating is the most widely used method by EDA tools. The utilization of the clock pulses, measured by data-to-clock toggling ratio, left after the employment of synthesis-based gating may still be very low. Fig. 1 depicts the average data-to-clock toggling ratio, obtained by extensive power simulations of 61 blocks comprising 200k FFs, taken from a 32 nm high-end 64-bit microprocessor. Those are mostly control blocks of the datapath, register file and memory management units of the processor.

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The technology parameters used throughout the papers are of 22 nm low-leakage process technology. Their clock enabling signals were derived by a mix of logic synthesis and manual definitions. The clock capacitive load is 70% of their total load. The blocks are increasingly ordered by their data-to-clock activity ratio. It is clearly shown that the data toggles in a very low rate compared to the gated clocks. Point (a) shows that in 87% of the blocks (53/61) the data toggles less than 6% compared to the gated clock, where the average shown by the horizontal dashed line is 3%. Also plots the corresponding cumulative clock capacitive load.

Point (b) shows that the above 87% blocks are responsible for 95% of the total clock load. Consequently, the switching of a significant portion of the system's clock load is redundant, but consumes most of its power. This calls for other than synthesis-based methods to address the above redundancy, a method called data-driven clock gating was proposed for flip-flops (FFs). There, the clock signal driving a FF, is disabled (gated) when the FF's state is not subject to change in the next clock cycle [9]. In an attempt to reduce the overhead of the gating logic, several FFs are driven by the same clock signal, generated by ORing the enabling signals of the individual FFs [8]. Based on the data-to-clock toggling probability, a model to derive the group size maximizing the power savings was developed.

A comparison between the synthesis-based and data-driven gating methods showed that the latter outperforms for control and arithmetic circuits, while the former outperforms for register-file based circuits. Data-driven gating is illustrated in Fig. 2. A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The outputs of XOR gates are ORed to generate a joint gating signal for FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is used by commercial tools and is called Integrated Clock Gate (ICG).

It is beneficial to group FFs whose switching activities are highly correlated. The work in [10] addressed the questions of which FFs should be placed in a group to maximize the power reduction, and how to find those groups. Data-driven gating suffers from a very short time-window where the gating circuitry can properly work.

This is illustrated in Fig. 3. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF. Such constraints may exclude 5%-10% of the FFs from being gated due to their presence on timing critical paths [10]. The exclusion percentage increases with the increase of critical paths, a situation occurring by downsizing or turning transistors of non-critical path to high threshold voltage (HVT) for further power savings.

II. Look-Ahead Clock Gating Technique:

LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation. LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs. Similarly to data-driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timingConstraints of AGFF and data-driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gaters. Furthermore, unlike data-driven gating whose optimization requires the knowledge of FFs' data toggling vectors, LACG is independent of those. The embedding of LACG logic in the RTL functional code is uniquely defined and easily derived from the underlying logic, independently of the target application. This simplification is advantageous as it significantly simplifies the gating implementation.

LACG is based on using the XOR output in Fig 5.1 to generate clock enabling signals of other FFs in the system, whose data depend on that FF. There is a problem though. The XOR output is valid only during a narrow window [t setup, tccq] of around the clock rising edge, where t and t are the FF's setup time and clock to output contamination delay, respectively. After a t ccq setup delay the XOR output is corrupted and turns eventually to zero. To be valid during the entire positive half cycle it must be latched as shown in Fig is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input clk_g. Such gating has been proposed in [10] and it involves another XOR and OR gates, useful for high clock switching probability.

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It is subsequently shown that clk_g probability is very low and it is therefore not further being gated.The working and functioning of look ahead clock gating by using auto-gated flip flops can be understood by observing the Fig 5.1.This method aims at reducing the drawbacks encountered in the previous systems. Look-ahead clock gating has been shown to be very useful in reducing the clock switching power.

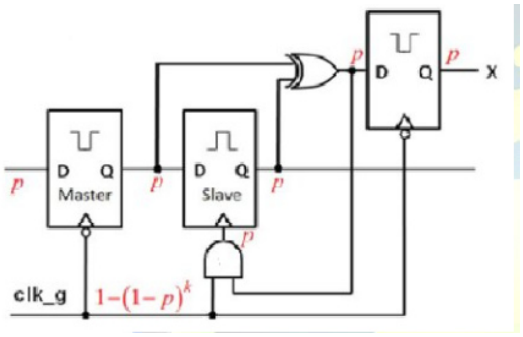

Fig1: Enhanced AGFF Used For LACG Flop

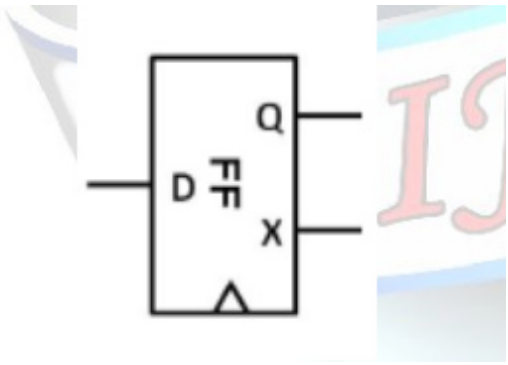

Fig2: Symbol For Enhanced AGFF

We call FF" target and FF' source. A target FF depends on K>1 source FFs. It is required that the logic driving a target FF does not have an input externally of the block. Let X(D") denote the set of the XOR outputs of the source FFs, and denote by Q(D") the set of their corresponding outputs. The source FFs can be found by a traversal of the logic paths from D" back to Q(D"),which can be performed either in the RTL or the net-list descriptions of the underlying system. The logic tree with root and leaves is sometimes called the logic cone of D". Using a FF for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating FF"' as shown in Fig.5.3 since FF"' is oppositely clocked and its data is sampled at the clock's falling edge, its clock enabling signal X"' must be negated. Also, FF"' is an ordinary FF where the internal XOR gate is connected.

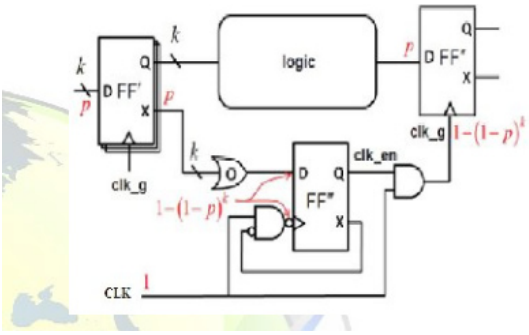

Fig3: LACG Of General Logic

Modelling the Power Savings:

Let X be a random variable of the FF's data-to-clock toggling (hereby data toggling) and let p=Pr[X=1] be its probability. Assuming that FFs are toggling their data independently of each other, there exists Independency is a worst case assumption. In reality toggling correlation exists, which may increase the actual power savings obtained by the subsequent analysis [10]. It follows from X independency that the probability of enabling the clock while it could be disabled is The power savings is formulated in terms of capacitance and data toggling probability. The power savings is formulated in terms of capacitance and data toggling probability .Frequency and voltage do not matter for relative savings calculation.

The product of capacitance and data toggling probability is called in VLSI jargon as dynamic capacitance or cdyn for short. Let be the clock input capacitance of a FF, and let cFF+CLK FF include also the clock driver and its interconnecting wire capacitance. We charge 1/3 of c FF+CLK to each of the three latches comprising the AGFF in Fig 5.1 The saved cdyn stems from the low clocking rate of the master and slave latches shown in Fig probability, while otherwise those would have been clocked in one probability.

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III. BLOCK DIAGRAM

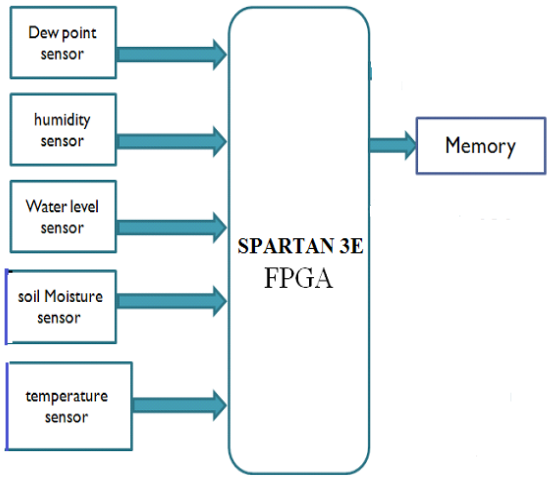

Fig4: Block diagram

Temperature sensors:

Temperature sensors are devices used to measure the temperature of a medium. There are 2 kinds on temperature sensors: 1) contact sensors and 2) noncontact sensors. these sensors measure a physical property which changes as a function of temperature. In these project a digital temperature is being used. The digital temperature sensors features low power consumption, up to 12 bit resolution and can operate over a temperature range as wide as -55 to +125°C.

Humidity sensors:

A humidity sensor measures the relative humidity and expressed as a percent (RH %). It is the ratio of actual moisture in the air to the highest amount of moisture in air can hold at that temperature. The most common type of humidity sensor used is the "capacitive sensor." This sensor is based on electrical capacitance . The sensor is composed of two metal plates with a non-conductive polymer film between them. The film collects moisture from the air, and the moisture causes minute changes in the voltage between the two plates. The changes in voltage are used to know the amount of moisture in the air. Humidity sensors are of three types. Resistive, Capacitive, and Thermal Conductivity sensing. Resistive sensors are useful in remote locations. Capacitive sensors are useful for wide RH range and condensation tolerance. Thermal conductivity sensors are beneficial in corrosive environments that have high temperatures.

IV. SIMULATION RESULTS

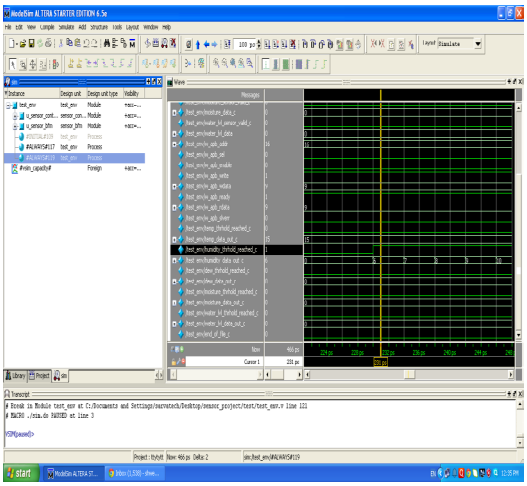

Fig5: simulation results using modelsim

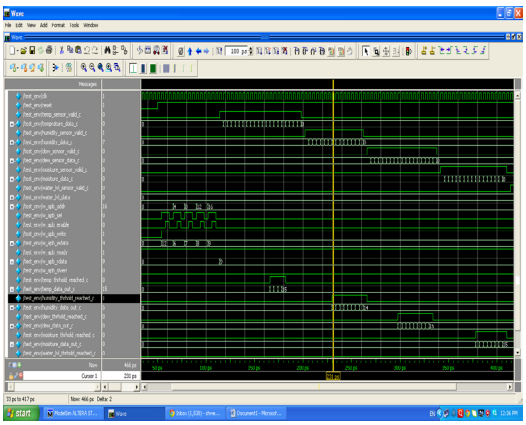

Fig6: simulation results

V. SYNTHESIS RESULTS

Synthesis Results using Xilinx

Block Diagram:

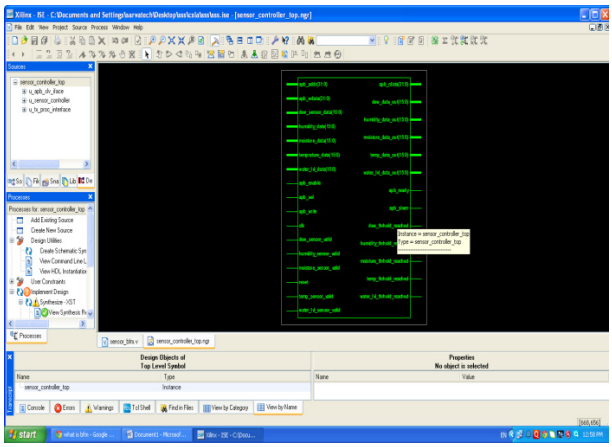

Fig7: synthesis results

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VI. CONCLUSION:

Look-ahead clock gating has been shown to be very useful in reducing the clock switching power. The computation of the clock enabling signals one cycle ahead of time avoids the tight timing constraints existing in other gating methods. A closed- form model characterizing the power saving was presented and used in the implementation of the gating logic. The gating logic can be further optimized by matching target FFs for joint gating which may significantly reduce the hardware overheads. While this paper discussed the case of merging two target FFs for joint gating, clustering target FFs in larger groups may yield higher power savings. This is a matter of a further research.

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