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Design of a Single Phase Clock Multiband Flexible Divider Using Low Power Techniques

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Abstract:

The frequency synthesizer is implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider which consumes a large portion of power in a frequency synthesizer. To reduce this power consumption A Low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers is proposed based on pulse-swallow topology and is implemented using a 0.18-µm CMOS technology.

The multiband divider consists of a proposed wideband multi-modulus 32/33/47/48 prescaler and an improved bit-cell for swallow counter operates in 2.4- and 5-GHz resolution selectable from 1 to 25 MHz and verified. There are few methods to reduce this static power consumption. But they have drawbacks such as sacrificing design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using Low power Techniques like Sleep Transistor Approach, Dual Stack, Sleepy P, and Sleepy N.

Keyword:

DFF, dual modulus prescaler, dynamic logic, E-TSPC, frequency synthesizer, high-speed digital circuits, true single-phase clock (TSPC), wireless LAN (WLAN).

I.INTRODUCTION:

Wireless LAN (WLAN) in the multi gigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized for high-rate data transmissions, and standards like network protocol IEEE 802.15.4 are recognized for low-rate data transmissions. The demands for low-power low-cost wireless radio-frequency transceivers.

The frequency synthesizer is implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in [1] and [2] consume up to 25mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and it has a narrow locking range.The frequency synthesizer at 5 GHz consumes 9.7mW at 1-V supply, where its complete divider consumes power around 6mW [4], where the first-stage divider is implemented using the source-coupled logic (SCL) circuit [5], which allows higher operating frequencies but uses more power.Dynamic latches are faster and consume less power compared to static dividers. The TSPC [6] and E-TSPC [6] designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem [5]. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz [8], [9]. In the previous design [1], a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodu-lus32/33/47/48. In this paper a new method for designing a dynamic logic multiband flexible divider has been proposed which uses a sleep transistor, it reduces static power in frequency divider with different low power techniques.

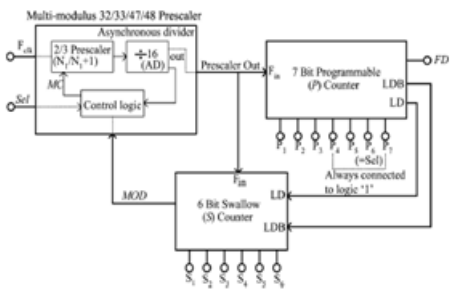

Fig 1:A dynamic logic multiband flexible divider

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II. DESIGN CONSIDERATIONS:

In the case of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

fmax = 1/ (tpLH + tpHL) (1)

where tpLH and tpHL are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. In CMOS digital circuits, the total power consumption is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

Pswitching = ∑ni=1fclkCLiV2dd (2)

where n is the number of switching nodes, fclk is the clock frequency, CL is the load capacitance at the output node of the i th stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

Psc = Isc * Vdd (3)

where Isc is the short-circuit current. The short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-um CMOS process.

III. WIDEBAND E-TSPC 2/3 PRESCALER:

The E-TSPC 2/3 prescaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single phase clock 2/3 prescaler used in this design was reported in [10]. which consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Fig. 2.

The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2. By embedding the two NOR gates into the DFF's, the number of stages has been reduced , which consequently reduces the propagation delay from the input node to output node. Here, the additional transistors M2,M¬25, M4, and M8 are added in DFF1 to eliminate the short-circuit power during the divide-by-2 operation.

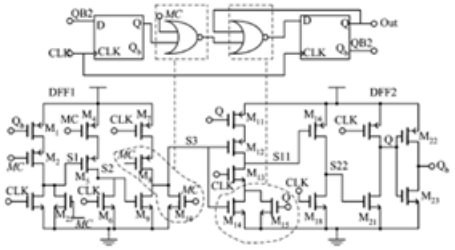

Fig. 2. Wide band single phase clock 2/3prescaler

The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

CL¬_wideband = Cdb M 19 + 2Cgd M 19 + CdbM21 + 2CgdM21 +
CgM1 (4)

When MC=1, transistor M10 turns on, transistors M2, M4 and Ms in DFF1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

Pwideband_divide_by_2=∑4i=1fclkCLiV2dd+Psc1+Psc2 (5)

When logic signal MC =0, transistor M10 turns-off the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode.

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During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1.

IV. MULTIMODULUS 32/33/47/48 PRESCALER:

The proposed wideband multi-modulus prescaler is similar to 32/33, but with an additional inverter and a multiplexer. This proposed prescaler can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 3. It performs additional divisions (divide- by-47 and divide-by-48) without adding any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V.

The multimodulus prescaler consists of the wideband 2/3 (N1/ (N1+1)) prescaler [10], four asynchronous TSPC divide-by-2 circuits ((AD=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+1) divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

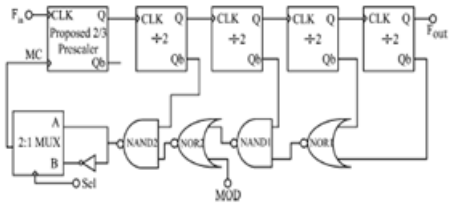

Fig 3:Proposed multimodulus 32/33/47/48 Prescaler.

A. Case 1: Sel= '0'

When Sel='0' the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide- by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD * N1) + (0*(N1+1)) = 32 \quad (6)$$

Where N1=2 and AD= 16 is fixed for the entire design. If MOD=0, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N+1 performed by the multimodulus prescaler is

$$N+1 = ((AD-1)* N1) + (1 * (N1+1)) = 33 \quad (7)$$

B. Case 2: Sel = 1

When Sel = 1, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC =1, the 2/3 prescaler operates in divide-by-3 mode and when Sel =0, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when Sel=0. If MOD=1, the division ratio N+1 performed by the multimodulus prescaler is same as (6) except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N+1 = (AD * (N1+1)) + (0* N1) = 48 \quad (8)$$

If M O D=1, the division ratio N performed by the multimodulus prescaler is

$$N= ((AD-1) * (N1 +1)) + (1*N1) = 47 \quad (9)$$

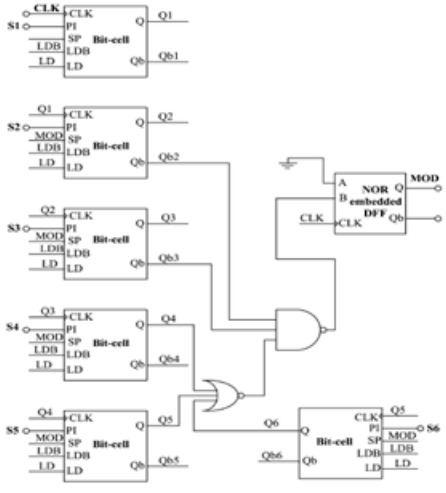

Fig 4: Asynchronous 6-bit S-counter.

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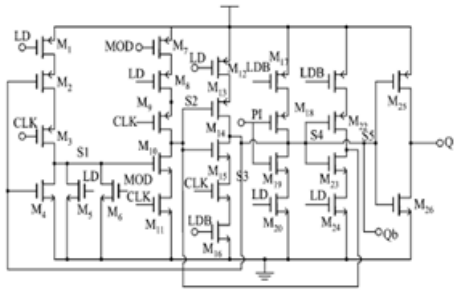

Fig 5: Asynchronous loadable bit-cell for S-counter.

B. Programmable (P) Counter:

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells [13] and additional logic gates as in [7]. Here, bit P7 is tied to the Sel signal of the multimodulus prescaler and bits P4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33(N/(N+1)) dual-modulus prescaler is used, a 7-bit P-counter is needed for the low-frequency band (2.4 GHz) while an 8-bit P-counter would be needed for the high-frequency band (5–5.825 GHz) with a fixed 5-bit S-counter. Thus, the multimodulus 32/33/47/48 prescaler eases the design complexity of the P-counter.

1) Sel=0 (2.4–2.484 GHz): When logic signal Sel=0, the multimodulus prescaler acts as a 32/33 prescaler, the P-counter is programmable from 64 to 127 (bit P7 of the P-counter always remains at logic "1"), and the S-counter is programmable from 0 to 31 to accommodate division ratios from 2048 to 4095 with finest resolution of 1MHz. However, since we are interested in the 2.4-GHz band, bit P6 of the P-counter always remains at logic "0," since it is tied to the logic signal Sel, allowing it to be programmable from 75 to 78. Bit S6 of the S-counter is kept at logic '0' (to satisfy the conditions N>S), allowing a programmable division from 0 to 31 for the low-frequency band of operation to accommodate division ratios between 2400 and 2484 with a resolution of 1 MHz for Bluetooth and Zigbee applications [7] and 5 MHz for the IEEE 802.15.4 frequency synthesizer [8] with a fixed reference frequency of 1MHz. Since the finest resolution and reference frequency is 1 MHz, different channel spacing can be achieved by programming S-counter in steps of 1. For example, 5-MHz channel spacing is achieved by programming S-counter in steps of "5" keeping the flexible divider resolution and reference frequency to 1MHz. The frequency division (SD) ratio of the multiband divider in this mode is given by

$$FD = (N+1)* S+N * (P-S) = NP+S \quad (10)$$

2) Sel= '1' (5–5.825 GHz): When logic signal Sel='1', the multimodulus prescaler acts as a 47/48(n/(N+1)) prescaler, the P-counter is programmable from 64 to 127 (bit P7 of the P-counter always remains at logic "1"), and the S-counter is programmable from 0 to 48 to accommodate division ratios from 3024 to 6096 with finest resolution of 1MHz. However, since we are interested in 5–5.825 GHz band, bit P6 of the P-counter always remains at logic "1," allowing it to be programmable from 105 to 122. The S-counter is programmable from 0 to 48 for the high frequency band of operation to accommodate division ratios between 5000 and 5825 with a resolution of 5 MHz. The frequency division (FD) ratio of the multiband divider in this mode is given by

$$FD = (N*S) + (N+1)* (P-S) = (N+1)P - S \quad (11)$$

VI DIVIDER USING LOW POWER TECHNIQUES:

A new method for designing a dynamic logic multiband flexible integer-N-divider has been proposed which was developed using a sleep transistor based and wideband multimodulus 32/33/47/48 prescaler with low-power wideband 2/3 prescaler and an integrated S and P counter.

(i)Sleepy P & Sleepy N techniques

A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply". The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit. The sleepy p &sleepy N provides good leakage power reduction. However when it enters in to sleep mode it loses the state information. This technique can be applied to only pull down or pull up circuit. This methodology is shown in figure 6, 7. Though this circuit utilizes one less sleep transistor at obvious area advantage.

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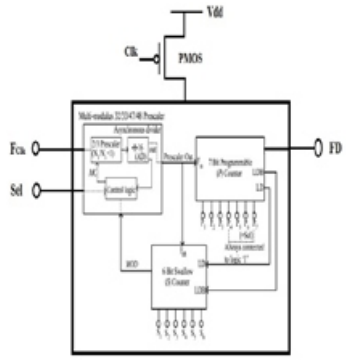

Fig 6: Proposed dynamic logic multiband flexible divider using Sleepy P transistor

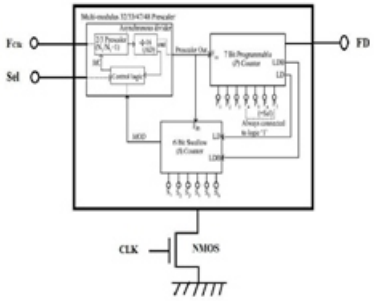

Fig 7: Proposed dynamic logic multiband flexible divider using Sleepy N transistor.

(ii)Sleep transistor approach:

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-down networks and ground while for fast switching speeds, low-Vth transistors are used in logic circuits. this technique dramatically reduces leakage power during sleep mode. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values.

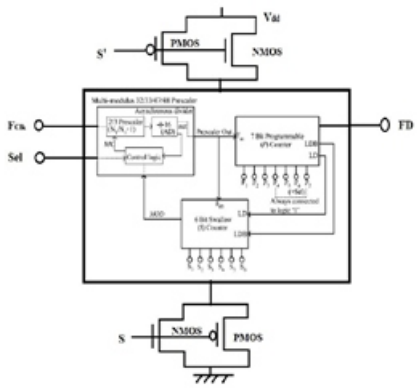

Fig 8: Proposed dynamic logic multiband flexible divider using Sleepy transistor approach

(iii)Dual Stack Approach :

In dual stack approach, 2 PMOS in the pull- down network and 2 NMOS in the pull-up network are used. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Compared to previous approaches it requires greater area. The delay is also increased. Figure 9 shows the configuration of dual stack method in case of a multiband flexible divider. In this method, there are two extra MOSFETS parallel to the sleep transistors. These transistors are stacked they help to reduce leakage power. Its operation is similar to the case of logic circuits. We apply S=1 when the circuit is in active mode and S=0 when it is in sleep mode.

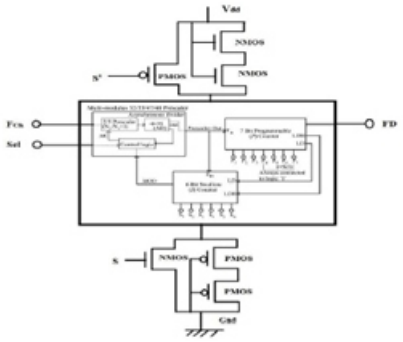

Fig 9: Proposed dynamic logic multiband flexible divider using dual stack technique

VII SIMULATION RESULTS:

The simulations of the designs are performed using H-Spice tool.Fig 10 shows the simulation results for proposed dynamic logic multiband flexible divider using Sleepy P transistor.

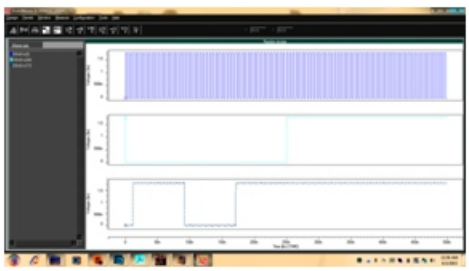

Fig 10: Simulation results for proposed dynamic logic multiband flexible divider using Sleepy P transistor.

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Fig 11 shows the simulation results for proposed dynamic logic multiband flexible divider using Sleepy N transistor.

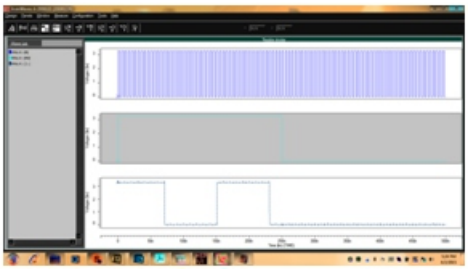

Fig 11: Simulation results for proposed dynamic logic multiband flexible divider using Sleepy N transistor

Fig 12 shows the simulation results for proposed dynamic logic multiband flexible divider using Sleepy transistor approach.

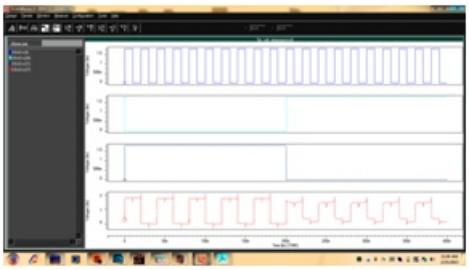

Fig 12:Simulation results for Proposed dynamic logic multiband flexible divider using Sleepy transistor approach.

Fig 13 shows the simulation results for proposed dynamic logic multiband flexible divider using dual stack technique.

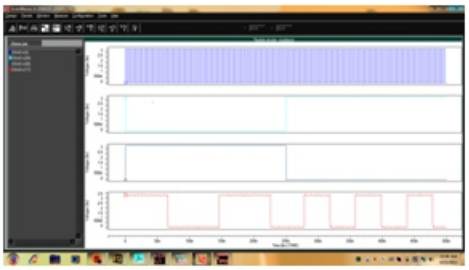

Fig 13: Simulation results for Proposed dynamic logic multiband flexible divider using dual stack technique.

After the simulation of all structures the performance of those designs is analyzed and formulated as a table which is shown in Table 1.

Table I: Performance of different dividers

	Previous Work	Sleepy P	Sleepy N	Sleep Transistor Approach	Dual Stack
Technology	180nm	180 nm	180nm	180nm	180nm
Supply Voltage(V)	1.8	1.8	1.8	1.8	1.8
Power(W)	2.6694E-04	2.4137 E-04	1.8155E-04	1.9712 E-04	1.0279E-04

VIII CONCLUSION:

We have implemented low power fully programmable multi-band flexible divider which uses 2/3 prescaler, multimodulous 32 /33/47/48 prescaler using the 0.18µm CMOS technology. Since the multimodulus32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively. A lower-power single-phase clock multiband flexible divider with sleep transistor, the circuit simply leads to reduced static power consumption, reduced number of gates required and hence a reduced area requirement,When compared to previous power consumption 57% has been reduced and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

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