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An Area Efficient Multiplier Design Using Fixed-Width Replica Redundancy

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Abstract:

In this paper, proposedAn Area Efficient Multiplier Design Using Fixed-Width Replica Redundancy by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analysing of probability and statistics. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. In a 16 × 16 bit ANT multiplier, circuit area in our fixed-width RPR can be lower and power consumption in our ANT design can be saved as compared with the state-of-art ANT design.

Key words:

Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR),voltageoverscaling(VOS),error tolerant adder(ETA),main digital signal processing(MDSP).

I.INTRODUCTION:

Rapid growth of portable and wireless computing systems in recent years drives the need for ultralow powersystems. To lower the power dissipation, supplyvoltage scaling [1] is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage. However, in deep-submicrometerprocess technologies, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, the design techniques to enhance noise tolerance have been widely developed [2]-[8]. An aggressive low-power technique, referred to as voltage over scaling (VOS), was proposed in lower supply voltage beyond critical supply voltage without sacrificing the throughput. However, VOS leads to severe degradationin signal-to-noise ratio (SNR).

A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced-precision replica (RPR), which combats softerrors effectively while achieving significant energy saving. Some ANT deformation designs are presented in [5]-[9]the ANT design concept is further extended to system level. However, the RPR designs in the ANT are in a customized manner, which are not easily adopted and repeated.

The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design is still the most popular design because of its simplicity. However, adopting with RPR should still pay extra area overhead and power consumption. In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block. Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead.

We take use of probability, statistics, and partial product weight analysis to find the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

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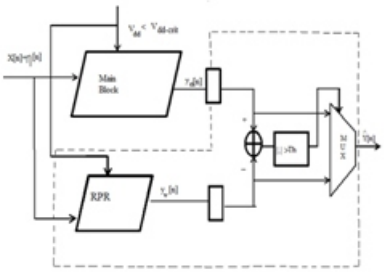

Fig1: ANT architecture

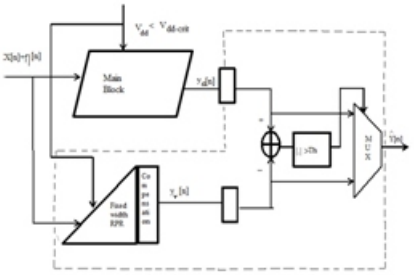

Fig2: Proposed ANT Architecture with fixed width RPR.

II. PROPOSED ANT MULTIPLIER DESIGN USING FIXED-WIDTH RPR:

In this paper, we further proposed the fixed-width RPR toreplace the full-width RPR block in the ANT design [2],as shown in Fig.2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lowerpower consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design in an ANT multiplier. The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needsto be compensated precisely. Many literatures have been presented to reduce the truncation error with constant correction value with variable correction value.

The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise, their compensation method is to compensate the truncation error between the full-length multiplier andthe fixed-width multiplier. However, in the fixed-width RPR of an ANT multiplier, the compensation error we need to correct is the overall truncation error of MDSP block. Unlike, our compensation method is to compensate the truncation error between the full-length MDSP multiplier and the fixed-width RPR multiplier. In nowadays, there aremany fixed-width multiplier designs applied to the full-width multipliers.

However, there is still no fixed-width RPR design applied to the ANT multiplier designs. To achieve more precise error compensation, we compensate the truncation error with variable correction value. We constructthe error compensation circuit mainly using the partial product terms with the largest weight in the least significantsegment. The error compensation algorithm makes use ofprobability, statistics, and linear regression analysis to findthe approximate compensation value [16]. To save hardwarecomplexity, the compensation vector in the partial productterms with the largest weight in the least significant segmentis directly inject into the fixed-width RPR, which does notneed extra compensation logic gates [17].

To further lower thecompensation error, we also consider the impact of truncatedproducts with the second most significant bits on the errorcompensation. We propose an error compensation circuit usinga simple minor input correction vector to compensation theerror remained. In order not to increase the critical path delay,we locate the compensation circuit in the non-critical path of the fixed-width RPR. As compared with the full-width RPRdesign in [15], the proposed fixed-width RPR multiplier notonly performs with higher SNR but also with lower circuitryarea and lower power consumption.A Proposed Precise Error Compensation Vector forFixed-Width RPR DesignIn the ANT design, the function of RPR is to correct theerrors occurring in the output of MDSP and maintain the SNRof whole system while lowering supply voltage. In the caseof using fixed-width RPR to realize ANT architecture, wenot only lower circuit area and power consumption, butalso accelerate the computation speed as compared with theconventional full-length RPR. However, we need to compensatehuge truncation error due to cutting off many hardwareelements in the LSB part of MDSP.In the MDSP of n-bit ANT Baugh–Wooley array

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multiplier,its two unsigned n-bit inputs of X and Y can be expressed ashe (n/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are mostsignificant part (MSP), input correction vector [ICV(ß)].

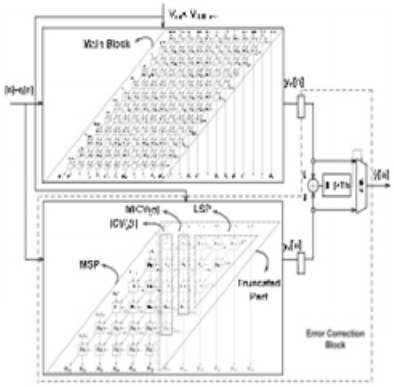
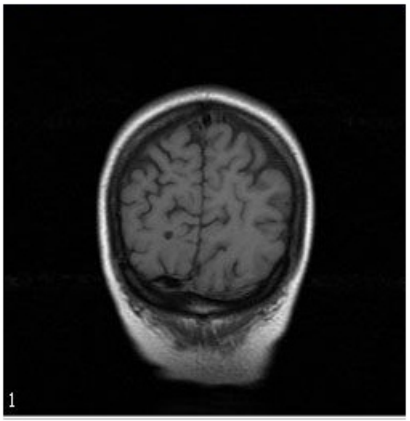


Fig3: 16 × 16 bit ANT multiplier is implemented with the 8-bit fixed width Replica redundancy block.

III. APPLICATION OF ERROR TOLERANT ADDER IN DIGITAL SIGNAL PROCESSING:

In image processing and many other DSP applications, fast Fourier transformation (FFT) is a very important function. The computational process of FFT involves a large number of additions and multiplications. It is therefore a good platform for embedding our proposed ETA. To prove the feasibility of the ETA, we replaced all the common additions involved in a normal FFT algorithm with our proposed addition arithmetic. As we all know, a digital image is represented by a matrix in a DSP system, and each element of the matrix represents the color of one pixel of the image. To compare the quality of images processed by both the conventional FFT and the inaccurate FFT that had incorporated ourproposed ETA, we devised the following experiment. An image was

(a)



(b)

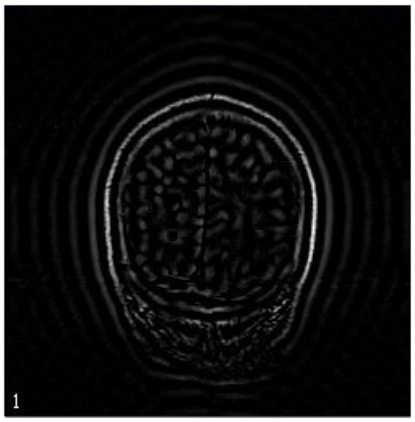


Fig4: Images after FFT and inverse FFT. (a) Image processed with conventionalmultiplier and (b) image processed with the proposed multiplier.

first translated to a matrix form and sent through a standard system that made used of normal FFT and normal reverse FFT. The matrix output of this system was then transformed back to an image and presented in Fig. The matrix of the same image was also processed in a system that used the inaccurate FFT and inaccurate reverse FFT, where both FFTs had incorporated the 16-bit multiplier described in Section, with the processed image given in Fig. 4(b). Although the two resultant matrices of the same image were different, the two pictures obtained (see Fig.4) look almost the same. Fig.4 (b) is slightly darker and contains horizontal bands of different shades of grey.

IV.SIMULATION RESULTS:

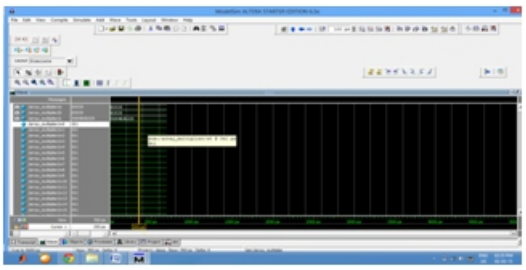


Fig: Array Multiplier Output Result

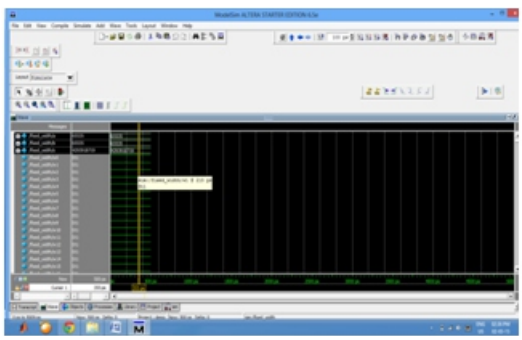


Fig: Fixed Width Multiplier Output Result

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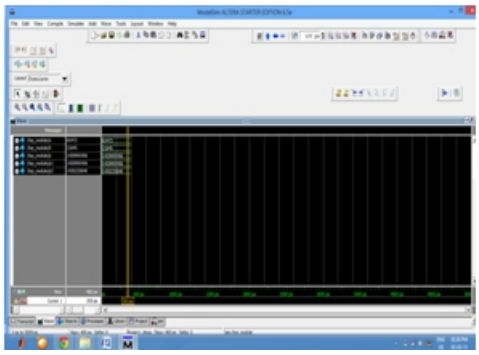

Fig: top module output result

V. SYSTHESIS RESULTS

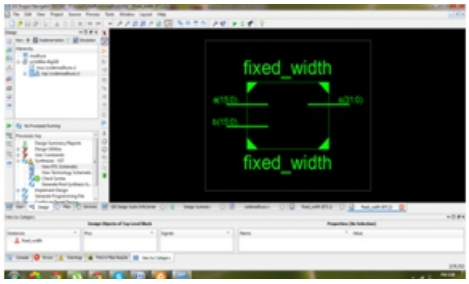

Fig:View RTL Schematic

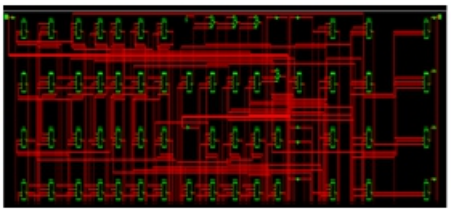

Fig: Technology schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	120	4656	2%
Number of 4 input LUTs	213	9312	2%
Number of bonded IOBs	47	232	20%

Fig:Device Utilization Summary

39.604ns (23.498ns logic, 16.106ns route)
(59.3% logic, 40.7% route)

Delay Calculations

VI. CONCLUSION:

In this paper, the concept of error tolerance is introduced in VLSI design. A novel type of adder, the error-tolerant adder, which trades certain amount of accuracy for significant power saving and performance improvement, is proposed. Extensive comparisons with conventionaldigital adders showed that the proposed multiplier outperformed the conventional adders in both power consumption and speed performance. The potential applications of the multiplier fall mainly in areas where there is no strict requirement on accuracy or where superlow power consumption and high-speed performance are more important than accuracy. One example of such applications is in the DSP application for portable devices such as cell phones and laptops.

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