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Physical Design Implementation of I2C Bus Master Controller

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ABSTRACT:

I2Cisatwo-wire,bi-directionalserialbusthatprovidesa simpleandefficient methodof dataexchange betweendevices.Itismore suitablefor applications requiringcommunicationoverashortdistancebetweenmany lowspeeddevices.

Devicescontrolling the busesiscalledMaster.Masterisresponsibleforgeneration of buscontroland synchronizing signals.SlavesjustfollowtheMaster.Any I2Cdevice canbe eitherreceiver or transmitter.

TheI2Cstandard isa true multi-master bus includingcollisiondetectionandarbitrationthatprovidesdatacollision. Amodule hasbeencreatedwhichactually interfaceswiththeprocess.Thecommunication design and process follow theWishboneprotocol.ThedesignofI2Ccontrollerissocomplexthattheonly way to design and fabricate such complexdesigns is to use computerto automateportions of the designprocess.

Thefocus will beon the numerous aspectsforthe physical design and how those aspectsare automated usingcomputer aided automation(CAD) tools by synopsys. Themainfocus is to studythecontemporarymethods ofIC physicaldesignandtosolvethe differentproblemsof physicaldesignwiththe applicationof synopsystools.

Emphasisisdoneontheconceptsofdesignplanning,placement, clock treesynthesisand routing.The code modulesfor theI2Cbusmaster controllerare developed inVerilog HDL and are synthesized at 90nm technology nodes using Synopsys Design Compiler.

keywords :

SDA,SCL,I2C,Clock Synchronization,Protocol,Arbitration,etc.

INTRODUCTION:

Nowadays the no of devices with multiples applications are increasing in the mother board and the area occupied by embedded memories in System-on-Chip (SoC) is over 90%, and expected to rise up to 94% by 2014 [1]. In such high density embedded systems the communication between different devices with multiples uses must be smooth to ensure proper functioning of the mother board.

In the other hand there are devices which needs to be connected even though they communicate rarely and also connecting low speed devices is a challenge that needs to overcome. Many technologies were developed in recent times to effective check the issue. Also communication between devices also involves collision and arbitration problems which adds to the risk.

With the advancing technology where the no of gates or transistors per chip is doubling every eighteen months we have to update the available features of the devices which provides communication between multiple devices. So Philips semi conductors today known as NXP semiconductors were first to design a multi master, multi slave, single-ended, serial computer bus known as I2C(inter integrated circuit) used for attaining low speed peripherals to computer mother boards and embedded systems.

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Several competitors, such as Siemens AG (later Infineon Technologies AG, now Intel mobile communications), NEC, Texas Instruments, STMicroelectronics (formerly SGS-Thomson), Motorola (later Free scale), and Intersil, have introduced compatible I²C productsto the market since the mid-1990s.SMBus, defined by Intel in 1995, is a subset of I²C that defines the protocols more strictly. One purpose of SMBus is to promote robustness and interoperability.Accordingly, modern I²C systems incorporate policies and rules from SMBus, sometimes supporting both I²C and SMBus, requiring only minimal reconfiguration.

To run in accordance with the advancing technologies and to know what has to be done , knowing the process of physical layout provides an insight into the functioning and physical devices that are used to design I2C or any other device used in the mother board pl. It involves firstly writing the code which suits to the qualities required in a serial bus or in any other design and then synthesizing it to convert into net list. We use this net list to design physical layout of the serial computer bus. We do this with the assistance of CAD (computer aided design) tools.

I2C(inter-integrated circuit):

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices[2].

The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. The interface defines 3 transmission speeds:

- Normal: 100Kbps
- Fast: 400Kbps
- High speed: 3.5Mbps

Only 100Kbps and 400Kbps modes are supported directly. For High speed special IOs are needed. If these IOs are available and used, then High speed is also supported.

OPERATION :

System configuration :

The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors. Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (see START and STOP signals).

I2C Protocols :

Normally, a standard communication consists of four parts:

1) START signal generation
2) Slave address transfer
3) Data transfer
4) STOP signal generation

Fig no 2.2 I2C protocols

START SIGNAL:

When the bus is free/idle, meaning no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal, usually referred to as the S-bit, is defined as a high-to-low transition of SDA while SCL is high.

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The START signal denotes the beginning of a new data transfer. A Repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus The core generates a START signal when the STA-bit in the Command Register is set and the RD or WR bits are set. Depending on the current status of the SCL line, a START or Repeated START is generated[3]

SLAVE ADDRESS TRANSFER :

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a seven-bits calling address followed by a RW bit. The RW bit signals the slave the data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

Note: The core supports 10bit slave addresses by generating two address transfers. See the Philips I2C specifications for more details.The core treats a Slave Address Transfer as any other write action. Store the slave device's address in the Transmit Register and set the WR bit. The core will then transfer the slave address on the bus.

DATA TRANSFER :

Once successful slave addressing has been achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge, the master can generate a STOP signal to abort the data transfer or generate a Repeated START signal and start a new transfer cycle.If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or Repeated START signal. To write data to a slave, store the data to be transmitted in the Transmit Register and set the WR bit. To read data from a slave, set the RD bit. During a transfer the core set the TIP flag, indicating that a Transfer is In Progress.

When the transfer is done the TIP flag is reset, the IF flag set and, when enabled, an interrupt generated. The Receive Register contains valid data after the IF flag has been set. The user may issue a new write or read command when the TIP flag is reset.

STOP SIGNAL:

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the P-bit, is defined as a low-to-high transition of SDA while SCL is at logical '1'.

ARBITRATION PROCEDURE :

CLOCK SYNCHRONIZATION :

The I2C bus is a true multimaster bus that allows more than one master to be connected on it. If two or more masters simultaneously try to control the bus, a clock synchronization procedure determines the bus clock. Because of the wired-AND connection of the I2C signals a high to low transition affects all devices connected to thebus. Therefore a high to low transition on the SCL line causes all concerned devices to count off their low period. Once a device clock has gone low it will hold the SCL line in that state until the clock high state is reached. Due to the wired-AND connection the SCL line will therefore be held low by the device with the longest low period, and held high by the device with the shortest high period.

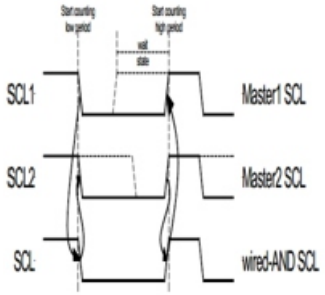

Fig no 2.3 clock synchronization

CLOCK STRETCHING :

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate.

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After the master has driven SCL low, the slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal low period is stretched, thus inserting wait states.

ARCHITECTURE :

The I2C core is built around four primary blocks; the Clock Generator, the Byte Command Controller, the Bit Command Controller and the DataIO Shift Register. All other blocks are used for interfacing or for storing temporary values.

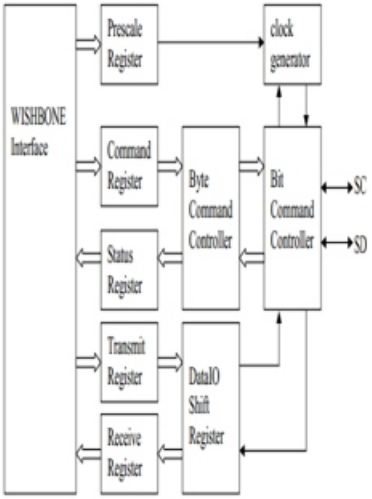

Fig no 2.4 Architecture of I2C

OPTIMIZING THE DESIGN :

Optimization is the Design Compiler synthesis step that maps the design to an optimal combination of specific target library cells, based on the design's functional, speed, and area requirements. You use the compile_ultra command or the compilecommand to compile a design. Design Compiler provides options that enable you to customize and control optimization. Several of the many factors affecting the optimization outcome are discussed in this chapter. For detailed information, see the Design Compiler Optimization Reference manual Design Compiler performs the following three levels of optimization:

- Architectural optimization
- Logic-level optimization
- Gate-level optimization

IMPLEMENTATION:

The main three blocks that are present in I2C are byte controller , bit controller and top module

TOP MODULE OF I2C:

The block diagram of top module is as follows

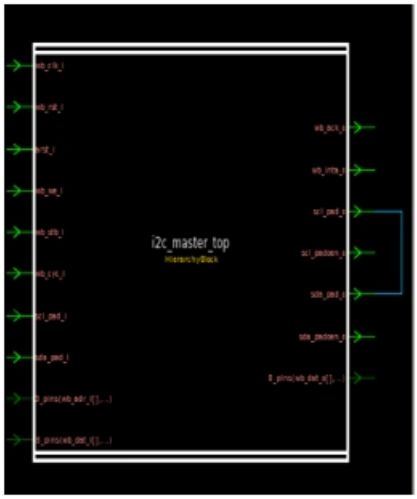

Fig no 5.1 Block diagram of top module

SYNTHESIS:

Synthesis is the process of converting the simulated code into optimized technology dependent net list. We guide the dc_compiler tool to generate and optimize the net list. For this we first have to read the entire code using the command analyze

BIT CONTROLLER BLOCK DIAGRAM

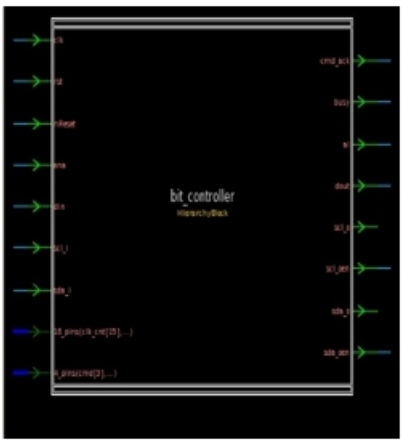

Fig no 5.2 Block diagram of Implemented Bit Controller

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BYTE CONTROLLER BLOCK DIAGRAM:

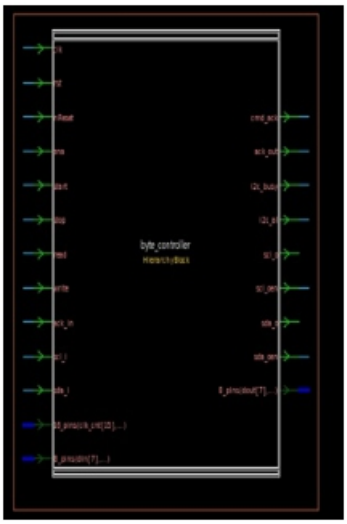

Fig no 5.3 Block diagram of Implemented Byte controller

RESULTS:

SIMULATION :

Simulation of code of top module, byte controller and bit controller gives the following result

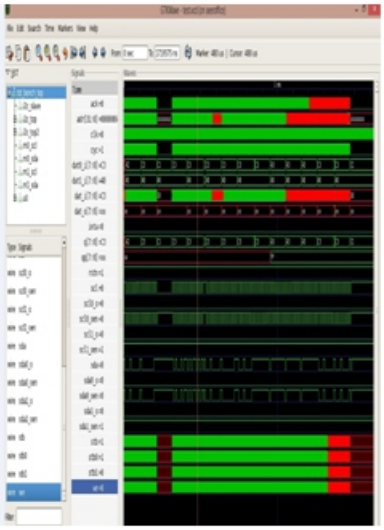

Fig no 6.1 simulation result

The main focus of this experiment revolves around numerous aspects of the physical design and how those aspects are automated using computer aided design(CAD) tools by Synopsys. That is to study the comtemporary methods of IC physical design and to solve the different problems of physical design with the application of synopsys tools. Some of main topics covered in this project are : design planning, placement, clock tree sysnthesis and routing

SYNTHESIS:

Synthesis is a phase in which the RTL code is converted into optimized and technology mapped netlist .[7] Synthesis result for top module is given in the following figure

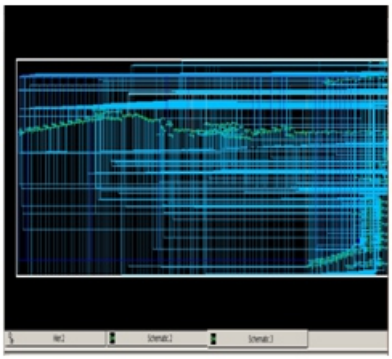

Fig no 6.2 Netlist of top module
Synthesis result for bit controller is given in the following figure

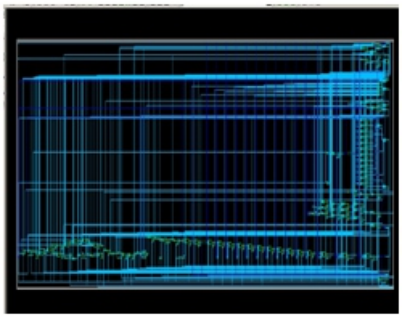

Fig no 6.3 Netlist of bit controller
Similarly synthesis result for byte controller is given in the following figure

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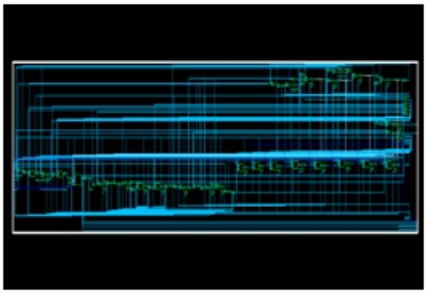

Fig no 6.4 Netlist of byte controller

PHYSICAL DESIGN:

There are four steps in physical design phase they are
Floor plan
Placement
Clock tree synthesis
Routing

FLOORPLAN:

This is the first step in physical design. This is the process of identifying structures that should be closed together and allocating space for them in such a manner as to meet the sometimes conflicting goals of available space, required performance and the desire to have everything close to everything else [8]

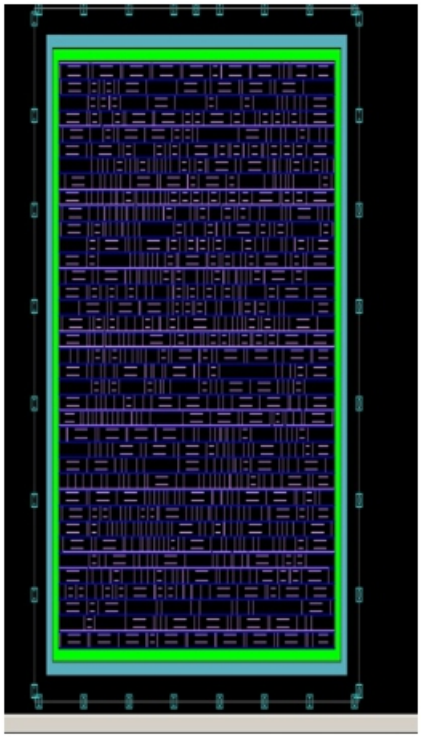

Fig no 6.5 Physical layout of floor plan

PLACEMENT:

It is performed in four optimization process

1.Pre-placement optimization

2.In placement optimization

3.Post placement optimization(PRO) before clock tree synthesis(CTS)

4.PRO and CTS

The placement result of master controller is shown in the below figure

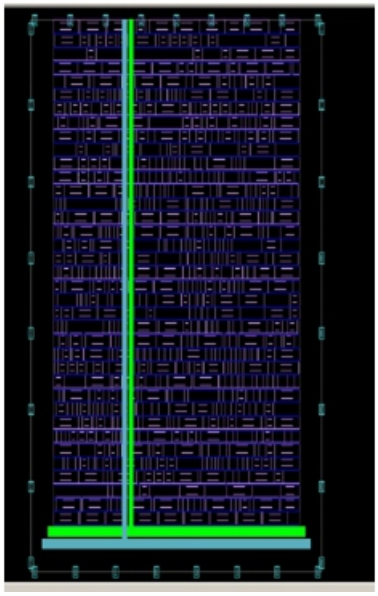

Fig no 6.6 Physical layout of Placement

ROUTING :

There are two types of routing in the physical design process, global routing and local routing. Global routing allocates routing resources that are used for connections. Detailed routing assigns routes to specific metal layers and routing tracts with in the global routing resources Figure below shows the routing of master controller

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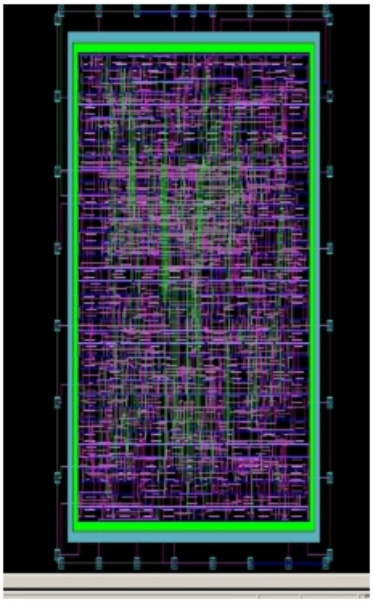

Fig no 6.7 Physical layout of Routing

CONCLUSION:

I2C is a device which is mainly used for communication between devices which are located closely. To design it successfully in the physical layout we have to first write code which satisfies its functionality and check whether the written code is simulated without errors. The output has to be given to synthesis phase which converts it into optimized technology mapped net list. The netlist generated by the synthesis using dc compiler is given along with synopsys design constraints to physical design phase for designing it using computer aided design (CAD) tools. Thus a serial bus master controller physical layout is done using xilix, dc compiler and ic compiler

FUTURE SCOPE :

I2C is the basis for ACCESS bus, the VESA display data channel interface, the system management bus (SMB), POWER MANAGEMENT BUS (PMB), and the INTELLIGENT PLATFORM MANAGEMENT BUS.[9] These variants have differences in voltage and clock frequency ranges and may have interrupt line. So there is a scope for development of many more buses using I2C technology with advanced features in the near future

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