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Design and Implementation of Complex Multiplier Using Compressors

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Abstract:

In this paper, a low-power high speed Complex Multiplier using compressor circuit is proposed for fast digital arithmetic integrated circuits. The compressor has been widely employed for multiplier realizations. Based on a new exclusive OR (XOR) and exclusive NOR (XNOR) module, a 4-2, 5-2, 7-2 compressor circuit has been designed. Proposed circuit shows power consumption variations. Maximum output delay of the circuit presents. Further, power- delay product (PDP) of circuit will change. Power consumption, delay and PDP of proposed complex multiplier circuit have been compared with earlier reported circuits and proposed circuit is proven to have the minimum power consumption and the lowest delay. Simulations have been performed by using DSCH based on Export Micro wind 0.12um CMOS technology.

Keywords:

complex multiplier,4-2,5-2,7-2 compressors, CMOS technology, full adder, power delay product (PDP).

I.INTRODUCTION:

Complex Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing systems, such as computer graphics, scientific calculation, image processing and so on. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. The multiplier architecture consists of a partial product generation stage, partial product reduction stage and the final addition stage.

The partial product reduction stage is responsible for a significant portion of the total multiplication delay, power and area. Therefore in order to accumulate partial products, compressors usually implement this stage because they contribute to the reduction of the partial products and also contribute to reduce the critical path which is important to maintain the circuit's performance. This is accomplished by the use of 4-2, 5-2, 7-2 compressor structures. A 4-2 compressor circuit is also known as full adder cell. As these compressors are used repeatedly in larger systems, so improved design will contribute a lot towards overall system performance. The internal structure of compressors are basically composed of XOR-XNOR gates and multiplexers. The XOR-XNOR circuits are also building blocks in various circuits like arithmetic circuits, multipliers, compressors, parity checkers, etc.

Optimized design of these XOR-XNOR gates can improve the performance of multiplier circuit. In present work, a new XOR-XNOR module has been proposed and 4-2 compressor has been implemented using this module. Use proposed circuit in partial product accumulation reduces transistor count as well as power consumption. This paper is organised as follows: In section II building blocks of complex multiplier circuit are described and compressors a new XOR-XNOR circuit has been proposed. In section III a 4-2 compressor has been designed with new XOR-XNOR module. Sections IV discuss the results. Finally section V concludes the work.

II.COMPRESSOR CIRCUIT BUILDING BLOCKS

There are different architectures and designs of compressor circuits reported in literature. These are mainly composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX).

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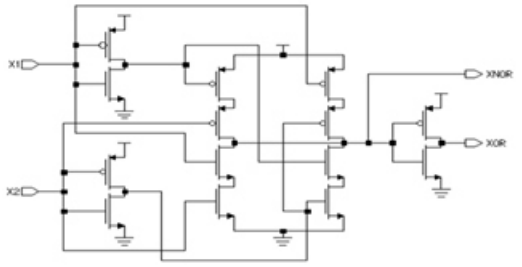
Complementary CMOS uses the dual networks to implement a given function. One part consists of complementary pull-up PMOS network while other part consists of pull-down NMOS networks. This technique requires more numbers of transistors and large layout area. Static CMOS XOR and XNOR gate is shown in figure. Another implementation of XOR-XNOR circuit with 12 transistors is shown in figure. Further in figure two pull-up PMOS-transistors and two pull-down NMOS–transistors are added to restore full swing operation. The circuit performs successfully at low supply voltages but this comes at the expense of increased area and number of transistors. Another disadvantage of the circuit is that each of the inputs drives four gates instead of two gates doubling the input load. This will cause slow response when this circuit is cascaded.



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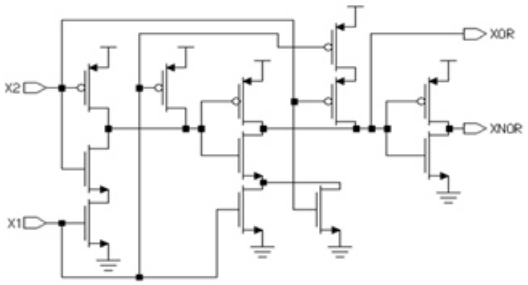

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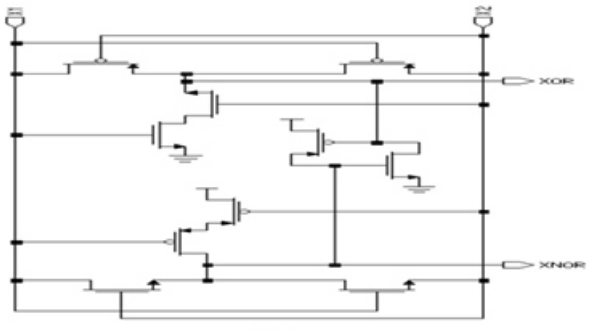
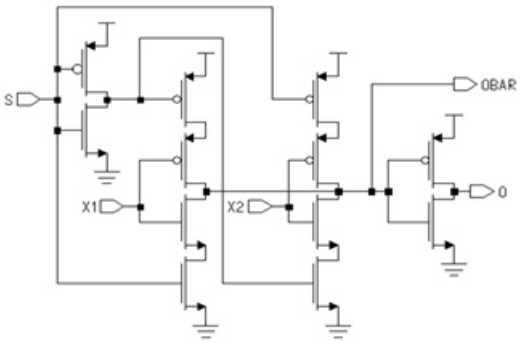


(c)

Fig: Different implementation of XOR-XNOR

Multiplexer module produces an output that accurate reflects state of one of the number of data inputs, based on value of one or more control inputs. Two data inputs multiplexer is named as 2-1 multiplexer. The carry generator module in compressor produces the signals generated by multiplexer. Figure 2(a) shows the multiplexer implemented in standard CMOS logic style. Figure 2(b) by adding an output buffer improves the driving capability but consumes more power. Multiplexer in figure 2(c) is also widely used in low power full adder cells. When buffers are not used at the output, this design of the multiplexer is faster than the CMOS design. This design consumes lesser power than the CMOS design.



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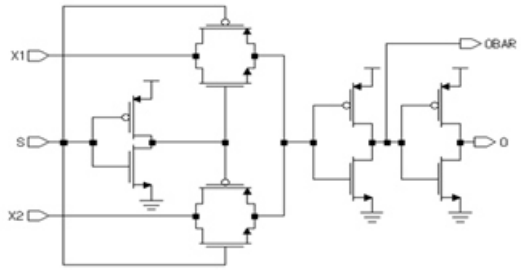

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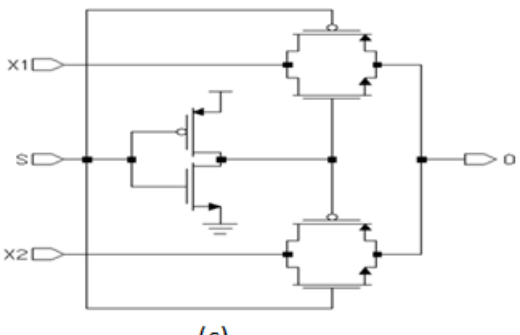

(c)

Fig: Different implementation of multiplexer

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Proposed design of XOR-XNOR circuit using eight transistors has been shown in figure 3(a). This circuit provides good driving capability as it uses static CMOS inverter and can operate at low supply voltages. In this circuit when X1=X2=0 output is low because P1, P2 and N3 transistors are on and logic 0 is passed to output. With input combination of X1=0 and X2=1 circuit show high output as transistor P1, N2 and N3 transistors are on while transistors P2, P3 and N1 are off and high logic is passed to output node. In another case when X1=1 and X2=0, transistor P2, P3 and N1 are on and high logic is passed to output node. In last case when X1=X2=1, output node show low logic as transistor P3, N1 and N2 are on, so proposed circuit works as XOR gate. XNOR operation has been obtained with addition of inverter. Figure 3(b) shows the input and output waveforms for XOR-XNOR circuit.

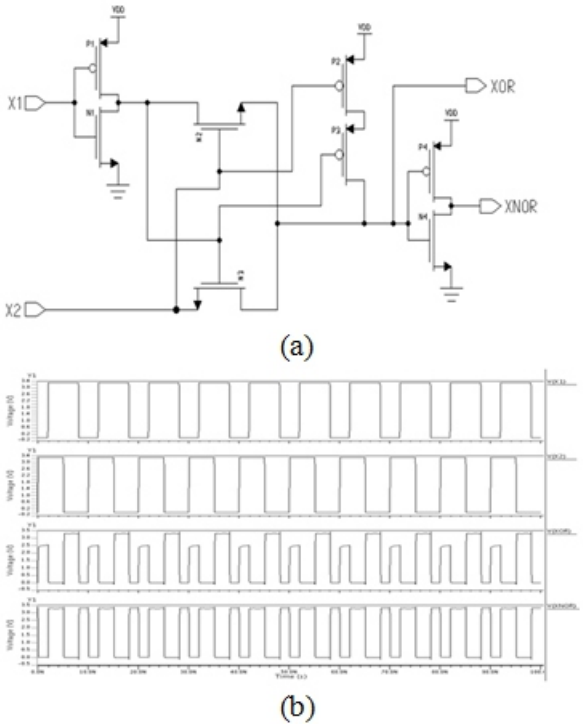

Fig.3: (a) Design of proposed XOR-XNOR (b) Input and output waveform for XOR-XNOR

III. DESIGN OF 4-2 COMPRESSOR :

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder [8].

It has three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two cascaded 3-2 compressor circuits. The conventional implementation of a 4-2 compressor is composed of two serially connected full adders, as shown in figure 4 [9]-[11]. Different structures of 4-2 compressors are reported in literature and these are governing by the basic equation as follows:

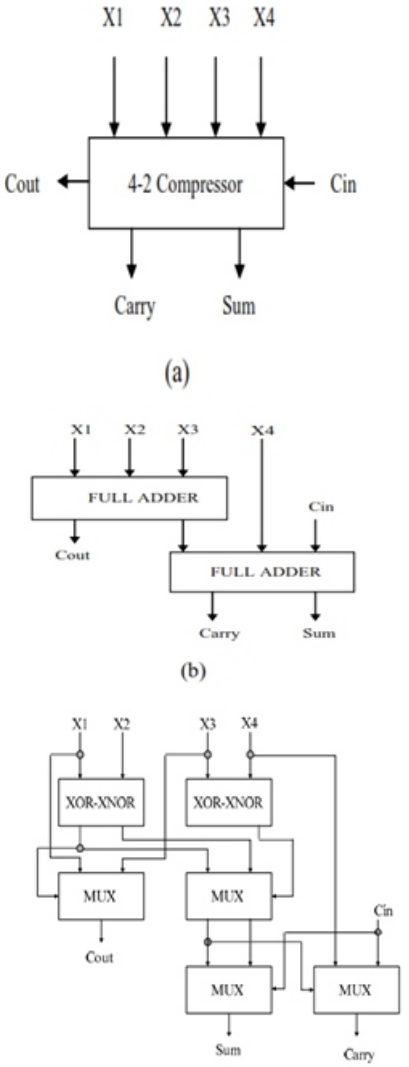

Fig. 4: (a) Block diagram (b) Full adder representation (c) Logic decomposition of 4-2 compressor

The 4-2 compressor has five inputs and three outputs, where the four inputs X1, X2, X3, X4 and the output Sum have the same weight. . On the other hand, the outputs Carry and Cout have one bit order higher, thus presents a higher compression ratio and a more regular interconnection arrangement.

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One vital point to be emphasized in this compressor is the independence of the input carry Cin in the output carry Cout. The 4-2 compressor optimized at gate level with XOR-XNOR modules and carry generators by 2:1 multiplexers (MUX) reduces the critical path delay as shown in figure. The multiplexer block at the SUM output takes the select bit prior to the inputs obtain and thus the transistors are already switched by the time they come. This minimizes the delay to a significant level. The complete circuit diagram of proposed 4-2 compressor is shown in figure.

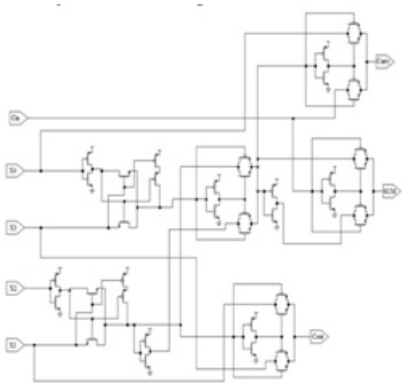

Fig: 4-2 compressor circuit

IV. COMPLUX MULTIPLIER DESIGNS:

In this paper complex Multiplier design is done using compressors and. Multiplication Algorithm The Complex multiplier design and its functionality were discussed in the previous chapters. Now this chapter deals with the simulation and synthesis results of the Complex multiplier. Here Modelsim tool is used in order to simulate the design and checks the functionality of the design.

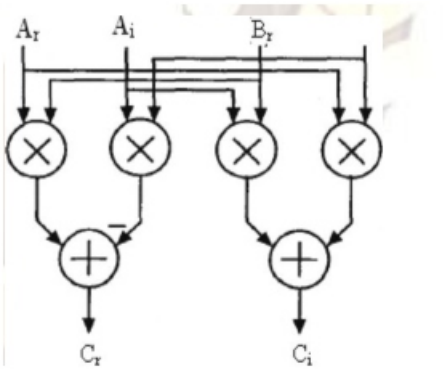

Fig: implementation of complex multiplier

V. Simulations Results:

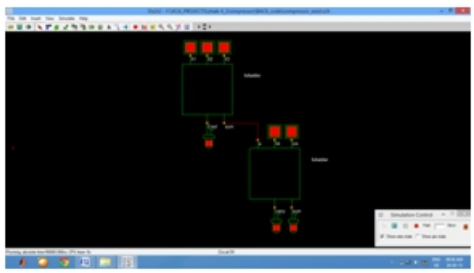

Fig: Existing compressor circuit

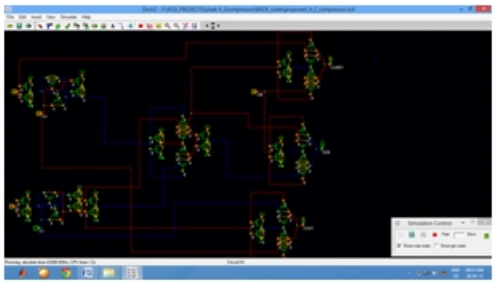

Fig: Proposed compressor circuit

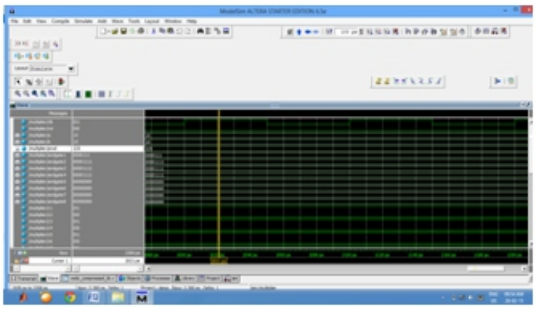

Fig: Simulation results of multiplier

VI. SYNTHESIS RESULT:

The developed Complex multiplier design is simulated and verified their functionality. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE tool. In synthesis process, the RTL model will be converted to the gate level netlist mapped to a specific technology library. This Complex multiplier design can be synthesized on the family of Spartan 3E.Here in this Spartan 3E family, many different devices were available in the Xilinx ISE tool. In order to synthesis this design the device named as "XC3S500E" has been chosen and the package as "FG320" with the device speed such as "-4". The design of Reversible Watermarking Algorithm is synthesized and its results were analyzed as follows.

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VII. CONCLUSION :

In this paper we report on a novel complex number multiplier design based on the compressors, highly suitable for high speed complex arithmetic circuits which are having wide application in VLSI signal processing. The implementation was done in Spice spectre and compared with the mostly used architecture like distributed. The developed Complex Multiplier design is modelled and is simulated using the Modelsim tool. The simulation results are discussed by considering different cases. The RTL model is synthesized using the Xilinx tool in Spartan 3E and their synthesis results were discussed with the help of generated reports.

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