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Fir Filter Design Based on Rounded and Truncated With Multiple Constant Multiplication and Accumulation

Motukatla Prudhvi Raj
M.Tech (Scholar),
Department of ECE,
AVR & SVR College of Engineering & Technology.

Dr.V.Padmanabha Reddy, Ph.D
Professor,
Department of ECE,
AVR & SVR College of Engineering & Technology.

Abstract:
Low-cost and power efficient finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multipliers. Here we consider the optimization of bit width and hardware resources without abdication of the frequency response and output signal precision in the process of accumulation of filter computations. Non uniform coefficient quantization with proper filter order is proposed to minimize total area cost. Multiple constant multiplication/accumulation (MCMA) in a direct FIR structure is implemented using an improved version of truncated multipliers. While Comparisons with prior FIR design like transposed structures which as huge digital novel components in the operation and we enhanced the architectural approaches show that the proposed designs achieve the best area and power results.

Keywords:
Truncation, Accumulation, Faithfully Rounding.

1. Introduction:

Multiplication is one of the most area consuming arithmetic operations in high-performance circuits. The fir filters designs use different types of multipliers to reduce the cost effective parameters. In prior designs we use only truncated multipliers, with those multipliers it will Consume some more area and power, and ineffective results in transposed form. In these form the structural adders and delay elements occupies more area and consumes power also so it was a reasoned to forward the proposed method. Multiplication operations are frequently required in digital signal processing.

To increase speed with which these are done, parallel multipliers can be used. These however require a large area on the chip and consume much power. An important goal would therefore be to reduce the area requirements. Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc.[1] A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest clement in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue[1] In VLSI system design the Current architectures range from small, low-performance shift and add multipliers, to large, high-performance array and tree multipliers. In these different chip designs or system designs of real time analysis the Conventional linear array multipliers achieve high performance in a regular structure, but require large amounts of silicon.

2. Operation of Truncated multiplier:

Truncated multiplication is a technique where only the most significant columns of the multiplication matrix are used and therefore area requirements can be reduced. In Truncation is a method where the least significant columns in the partial product matrix are not formed. The amount of columns not formed in this way, T, defines the degree of truncation and the T least significant bits of the product always result in '0'. The algorithm behind truncated multiplication is the same as when dealing with non truncated multiplication regardless of the truncation degree. The effect is illustrated in Figure, where a truncation degree of T = 3, is applied.With this approach we enhance the

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multiplication extensions of various numbers of bits.[1] Notice that the columns to the right of the maroon vertical line are missing.

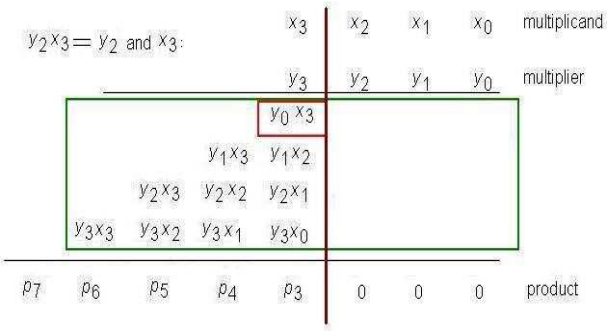

Fig.1. 4x4Binary Multiplication with truncation degree T=3

3. STEPS INCLUDED IN PPB:

In the truncated multiplier the removal of Partial Product Bits (PPB) is composed of three processes:

1. Deletion
2. Truncation
3. Rounding

3.1DELETION:

In truncated multiplier we start the multiplication process with deletion only. In the partial product bits we remove the more than half of the bits, and then remaining bits become the partial products in the process. This is the main criteria of deletion. The PPBs are directly eliminated at the first level without any weight of that bits positions in the process of multiplication.

3.2TRUNCATION:

Truncation is a method where the least significant columns in the partial product matrix are not formed. The amount of columns not formed in this way, T, defines the degree of truncation and the T Least Significant Bits (LSB) of the product always results in 0. The algorithm behind fixed width multiplication is the same as when dealing with non fixed width multiplication regardless of the truncation degree. [3]

3.3ROUNDING:

Conventionally an n-bit multiplicand and an n-bit multiplier would render a 2n-bit product. Sometimes an n-bit output is desired to reduce the number of stored bits.[1] The proposed truncated multiplier consists of several operations such as deletion, reduction, truncation, rounding, and final addition. The first step of deletion operation is performed which removes all the unnecessary PP bits. Those bits are those which are need not to be generated.[3] In the faithfully rounded FIR filter implementation, it is required that the total error introduced during the arithmetic operations is no larger than one ulp. The next step is deletion, where as many possible PP bits are deleted till the deletion error of ED' is bounded by $-1/2$ ulp $\leq$ ED' $\leq$ 0.The correction bias constant injection [4] of a of 1/4 ulp leads the deletion error as $-1/4$ ulp $\leq$ ED'$\leq 1/4$ ulp. Per-column reduction is performed after the deletion of PP bits and two rows of PP bits is generated.[3] So that more PPBs can be deleted, leading to smaller area cost. Compare the two approaches. In [3], the removal of unnecessary PPBs is com- posed of three processes: deletion, truncation, and rounding. Two rows of PPBs are set undeletable because they will be removed at the subsequent truncation and rounding. The error ranges of deletion, truncation, and rounding before and after adding the offset constants.

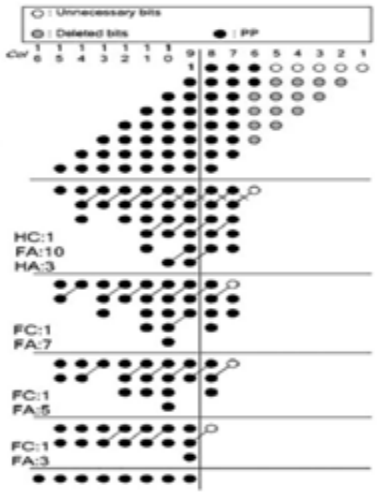

Fig.2.Method of truncated multiplier

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In the process of truncation multiplication after the multiplication process we add the partial product bits, for this process of addition [3] we use the carry save adder for the multiple bits simple addition which can increase the performance.

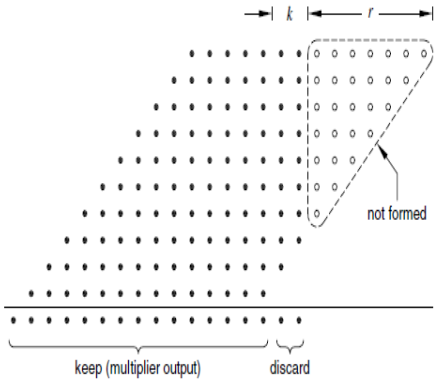

Fig.3. Final truncation output presentation

Truncation error is the difference between a truncated value and the actual value. A truncated quantity is represented by a numeral with a fixed number of allowed digits, with any excess digits "chopped off" (hence the expression "truncated").[3]

4. Introduction of FIR filters:

Finite Impulse Response (FIR) filters are one of two primary types of filters used in DSP, the other type being Infinite Impulse Response Filters (IIR) filters.[1] The impulse response of an FIR filter is “finite" because there is no feedback in the filter. Compared to IIR filters, FIR filters offer various advantages. Linear phase refers to the fact that the phase response of the filter is a straight-line function of frequency.

This means that the delay through the filter will be the same at all frequencies. This is the major advantage of FIR filters. They can easily be designed to be "Linear Phase”. Linear-Phase filters delay the input signal, but don’t distort its phase. They are simple to implement. On most DSP microprocessors, looping a single instruction can do the FIR calculation.

5. Various Types of FIR filters:

There are two basic FIR structures, direct form and transpose form, for a linear-phase even-order FIR filter.

5.1 STRUCTURE OF TRANSPOSED FORM:

In the transposed form the operands of the multipliers in the MCM module are the current input signal x[n] and coefficients.[2]

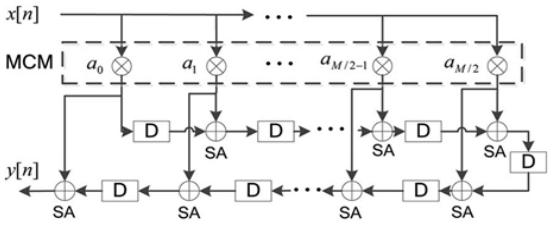

Fig.4. Transposed form of FIR structure

The results of individual constant multiplications go through structure adders (SAs) and delay elements. When we do the analyzation[5] of forms of FIR structures, first the transposed form possess the memory results as low as possible with the truncated multipliers. But in the transposed form the power analyzation results are not giving effective results to decrease the cost of FIR filters Due to the components usage is more in the transposed form and the internal architecture is also highly complexity possess in the wiring of those components so automatically the power factor is increasing.

5.2 STRUCTURE OF DIRECTFORM:

In the direct form in the multiple constant multiplication (MCM)/accumulation (MCMA) module performs the concurrent multiplications of individual delayed signals and respective filter coefficients, followed by accumulation of all the products. Thus, the operands of the multipliers in MCMA are delayed input signals x [n − i] and coefficients ai.

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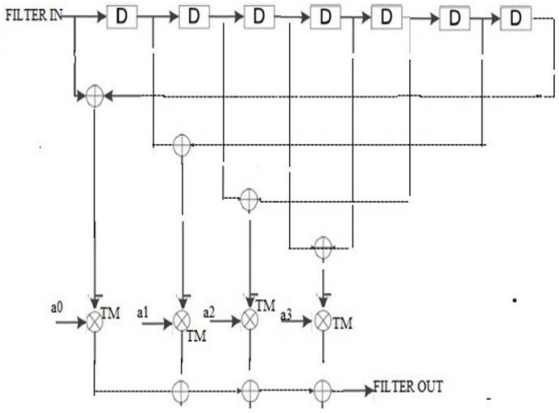

Fig.5. Direct form of FIR structure

In the anlyzation of parameters in the direct form we got the effective results in terms of power and delay based results. The area also in the satisifactable range in the direct form. This direct form possess the low-cost FIR filter designs by jointly considering the optimization of coefficient bit width and hardware resources in and the implementations done with the low power values. When compare with the prior designs like transposed form, we observe that the direct FIR structure with faithfully rounded MCMAT [5] leads the smallest area cost and power consumption.

6. ANALYSIS OF PROS & CONS

6.1 PROS:

- Memory occupation in the truncated multiplier is low compare to other multipliers.
- Delay will be changes with respect to the number of bits taken in the multiplier (4-bit, 8-bit, 12-bits) that is low.
- Speed also high i.e. if the delay is low then speed will be increase; those are inversely proposal to each other.
- Power consumption in the truncated multiplier is low compare to other multiplier (dadda, Wallace, array multiplier).

6.2 CONS:

- The main disadvantage of the truncated multiplier is it gives rounded value but not exact value.
- We got nearest value in this truncated multiplier as increase the complexity in number of bit widths and the operational phenomena.
- In terms of FIR filters also the final output after the process of accumulations multiple truncated multipliers and arithmetic adders we got the appropriate value.

7. Analysis of Results

7.1. Synthesis results

7.1.1. RTL schematics

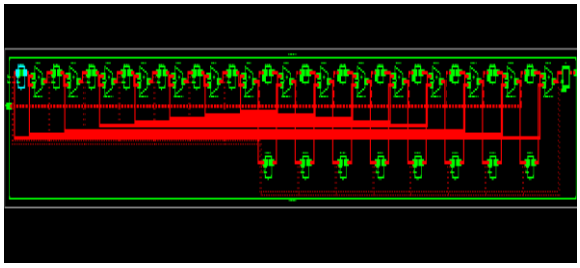

Fig.6. RTL schematic of direct form

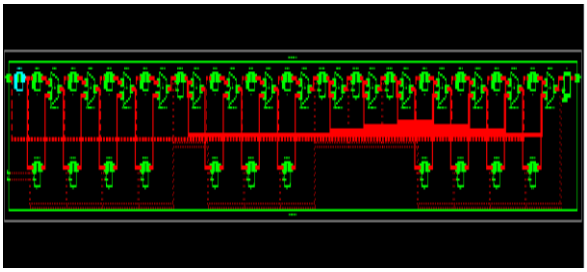

Fig.7. RTL schematic of transposed form

7.2 Device power report

Selected Device: SPARTAN 3E 3s500efg320-4

By the analysis of XILINX analyze power distribution we evaluate the final device power (in mw) report.

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	7	9312	0
Signals	0.000	15	---	---
IOs	0.000	14	232	6
Leakage	0.076			
Total	0.076			

TAB.1. Device power report

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TRANSPOSED FORM FIR FILTER (EXISTING)	12 BIT	8 BIT	4 BIT
LUT's (Look Up Tables)	638	192	42
POWER (in mw)	5.2	1.5	0.3
DELAY (in ns)	4.283 ns	4.283 ns	4.283 ns

TAB.2. Synthesis analysis of FIR forms

DIRECT FORM FIR FILTER (PROPOSED)	12 BIT	8 BIT	4 BIT
LUT's (Look Up Tables)	278	125	63
POWER (in mw)	2.2	1	0.5
DELAY (in ns)	4.283 ns	4.283ns	4.283 ns

TAB.3. Synthesis analysis of FIR forms

7.3 Simulation results

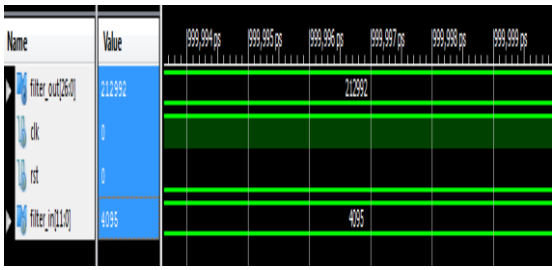

Fig.8. Final output of 12-bit direct form

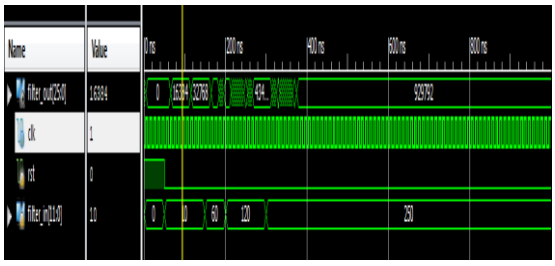

Fig.9. Final output of 12-bit transposed form

8. Conclusion:

In the comparison of parameters in different forms of FIR structures has presented low-cost FIR filter designs by jointly considering the direct form in the optimization of coefficient bit width and hardware resources in implementations with FIR filters.In the most prior designs are based on the transposed form but the power related parameters are not satisfied. So we implemented the direct FIR structure with faithfully rounded MCMAT leads to the smallest area cost and low power parameters.

8.1 FUTURE SCOPE:

In every application of chip system designs the significance and operations of multiplier's and adder's accumulation part is necessary so we forward with these truncation process with the power efficient devices with the appropriate results.

9. REFERENCES:

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