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A New General Topology for Cascaded Multilevel Inverters Based on Developed H Bridge

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ABSTRACT:
A new general cascaded multilevel inverter using developed H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. A new algorithm to determine the magnitude of dc voltage sources is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation and experimental results.

INTRODUCTION:
Multilevel inverters have received more attention for their ability on high-power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference. These inverters generate a stepped voltage waveform by using a number of dc voltage sources as the input and an appropriate arrangement of the power-semiconductor-based devices. Three main structures of the multilevel inverters have been presented: “diode clamped multilevel inverter,” “flying capacitor multilevel inverter,” and “cascaded multilevel inverter”. The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources.

In the symmetric types, the magnitudes of the dc voltage sources of all H-bridges are equal while in the asymmetric types, the values of the dc voltage sources of all H-bridges are different. The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage.

EXCISTING SYSTEM:
Several algorithms for determining the magnitudes of dc voltage sources for the conventional cascaded multilevel inverter have been presented. The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage. In this paper, in order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed. It is important to note that in the proposed topology, the unidirectional power switches are used. Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of IGBTs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch.

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PROPOSED TOPOLOGY:

In below figure, two new topologies are proposed for a seven-level inverter. As shown in Fig. 1, the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches (*Sa*, *Sb*, *SL*,1, *SL*,2, *SR*,1, and *SR*,2) and two dc voltage sources (*VL*,1 and *VR*,1). In this paper, these topologies are called developed H-bridge. As shown in Fig. 1, the simultaneous turn-on of *SL*,1 and *SL*,2 (or *SR*,1 and *SR*,2) causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided.

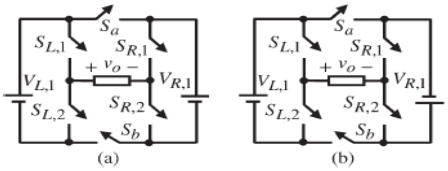

Fig. 1. Proposed seven-level inverters. (a) First proposed topology. (b) Second proposed topology.

TABLE I
OUTPUT VOLTAGES OF THE PROPOSED SEVEN-LEVEL INVERTERS

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o (Fig. 1(a))	v_o (Fig. 1(b))
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}-V_{R,1}$	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}-V_{R,1})$	$-(V_{L,1}+V_{R,1})$

In addition, *Sa*and *Sb*should not turn on, simultaneously. The difference in the topologies illustrated in Fig. 1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON- and OFF-states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three.

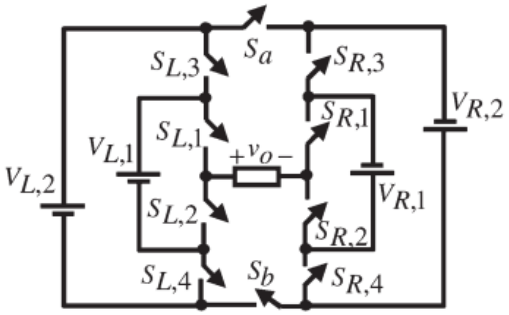

Fig. 2.Proposed 31-level inverter.

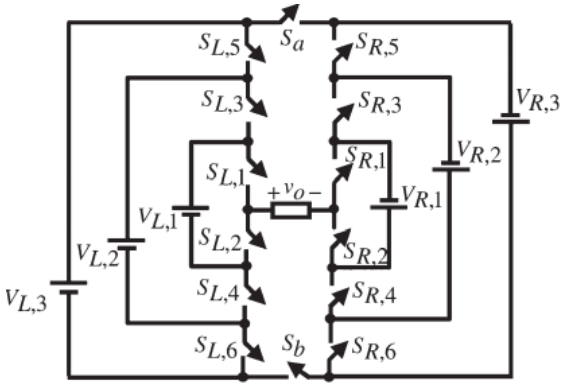

Fig. 3.Proposed 127-level inverter.

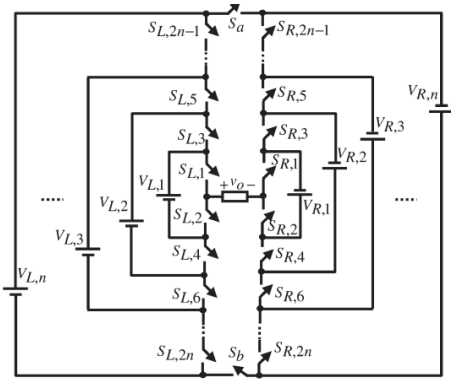

Fig. 4.Proposed general topology.

In the proposed general topology, the number of output voltage levels (Nstep), number of switches (Nswitch), number of dc voltage sources (Nsource), and the maximum magnitude of the generated voltage

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(Vo,max) are calculated as follows, respectively:

$$N_{\text{step}} = 2^{2n+1} - 1 \quad (1)$$
$$N_{\text{switch}} = 4n + 2 \quad (2)$$
$$N_{\text{source}} = 2n \quad (3)$$
$$V_{o,\max} = V_{L,n} + V_{R,n}. \quad (4)$$

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [20]. The number of variety of the values of dc voltage sources (Nvariety) is given by

Nvariety = 2n. (5)

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig. 1(b), the blocking voltage of SR,1 and SR,2 are calculated as follows:

$$V_{\text{SR},1} = V_{\text{SR},2} = V_{R,1} \quad (6)$$

where VSR,1 and VSR,2 indicate the maximum blocking voltages of SR,1 and SR,2, respectively. The blocking voltage of SL,1 and SL,2 are as follows:

$$V_{\text{SL},1} = V_{\text{SL},2} = V_{L,1} \quad (7)$$

where VSL,1 and VSL,2 indicate the maximum blocking voltages of SL,1 and SL,2, respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (Vblock,1) is calculated as follows:

$$V_{\text{block},1} = V_{\text{SR},1} + V_{\text{SR},2} + V_{\text{SL},1} + V_{\text{SL},2} + V_{\text{Sa}} + V_{\text{Sa}} = 4(V_{R,1} + V_{L,1}). \quad (8)$$

Considering Fig. 2, the maximum blocking voltage of the switches is as follows:

$$V_{\text{SR},1} = V_{\text{SR},2} = V_{R,1} \quad (9)$$
$$V_{\text{SR},3} = V_{\text{SR},4} = V_{R,2} - V_{R,1} \quad (10)$$
$$V_{\text{SL},1} = V_{\text{SL},2} = V_{L,1} \quad (11)$$
$$V_{\text{SL},3} = V_{\text{SL},4} = V_{L,2} - V_{L,1} \quad (12)$$
$$V_{\text{Sa}} = V_{\text{Sb}} = V_{R,2} + V_{L,2}. \quad (13)$$

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter (Vblock,2) is as follows:

$$V_{\text{block},2} = V_{\text{SR},1} + V_{\text{SR},2} + V_{\text{SR},3} + V_{\text{SR},4} + V_{\text{SL},1} + V_{\text{SL},2} + V_{\text{SL},3} + V_{\text{SL},4} + V_{\text{Sa}} + V_{\text{Sb}} = 4(V_{R,2} + V_{L,2}). \quad (14)$$

PROPOSED ALGORITHM:

The following algorithm is applied to determine the magnitude of dc voltage sources. It is important to note that all voltage levels (even and odd) can be generated.

A. Proposed Seven-Level Inverter:

The magnitudes of the dc voltage sources of the seven-level inverter shown in Fig. 1(b) are determined as follows:

$$V_{L,1} = V_{\text{dc}} \quad (17)$$
$$V_{R,1} = 2V_{\text{dc}}. \quad (18)$$

Considering (17), (18), and Table I, the proposed seven-level inverter can generate 0, ±Vdc, ±2Vdc, and ±3Vdc at output.

B. Proposed 31-Level Inverter:

The magnitudes of the dc voltage sources of the proposed 31-level inverter are recommended as follows:

$$V_{L,1} = V_{\text{dc}} \quad (19)$$
$$V_{R,1} = 2V_{\text{dc}} \quad (20)$$
$$V_{L,2} = 5V_{\text{dc}} \quad (21)$$
$$V_{R,2} = 10V_{\text{dc}}. \quad (22)$$

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The proposed inverter can generate all negative and positive voltage levels from 0 to 15Vdc with steps of Vdc.

C. Proposed 127-Level Inverter:

The magnitudes of the dc voltage sources of the proposed 127-level inverter are calculated as follows:

$$V_{L,1} = V_{\mathrm{dc}} \quad (23)$$

$$V_{R,1} = 2V_{\mathrm{dc}} \quad (24)$$

$$V_{L,2} = 5V_{\mathrm{dc}} \quad (25)$$

$$V_{R,2} = 10V_{\mathrm{dc}} \quad (26)$$

$$V_{L,3} = 25V_{\mathrm{dc}} \quad (27)$$

$$V_{R,3} = 50V_{\mathrm{dc}}. \quad (28)$$

By using this algorithm, the inverter can generate all negative and positive voltage levels from 0 to 63Vdc with steps of Vdc.

D. Proposed General Multilevel Inverter:

The magnitudes of the dc voltage sources of the proposed general multilevel inverter can be obtained as follows:

$$V_{L,j} = 5^{j-1}\, V_{\mathrm{dc}} \quad \text{for} \quad j = 1, 2, 3, \ldots, n \quad (29)$$

$$V_{R,j} = 2 \times 5^{j-1}\, V_{\mathrm{dc}} \quad \text{for} \quad j = 1, 2, 3, \ldots, n. \quad (30)$$

Considering (4) and (16), the values of Vo,max and Vblock,n of the proposed general multilevel inverter are as follows,

$$V_{o,\max} = V_{L,n} + V_{R,n} = 3 \times 5^{n-1} V_{dc} \quad (31)$$

$$V_{\mathrm{block},n} = 4(V_{L,n} + V_{R,n}) = 12(5^{n-1})V_{\mathrm{dc}}. \quad (32)$$

COMPARING THE PROPOSED GENERAL TOPOLOGY WITH THE EXCITING TOPOLOGIES:

To clarify the advantages and disadvantage of the proposed topology, it should be compared with the different kinds of topologies presented in literature. The conventional cascaded multilevel inverter with two different algorithms has been presented. These algorithms are known as the symmetric cascaded multilevel inverters and the asymmetric ones with the binary method for determining the magnitude of dc voltage sources. The conventional symmetric cascaded multilevel inverter is indicated by R1 and the conventional binary asymmetric cascaded multilevel inverter is shown by R2. Four different structures for the cascaded multilevel inverter have been presented, and in this paper, they are indicated by R6–R7 and R11–R12. It is important to note that the power switches in the aforementioned topologies are unidirectional.

TABLE II:OUTPUT VOLTAGES OF THE PROPOSED 31-LEVEL INVERTER

No.	$S_{L,1}$	$S_{L,2}$	$S_{L,3}$	$S_{L,4}$	$S_{R,1}$	$S_{R,2}$	$S_{R,3}$	$S_{R,4}$	S_a	S_b	v_o
1	1	0	1	0	1	0	1	0	0	1	$V_{L,2}+V_{R,2}$
2	1	0	1	0	0	1	1	0	0	1	$V_{L,2}+V_{R,2}-V_{L,1}$
3	0	1	1	0	1	0	1	0	0	1	$V_{R,2}+V_{L,2}-V_{R,1}$
4	0	1	1	0	0	1	1	0	0	1	$V_{L,2}+V_{R,2}-V_{L,1}-V_{R,1}$
5	1	0	1	0	1	0	0	1	0	1	$V_{L,1}+V_{R,2}$
6	1	0	1	0	0	1	0	1	0	1	$V_{R,2}$
7	0	1	1	0	1	0	0	1	0	1	$V_{L,1}-V_{R,1}+V_{R,2}$
8	0	1	1	0	0	1	0	1	0	1	$V_{R,2}-V_{R,1}$
9	1	0	0	1	1	0	1	0	0	1	$V_{L,2}+V_{R,1}$
10	1	0	0	1	0	1	1	0	0	1	$V_{L,2}+V_{R,1}-V_{L,1}$
11	0	1	0	1	1	0	1	0	0	1	$V_{L,2}$
12	0	1	0	1	0	1	1	0	0	1	$V_{L,2}-V_{L,1}$
13	1	0	0	1	1	0	0	1	0	1	$V_{L,1}+V_{R,1}$
14	1	0	0	1	0	1	0	1	0	1	$V_{R,1}$
15	0	1	0	1	1	0	0	1	0	1	$V_{L,1}$
16	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0 1	0
17	1	0	1	0	0	1	1	0	1	0	$-V_{L,1}$
18	0	1	1	0	1	0	1	0	1	0	$-V_{R,1}$
19	0	1	1	0	0	1	1	0	1	0	$-(V_{L,1}+V_{R,1})$
20	1	0	1	0	1	0	0	1	1	0	$-(V_{L,2}-V_{L,1})$
21	1	0	1	0	0	1	0	1	1	0	$-V_{L,2}$
22	0	1	1	0	1	0	0	1	1	0	$-(V_{L,2}+V_{R,1}-V_{L,1})$
23	0	1	1	0	0	1	0	1	1	0	$-(V_{L,2}+V_{R,1})$
24	1	0	0	1	1	0	1	0	1	0	$-(V_{R,2}-V_{R,1})$
25	1	0	0	1	0	1	1	0	1	0	$-(V_{L,1}-V_{R,1}+V_{R,2})$
26	0	1	0	1	1	0	1	0	1	0	$-V_{R,2}$
27	0	1	0	1	0	1	1	0	1	0	$-(V_{L,1}+V_{R,2})$
28	1	0	0	1	1	0	0	1	1	0	$-(V_{L,2}+V_{R,2}-V_{L,1}-V_{R,1})$
29	1	0	0	1	0	1	0	1	1	0	$-(V_{R,2}+V_{L,2}-V_{R,1})$
30	0	1	0	1	1	0	0	1	1	0	$-(V_{L,2}+V_{R,2}-V_{L,1})$
31	0	1	0	1	0	1	0	1	1	0	$-(V_{L,2}+V_{R,2})$

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SOFTWARE TOOLS:

(Matlab Simulation)

- **Simulink**
- It is a commercial tool for modeling, simulating and analyzing multi domain dynamic systems.
- Its primary interface is a graphical block diagramming tool and a customizable set of block libraries.
- Simulink is widely used in control theory and digital signal processing for multi domain simulation and Model based design.

APPLICATIONS

1.Technical computing

2.Engineering and sciences applications

- Electrical Engineering
- DSP and DIP
- Automation
- Communication purpose
- Aeronautical
- Pharmaceutical
- Financial services.

Other Features

- 2-D and 3-D graphics functions for visualizing data
- Tools for building custom graphical user interfaces
- Functions for integrating MATLAB based algorithms with external applications and languages, such as C,
-

EXPERIMENTAL RESULTS:

SIMULATION DIAGRAMS:

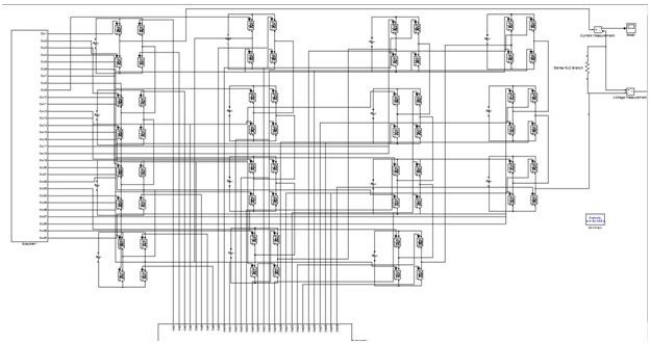

Figure: Cascaded Multilevel Inverters

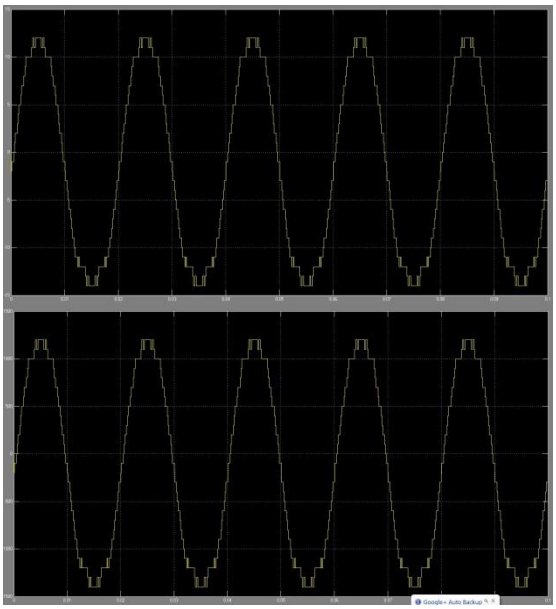

Figure: output waveforms

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