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Improved Version of 128 Bit Binary Adder design using QCA with Area Efficiency and High Speed

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Abstract:

Among the emerging technologies recently proposed as alternatives to the classic CMOS, Quantum-dot cellular automata (QCA) is one of the most promising solutions to design area efficient and very high speed digital circuits. As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. According to recent analysis the minimum limit for transistor size may be reached. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this survey a binary adder is taken for analysis and a new adder is designed based upon QCA technology. The aim of this proposed technique is that to reducing number of majority gates used in the design. This will lead to reduce number of QCA cells so that total area of binary adder circuit can be minimized compare to previous designs. The proposed 128 Bit QCA adder is implemented on Xilinx ISE and designed using Verilog HDL.

Index Terms:

Adders, nano computing, quantum-dot cellular automata (QCA).

I. INTRODUCTION:

Binary adders are one of the most essential logic elements within a digital system. In addition, binary adders are also helpful in units other than Arithmetic Logic Units (ALU),such as multipliers, dividers and Memory addressing. Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra-dense low-power high-performance digital circuits [1]. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits [2]–[16], with the main interest focused on the binary addition [11]–[16] that is the basic operation of any digital system. Of course, the architectures commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry (RCA), carry look-ahead (CLA), and conditional sum adders were presented in [11]. The carry-flow adder (CFA) shown in [12] was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA in [13] and [14]. Recently, more efficient designs were proposed in [15] for the CLA and the BKA, and in [16] for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA. Theoretical formulations demonstrated in [15] for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.

An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-ofthe-art competitors and achieves the lowest area-delay product (ADP). The rest of this brief is organized as follows: a brief background of the QCA technology and existing adders designed in QCA is given in Section II, the novel adder design is then introduced in Section III, simulation and comparison results are presented in Section IV, and finally, in Section V conclusions are drawn.

II. BACKGROUND:

Quantum-dot cellular automata(QCA) is based on field coupled computing. States of a cell change due to mutual interactions of either electrostatic or magnetic fields. QCA Cell is the fundamental component of QCA Logic. Each QCA cell is made of four quantum dots in which two mobile electrons can be trapped which can tunnel between the dots. Due to the repulsion between the electrons, two electrons always take up the diagonal positions. Binary levels are represented by the positions of the electrons inside the cell unlike the voltage or current levels as in the CMOS.

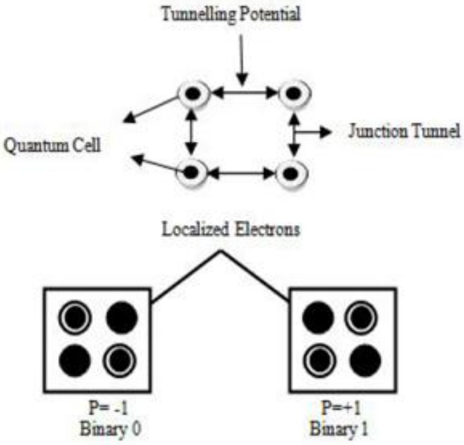

Fig 1: QCA Cell

Fig.1 show the structures of quantum cell with two different polarizations (electrons are shown with black filled circular dots). Majority gate and Inverter are the two basic logic devices of QCA.

Fig.2 shows the structure of the majority gate with 3 inputs, driver cell and output cell. Computation starts by driving the driver cell to the lowest energy state. Input cell changes its state by the signal which arrives towards the driver cell.Driver cell always gets the binary value of majority of input signals since it is where the repulsion for the mobile electrons in driver cell is at minimum and output follows the state of driver cell.

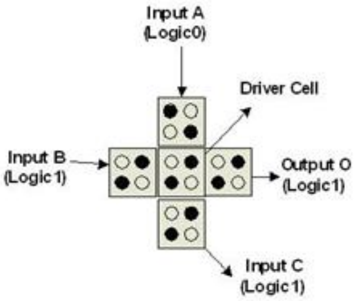

Fig.2 Majority Gate

The logic function for the majority gate is given by M(a,b,c) = ab+bc+ca (1) Where a, b, c as boolean variables. In this way two input AND, OR gates can be designed by keeping the third variable as either 0 or 1 respectively.Inverter is the other basic logic device of QCA. If cells are placed diagonally to each other then they will have opposite polarizations. QCA Inverter is designed by this characteristic, such as shown in Fig. 3.

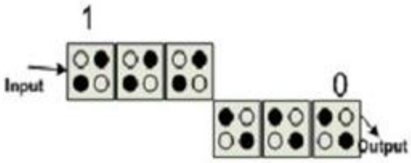

Fig.3. QCA Inverter

III. LITERATURE SURVEY:

Several designs of adders in QCA exist in literature. The RCA [11], [13] and the CFA [12] process n-bit operands by cascading n full-adders (FAs). Even though these addition circuits use different topologies of the generic FA, they have a carry-in to carry-out path consisting of one MG, and a carry-in to sum bit path containing two MGs plus one inverter. As a consequence, the worst case computational paths of the n-bit RCA and the n-bit CFA consist of (n+2) MGs and one inverter. A CLA architecture formed by 4-bit slices was also presented in [11]. In particular, the auxiliary propagate and generate signals, namely pi = ai + bi and gi = ai · bi , are computed for each bit of the operands and then they are grouped four by four. Such a designed n-bit CLA has a computational path composed of 7 + 4 × (log4 n) cascaded MGs and one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which only one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path. In addition, to compute the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that, to process n-bit addends, log4 n levels of CLA logic are required, each contributing to the computational path with four cascaded MGs. Finally, the computation of sum bits introduces two further cascaded MGs and one inverter.

The parallel-prefix BKA demonstrated in [13] exploits more efficient basic CLA logic structures. As its main advantage over the previously described adders, the BKA can achieve lower computational delay. When n-bit operands are processed, its worst case computational path consists of 4 × log2 n − 3 cascaded MGs and one inverter. Apart from the level required to compute propagate and generate signals, the prefix tree consists of 2 × log2n −2 stages. From the logic equations provided in [13], it can be easily verified that the first stage of the tree introduces in the computational path just one MG; the last stage of the tree contributes with only one MG; whereas, the intermediate stages introduce in the critical path two cascaded MGs each. Finally, for the computation of the sum bits, further two cascaded MGs and one inverter are added. With the main objective of trading off area and delay, the hybrid adder (HYBA) described in [14] combines a parallel-prefix adder with the RCA. In the presence of n-bit operands, this architecture has a worst computational path consisting of 2×log2 n +2 cascaded MGs and one inverter. When the methodology recently proposed in [15] was exploited, the worst case path of the CLA is reduced to 4 × log4 n + 2 × log4 n − 1 MGs and one inverter. The above-mentioned approach can be applied also to design the BKA. In this case the overall area is reduced with respect to [13], but maintaining the same computational path. By applying the decomposition method demonstrated in [16], the computational paths of the CLA and the CFA are reduced to 7 + 2 × log2(n/8) MGs and one inverter and to (n/2) + 3 MGs and one inverter, respectively.

IV. NOVEL QCA ADDER:

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two n-bit addends A = a_{n-1},..., a_0 and B = b_{n-1},..., b_0 and suppose that for the ith bit position (with i = n − 1,..., 0) the auxiliary propagate and generate signals, namely p_i = a_i + b_i and g_i = a_i· b_i , are computed. c_i being the carry produced at the generic (i−1)th bit position, the carry signal c_{i+2}, furnished at the (i+1)th bit position, can be computed using the conventional CLA logic reported in (2). The latter can be rewritten as given in (3), by exploiting Theorems 1 and 2 demonstrated in [15]. In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

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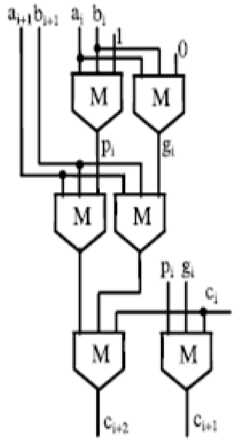


Fig. 4.Novel 2-bit basic module.

Equation (3) is exploited in the design of the novel 2-bit module shown in Fig. 4 that also shows the computation of the carry ci+1 = M(pi gi ci). The proposed n-bit adder is then implemented by cascading n/2 2-bit modules as shown in Fig. 5(a). Having assumed that the carry-in of the adder is c_{in} = 0, the signal p0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in Fig. 5(b).

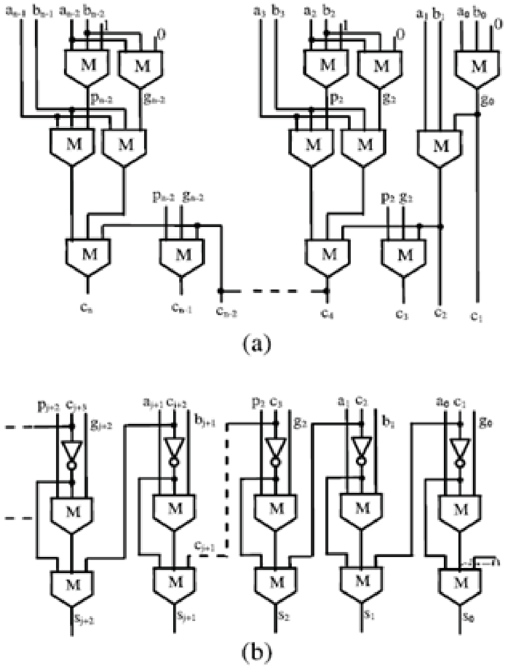


Fig.5 Novel n-bit adder (a) carry chain and (b) sum block.

It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position (i.e., g0 = 1) and then it is propagated through the subsequent bit positions to the most significant one. In this case, the first 2-bit module computes c2, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to (n − 2)/2. Considering that further two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of (n/2) + 3 MGs and one inverter.

ci+2 = gi+1 + pi+1 · gi + pi+1 · pi · ci (2)
ci+2 = M(M ai+1, bi+1, gi M ai+1, bi+1, pi ci). (3)

V.SIMULATION RESULTS:

The synthesis and simulation are performed on Xilinx ISE 14.7.All the synthesis and simulation results are implemented using Verilog HDL. The simulation results are shown below figures.The corresponding simulation results of the Novel proposed QCA 128Bit adders are shown below.

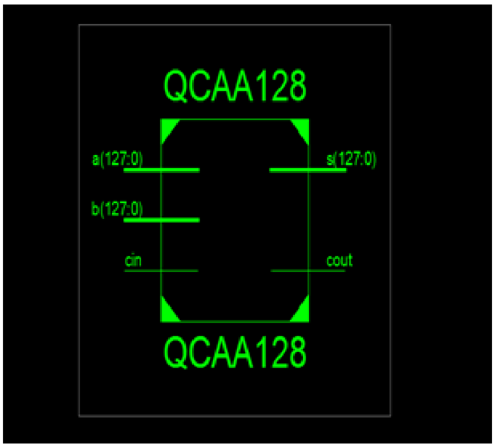


Fig.6 RTL schematic of Top-level of Novel QCA 128Bit Adder

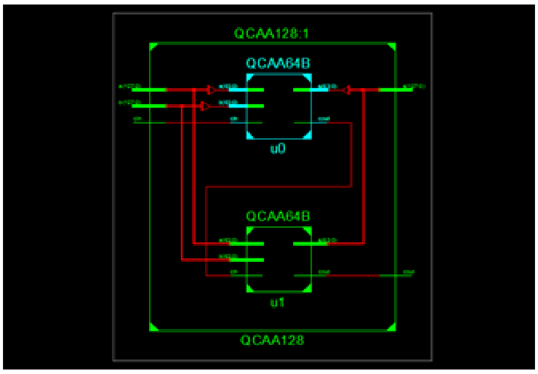


Fig.7 RTL Internal block of Novel QCA 128Bit Adder

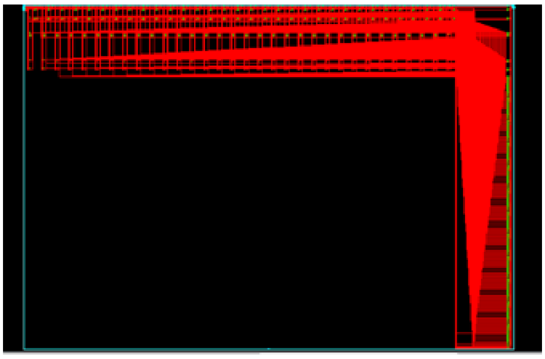
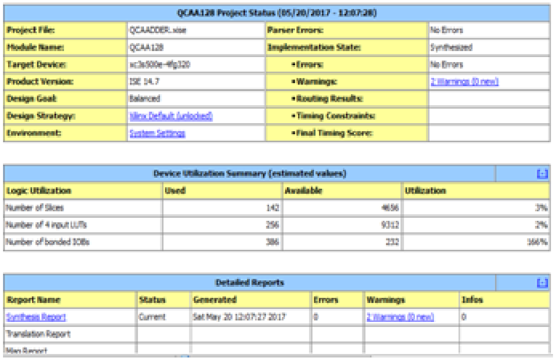


Fig.8 Technology schematic of Novel QCA 128Bit Adder



QCAA128 Project Status (05/20/2017 - 12:07:28)			
Project File:	QCAADDER.xise	Parser Errors:	No Errors
Module Name:	QCAA128	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	•Errors:	No Errors
Product Version:	ISE 14.7	•Warnings:	2 Warnings (0 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	142	4656	3%
Number of 4 input LUTs	256	9312	2%
Number of bonded IOBs	386	232	166%

Detailed Reports					[-]
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat May 20 12:07:27 2017	0	2 Warnings (0 new)	0
Translation Report					
Map Report					

Fig.9 Synthesis design report of Novel QCA 128Bit Adder

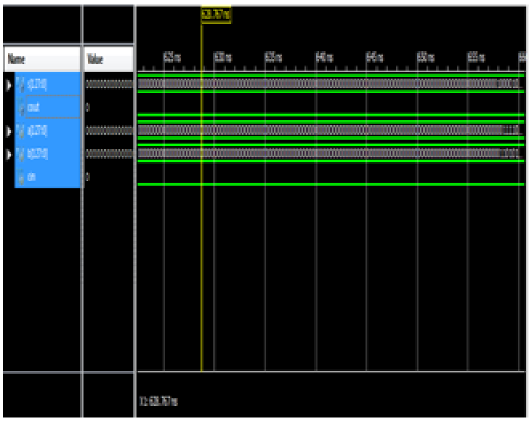


Fig.10 Simulated output for Novel QCA 128Bit Adder

V. CONCLUSION:

A simple approach is proposed in this paper to reduce the area and power of adder architecture. The logic operations eliminated all the redundant logic operations of the conventional adder and proposed a new logic formulation for the adder. A new 128-bit adder designed in QCA was presented. This novel adder is operated in RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than existing adders. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated in [13] and [16]. The design and implementation was verified by using Xilinx ISE 14.7 simulation tool The Future extension of our work is to design digital multipliers in QCA using proposed area efficient and high speed structures.

REFERENCES:

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, “Quantum cellular automata,” Nanotechnology, vol. 4, no. 1, pp. 49–57, 1993.

[2] M. T. Niemer and P. M. Kogge, “Problems in designing with QCAs: Layout = Timing,” Int. J. Circuit Theory Appl., vol. 29, no. 1, pp. 49–62, 2001.

[3] J. Huang and F. Lombardi, Design and Test of Digital Circuits by Quantum-Dot Cellular Automata. Norwood, MA, USA: Artech House, 2007.

[4] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, Jr., "Design rules for quantum-dot cellular automata," in Proc. IEEE Int. Symp. Circuits Syst., May 2011, pp. 2361–2364.

[5] K. Kim, K. Wu, and R. Karri, "Toward designing robust QCA architectures in the presence of sneak noise paths," in Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit., Mar. 2005, pp. 1214–1219.

[6] K. Kong, Y. Shang, and R. Lu, "An optimized majority logic synthesis methology for quantum-dot cellular automata," IEEE Trans. Nanotechnol., vol. 9, no. 2, pp. 170–183, Mar. 2010.

[7] K. Walus, G. A. Jullien, and V. S. Dimitrov, "Computer arithmetic structures for quantum cellular automata," in Proc. Asilomar Conf. Sygnals, Syst. Comput., Nov. 2003, pp. 1435–1439.

[8] J. D. Wood and D. Tougaw, "Matrix multiplication using quantumdot cellular automata to implement conventional microelectronics," IEEE Trans. Nanotechnol., vol. 10, no. 5, pp. 1036–1042, Sep. 2011.

[9] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power full adders based on majority-not gates," Microelectron. J., vol. 40, pp. 126–130, Jan. 2009.

[10] L. Lu, W. Liu, M. O'Neill, and E. E. Swartzlander, Jr., "QCA systolic array design," IEEE Trans. Comput., vol. 62, no. 3, pp. 548–560, Mar. 2013.

[11] H. Cho and E. E. Swartzlander, "Adder design and analyses for quantum-dot cellular automata," IEEE Trans. Nanotechnol., vol. 6, no. 3, pp. 374–383, May 2007.

[12] H. Cho and E. E. Swartzlander, "Adder and multiplier design in quantum-dot cellular automata," IEEE Trans. Comput., vol. 58, no. 6, pp. 721–727, Jun. 2009.

[13] V. Pudi and K. Sridharan, "Low complexity design of ripple carry and Brent–Kung adders in QCA," IEEE Trans. Nanotechnol., vol. 11, no. 1, pp. 105–119, Jan. 2012.

[14] V. Pudi and K. Sridharan, "Efficient design of a hybrid adder in quantumdot cellular automata," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 9, pp. 1535–1548, Sep. 2011.

[15] S. Perri and P. Corsonello, "New methodology for the design of efficient binary addition in QCA," IEEE Trans. Nanotechnol., vol. 11, no. 6, pp. 1192–1200, Nov. 2012.

[16] V. Pudi and K. Sridharan, "New decomposition theorems on majority logic for low-delay adder designs in quantum dot cellular automata," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 10, pp. 678–682, Oct. 2012.

[17] K. Walus and G. A. Jullien, "Design tools for an emerging SoC technology: Quantum-dot cellular automata," Proc. IEEE, vol. 94, no. 6, pp. 1225–1244, Jun. 2006.

[18] S. Bhanja, M. Ottavi, S. Pontarelli, and F. Lombardi, "QCA circuits for robust coplanar crossing," J. Electron. Testing, Theory Appl., vol. 23, no. 2, pp. 193–210, Jun. 2007.

[19] A. Gin, P. D. Tougaw, and S. Williams, "An alternative geometry for quantum dot cellular automata," J. Appl. Phys., vol. 85, no. 12, pp. 8281–8286, 1999. [20] A. Chaudhary, D. Z. Chen, X. S. Hu,

and M. T. Niemer, “Fabricatable interconnect and molecular QCA circuits,” IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 26, no. 11, pp. 1977–1991, Nov. 2007.

[21] M. Janez, P. Pecar, and M. Mraz, “Layout design of manufacturable quantum-dot cellular automata,” Microelectron.J., vol. 43, no. 7, pp. 501–513, 2012.