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Design of Compact Reversible Bidirectional Shifters for Arithmetic and Logic Unit

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ABSTRACT:
The development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In this paper we propose an approach for the design of n-bit reversible bidirectional barrel shifter using compact reversible logic gates. The proposed bidirectional barrel shifter can shift at most (n - 1) bits using logn bits select input whereas the existing reversible barrel shifters can shift at most logn bits using the same number of select inputs. All the synthesis and simulation are performed on Xilinx ISE 14.7 using Verilog HDL. The proposed reversible compact barrel shifter design for Arithmetic and Logical Unit(ALU). A comparative analysis has been presented to show the significant improvement of our proposed design with respect to the existing approaches in terms of numbers of gates, garbage outputs and quantum cost.

I. INTRODUCTION:
Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit if it is constructed using the reversible logic gates will allow the recovery of the information. In 1960s R. Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware, results in energy dissipation due to information loss [1].He showed that the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzman's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that this KTln2 joules of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits [2]. In reversible logic, there is a one to one mapping between inputs and outputs and for this reason no information is lost. Reversible logic is widely used in the fields of Quantum Computing, Nanotechnology, DNA Computing etc. Different architectures of reversible barrel shifter [1], [2], [3] have been proposed in literature which can rotate at most logn-bit for n-bit input. In this paper, a novel approach of reversible barrel shifter is proposed where maximum shift amount is (n − 1) bit. The proposed design performs rotation operation in both directions and it requires less number of gates, quantum cost and garbage outputs.

II. PRIOR WORK
This section presents the basic definitions regarding reversible logic.

A. Reversible Gate
Reversible gate is an n-input and n-output (denoted by n × n) circuit that produces a unique output pattern for each possible input pattern [4]. In other words, reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one-to-one correspondence between the vector of inputs and outputs. In this paper, we use some reversible gates, such as Feynman Gate (FG) [5] , Modified Fredkin Gate (MFG) [6], Peres Gate (PG) [7], Fredkin Gate (FRG) [8] and BJN Gate [9], to design our proposed circuit.

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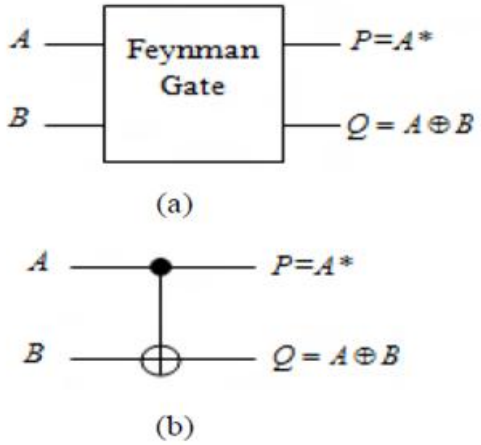

Figure 1. (a) Block diagram of 2x2 Feynman gate and (b) Equivalent quantum representation

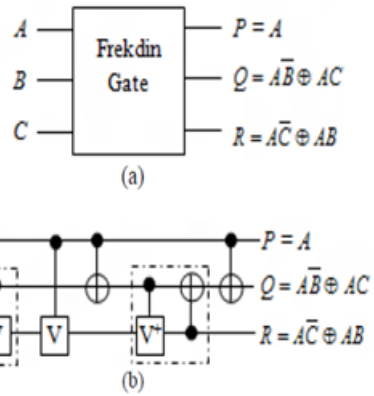

Figure 2. (a) Block diagram of 3*3 Frekdin gate and (b) Equivalent quantum representation

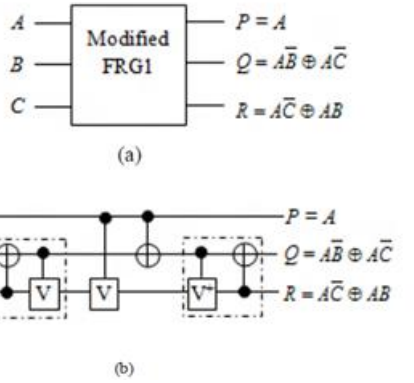

Figure 3. (a) Block diagram of Modified FRG and (b) Equivalent quantum representation

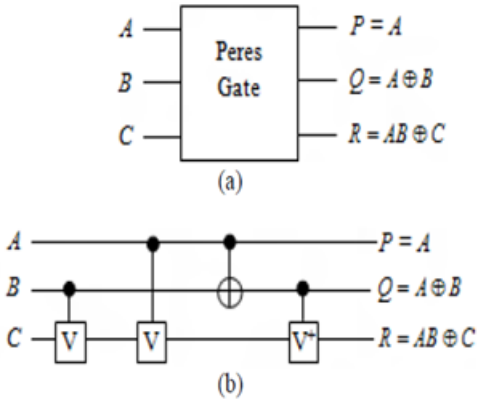

Figure 4. (a) Block diagram of 3*3 Peres and (b) Equivalent quantum representation.

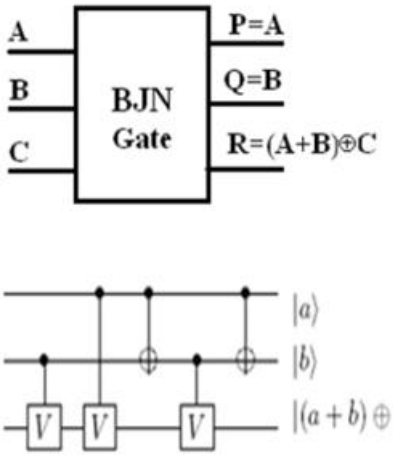

Figure 5. (a) BJN Gate - 3*3 gate and (b) Quantum realization of BJN gate

B. Garbage Outputs

Unwanted or unused output of a reversible gate (or circuit) is known as garbage output [10]. The garbage outputs are needed only to maintain the reversibility.

C. Quantum Cost

The quantum cost of a reversible gate (circuit) is the number of elementary quantum gates required to realize a reversible function [11]. The most used elementary quantum gate are NOT gate, controlled-NOT (CNOT) gate, controlled-V gate and controlled V^+ gate.

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III. LITERATURE SURVEY

Gorgin et al. [1] proposed a reversible unidirectional logarithmic barrel shifter. In that paper, the shift value is at most logn bits for an n-bit data input and the design requires large number of gates, quantum cost and garbage outputs. Hashmi et al. [2] proposed a reversible unidirectional logarithmic barrel shifter which requires less number of gates, quantum cost and garbage outputs than [1]. But, the design can rotate at most logn bits for an n-bit data input. Aradhiya et al. [3] proposed a reversible barrel shifter which can perform rotate and shift operations in both directions. But no generalized design is shown in this paper and the design has more quantum cost than previous designs [1], [2].

IV. PROPOSED REVERSIBLE BIDIRECTIONAL BARREL SHIFTER

This section presents the proposed architecture of reversible barrel shifter which performs rotate operation in both directions. If the data input is of n-bit and the maximum shift amount is b-bit then the barrel shifter is defined as (n, b) barrel shifter. The select input is of logn-bit which represents the shift amount. There is one control input d_{ir} which represents the direction of the rotation (left or right). When control input d_{ir} is 1, a left rotation is performed. Otherwise, a right rotation is performed. According to [12], if an n-bit data input is right rotated by b-bit, it is equivalent to an (n − b)-bit left rotation. Besides, if n is a integer power of 2, then (n − b) is the 2's complement of b [13]. Based on this concept, when d_{ir} = 1, select input is 2's complemented and a right rotation is performed based on 2's complemented select input. When di_r = 0, the select input is kept unchanged. A 1-bit (S_1 = 0, S_0 = 1) right rotation is equivalent to a 3-bit (2's complement of 1) left rotation. This statement is true for all other values of select input as long as number of bits of data input is a power of two. The data inputs are divided into pairs, where bits in each pair swaps for a particular condition. The conditions for swapping are calculated from the select input.

So, the proposed bidirectional barrel shifter can be divided into 3 components:

1) 2's complement generator,

2) swap condition generator and

3) right rotator. A simplified block diagram is shown in Figure 6 to realize the bidirectional barrel shifter. The detail circuit of the proposed reversible bidirectional barrel shifter is presented in later sections.

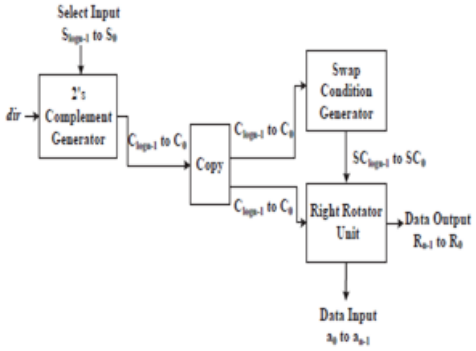

Figure 6: Simple Block Diagram of the Proposed Barrel Shifter

A. Proposed Reversible 3 × 3 Modified BJN Gate

We propose a 3×3 reversible Modified BJN gate (MBJN) to minimize the quantum cost of the proposed reversible 2's complement generator. This gate is a modified version of existing reversible BJN gate [9]. The proposed gate maps three inputs (A, B, C) to three outputs (A, A⊕B, (A+B)⊕C) and maintains a one-to-one relationship between them. Figure 7 (a) and 2 (b) represent the block diagram and quantum realization of proposed reversible MBJN gate. The proposed MBJN gate requires quantum cost of 4.

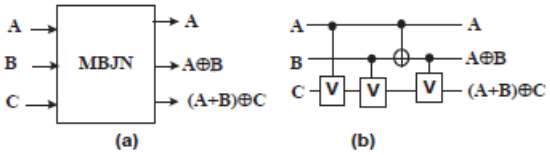

Figure 7: (a) Block Diagram and (b) Quantum Realization of Proposed Reversible MBJN Gate

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B. Proposed Reversible 2's Complement Generator

According to [13], the 2's complement of a binary number can be calculated in two steps: 1) find 1's complement by complementing each bit and 2) addition of 1 to the leastsignificant-bit (lsb) position. In this paper, 2's complement of the select input is generated without using any adder circuitry. Algorithm 1 is presented to generate 2's complement of lognbit select input of an n-bit barrel shifter.

Algorithm 1 2's Complement Generator

Input: Select input S_{logn-1} to S_0, Control input dir
Output: Modified Select input C_{logn-1} to C_0
$C_0 = S_0$
$C_1 = S_0 \oplus S_1$
for $i = 2 \rightarrow (logn - 1)$
  $C_i = S_i \oplus (S_{i-1}$ OR S_{i-2} OR ... OR $S_0)$
end for
if $dir = 1$ then
  return C_{logn-1} to C_0
else
  return S_{logn-1} to S_0
end if

Let, the 2's complement of select input Si be C_i , where $0 \leq i \leq logn - 1$. According to Algorithm 1, the lsb (S0) of the select input is equivalent to it's 2's complement. If index i is one, the 2's complement of Si is the XOR of the lsb and the bit itself. To generate the bits at index $i \geq 2$, the corresponding bit is XORed with the OR of all bits at lower positions. For example, the 2's complement of bit S_2 is $S_2 \oplus (S_1 + S_0)$. If control input dir is zero, select input Si is returned. Otherwise, 2's complement of select input is returned, where, $0 \leq i \leq logn-1$. A 2-bit and 3-bit 2's complement generator as shown in Figure 8 (a) and 3 (b). Proposed 2 and 3-bit reversible 2's complement generator needs total 3 and 5 gates with quantum cost of 6 and 14, respectively.

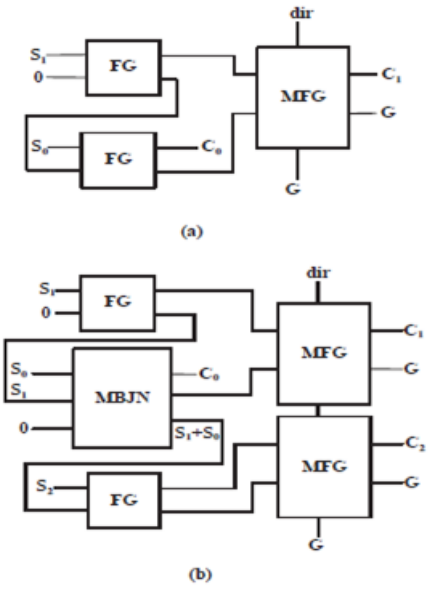

Figure 8: (a) 2-Bit and (b) 3-Bit Reversible 2's Complement Generator

Lemma 1: Let GC be the number of gates, QC be the quantum cost and GO be the number of garbage outputs of an logn-bit reversible 2's complement generator of an n-bit barrel shifter. Then, GC = 2logn − 1, QC = 8logn − 10 and GO = logn.

C. Proposed Reversible Swap Condition Generator

This unit generates swap conditions to swap bits in a pair of data inputs in n(> 4)-bit right rotator unit. The outputs of 2's complement generator are fed to swap condition generator as inputs. An n-bit data input can be divided into n/2 number of pairs. Since each pair needs a particular swap condition, we need total n/2 number of conditions. A methodology to implement a swap condition generator is explained with the following example:

Input: Outputs of 2's complement generator C_{logn-1} to C_0.
Output: Swap conditions $SC_{n/2-1}$ to SC_0.

Step 1: Swap condition for pair0 is the msb of the select input and swap condition for pair n 4 is 2nd msb

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of the select input. For example, a 16-bit data input needs 8 swap conditions where, $SC_0 = C_3$, $SC_4 = C_2$.

Step 2: For Swap conditions that are greater than zero and less than n/4 , perform C_{logn-2} AND outputs of (logn − 1)- bit swap condition generator that are greater than zero. For example, an 8-bit data input has 3-bit select input and swap conditions are, $SC_0 = C_2$, $SC_1 = (C_1$ AND $C_0)$, $SC_2 = C_1$, $SC_3 = (C_1$ OR $C_0)$. Similarly, a 16-bit data input has 4-bit select input and its swap condition is less than four, which are $SC1= C_2$ AND $(C_1$ AND $C_0)$, $SC_2 = C_2$ AND C_1, and so on.

Step 3: For Swap conditions that are greater than n/4 , perform C_{logn-2} OR outputs of (logn −1)-bit swap condition generator that are greater than zero. A 16-bit data input has 4-bit select input and its swap condition is greater than four, which are $SC_5= C_2$ OR $(C_1$ AND $C_0)$, $SC_6 = (C_2$ OR $C_1)$, and so on. A 3-bit and a 4-bit reversible swap condition generators are shown in Figures 9 and 10.

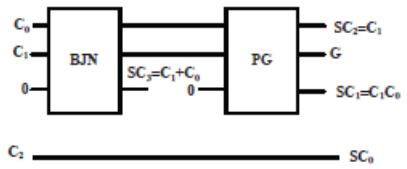

Figure 9: 3-Bit Reversible Swap Condition Generator

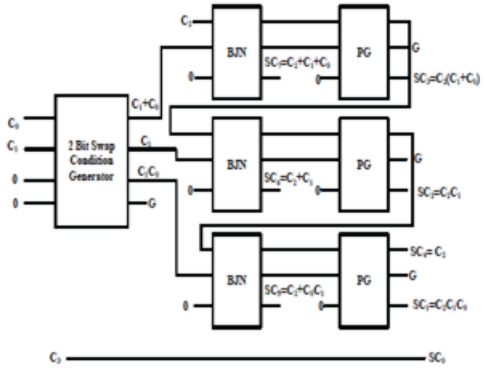

Figure 10: 4-Bit Reversible Swap Condition Generator

Lemma 2: Let GC be the number of gates, QC be the quantum cost and GO be the number of garbage outputs of an logn-bit reversible swap condition generator of an n-bit reversible barrel shifter. Then, GC = n − 2logn, QC = 9(n/2 − logn) and GO = n/2 − logn.

D. Proposed Reversible Right Rotator

An n-bit (n > 4) right rotator takes an n-bit data input, outputs of 2's complement generator and outputs of swap condition generator to rotate at most b(= n − 1) bits in right direction. In this section, first a (4, 3) reversible right rotator is presented and then a generalized approach is developed.

1) Proposed (4, 3) Reversible Right Rotator:

A (4, 3) reversible right rotator takes 4-bit data input, 2-bit select input from 2's complement generator and rotates at most three bits as shown in Figure 11. The swap condition generator is not needed for a (4, 3) reversible right rotator. The proposed circuit needs 5 gates with 21 quantum cost and it generates 2 garbage outputs. Proposed (4, 3) reversible right rotator is used to realize an nbit reversible right rotator.

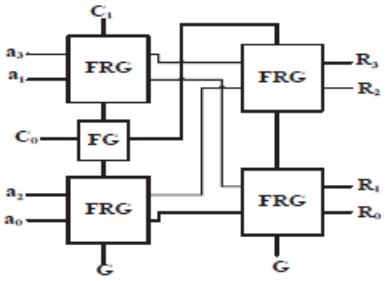

Figure 11: A (4,3) Reversible Right Rotator

2) Proposed Generalized Reversible Right Rotator:

A methodology to implement a right rotator is explained with the following example:

Input: Data inputs a_{n-1} to a_0, outputs of 2's complement generator C_{logn-1} to C_0, outputs of swap condition generator $SC_{n/2-1}$ to SC_0.

Output: Right Rotated Outputs R_{n-1} to R_0.

Step 1: Partition n-bit data input into two groups and take one bit from the 1st partition and one bit from the 2nd partition to form a pair.

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Step 2: Call the algorithm swap condition presented in Section IV-C. Bits in a pair are swapped if XOR of corresponding swap condition and msb of the select input is 1.

Step 3: Take the 1st bit of all pairs to form partition 1 and 2nd bit of all pairs to form partition 2. The bits in 1st partition and select input except the msb are fed to an n 2 -bit right rotator. Similarly, the bits in 2nd partition and select input except the msb are fed to an n 2 -bit right rotator. An n 2 -bit right rotator is called recursively until n becomes 4. When, n becomes 4, we need a 4-bit right rotator which is shown in Figure 11. The 1st rotator generates outputs Rn−1 to $R_{n/2}$ and the 2nd rotator produces outputs $R_{n/2-1}$ to R_0.

Lemma 3: Let GC be the number of gates, QC be the quantum cost and GO be the number of garbage outputs of an n-bit reversible right rotator unit. Then, GC = (3n /4 − 7)logn + 5n/2 + 3, QC = (3n − 29)logn + 19n/2 + 17 and GO = (n/2 − 3)logn + n/2 + 2.

V. 8-BIT PROPOSED REVERSIBLE BIDIRECTIONAL BARREL SHIFTER

In this section, the whole architecture of the proposed reversible bidirectional barrel shifter is presented. The three reversible components discussed in previous sections are combined to implement the proposed reversible bidirectional barrel shifter. The architecture of proposed reversible (8, 7) bidirectional barrel shifter is depicted in Figure 12.

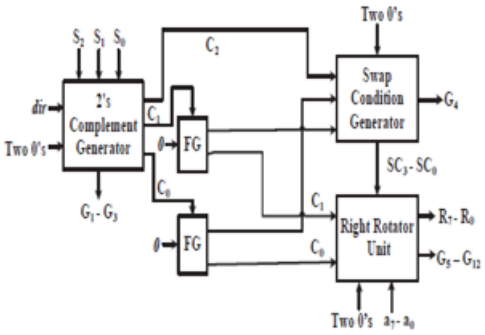

Figure 12: Block Diagram of (8, 7) Reversible Bidirectional Barrel Shifter

So, the reversible circuits presented in Section IV-B, IV-C and IV-D can be combined with additional FG gates to realize a generalized reversible bidirectional barrel shifter. The property of the proposed n-bit reversible bidirectional barrel shifter is presented in Lemma 4 to calculate the cost parameters such as gate count, quantum cost and garbage outputs. Lemma 4: Let GC be the number of gates, QC be the quantum cost and GO be the number of garbage outputs of an n-bit reversible bidirectional barrel shifter. Then, GC = (3n/ 4 − 7)logn + 7n/2 + 2, QC = (3n − 30)logn + 14n + 7 and GO = (n/2 − 3)logn + n + 2.

VI. COMPARATIVE STUDY

This section analyzes the proposed design of reversible bidirectional barrel shifter with existing designs in terms of gate count, quantum cost and garbage outputs. We compare the proposed reversible bidirectional 4-bit and 8-bit barrel shifters.

TABLE I: Comparison of Different 4-Bit Reversible Barrel Shifters

Circuit	Gate Count	Garbage Outputs	Quantum Cost	Properties
Proposed Circuit	8	4	27	Bidirectional
Existing [1]	24	14	72	Unidirectional
Existing [2]	10	6	34	Unidirectional
Existing [3]	11	7	53	Bidirectional

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TABLE II: Comparison of Different 8-Bit Reversible Barrel Shifters

Circuit	Gate Count	Garbage Outputs	Quantum Cost	Properties
Proposed Circuit	29	12	101	Bidirectional
Existing [1]	112	59	336	Unidirectional
Existing [2]	36	19	116	Unidirectional

TABLE III: Comparison of Different 16-Bit Reversible Barrel Shifters

Circuit	Gate Count	Garbage Outputs	Quantum Cost	Properties
Proposed Circuit	118	98	519	Bidirectional
Existing [1]	336	117	1008	Unidirectional

From Table I and II, we find that our proposed 4-bit, 8-bit and 16 bit reversible bidirectional barrel shifters require less number of gates, less quantum cost and produces less garbage outputs than existing designs [1], [2] and [3]. For example, the proposed 4-bit reversible barrel shifter is improved by 66.67%, 20% and 27.27% than existing designs [1], [2] and [3] in terms of gate count. Similarly, the proposed 8-bit reversible barrel shifter is improved by 74.10% and 19.44% than existing designs [1] and [2] in terms of gate count. Moreover, the proposed 8-bit reversible barrel shifter can shift up to 8−1 = 7 bits whereas, the existing designs [1] and [2] can shift up to log8 = 3 bits only.

VII. SIMULATION RESULTS:

All the synthesis and simulation results of the Proposed Reversible 16bit Bidirectional Barrel Shifters are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The corresponding simulation results of Proposed Reversible 16bit Bidirectional Barrel Shifters are shown below.

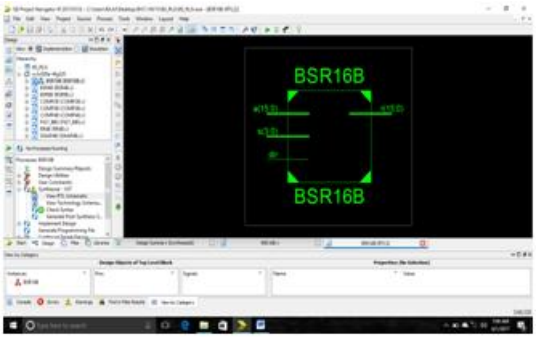

Figure 13: RTL schematic of Top-level of Proposed Reversible 16bit Bidirectional Barrel Shifter

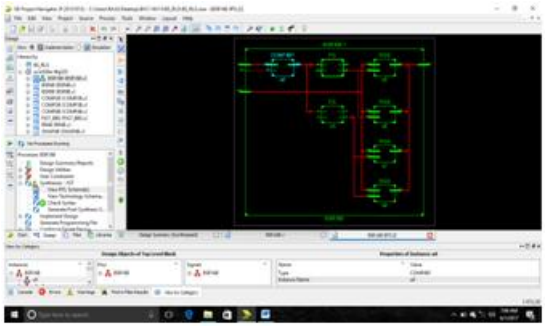

Figure 14: RTL schematic of Internal block of Proposed Reversible 16bit Bidirectional Barrel Shifter

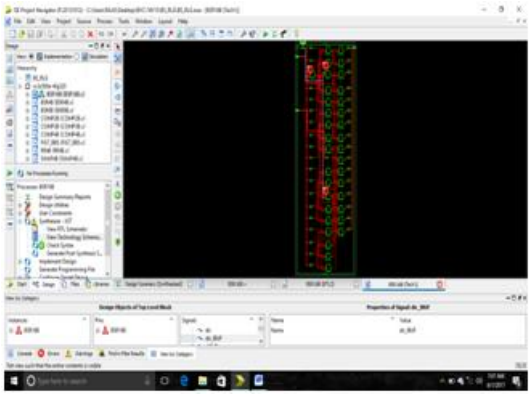

Figure 15: Technology schematic of Internal block of Proposed Reversible 16bit Bidirectional Barrel Shifter

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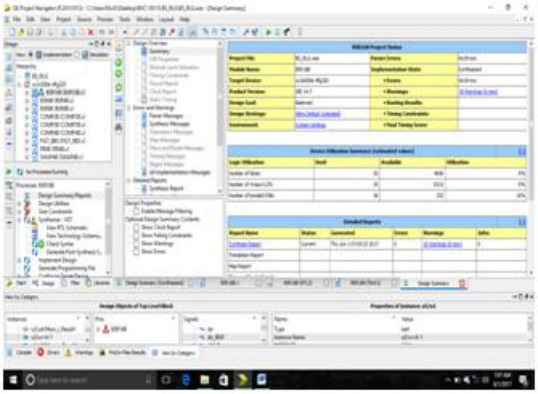

Figure 16: Synthesis summary report of Proposed Reversible 16bit Bidirectional Barrel Shifter

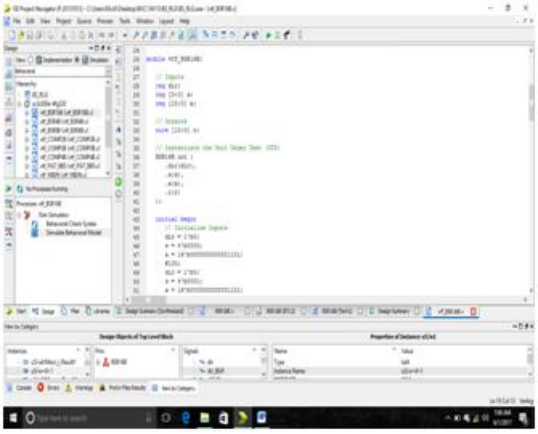

Figure 17: Test Bench for Proposed Reversible 16bit Bidirectional Barrel Shifter

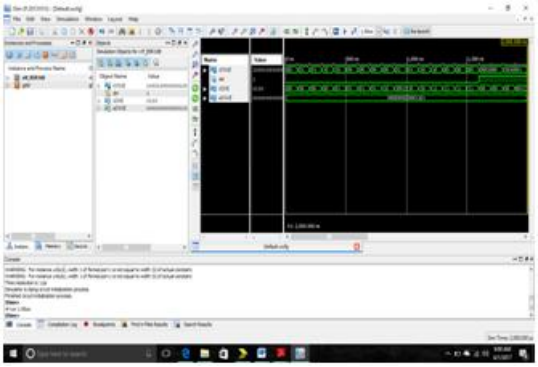

Figure 18: simulated outputs for Proposed Reversible 16bit Bidirectional Barrel Shifter

VIII. CONCLUSIONS:

This paper presented the design methodology of an efficient and generalized reversible barrel shifter. In the way of presenting the proposed design, a 2's complement generator is implemented using reversible logic which can be used in arithmetic circuits for signed number. Two algorithms have been presented to realize a cost efficient reversible bidirectional barrel shifter. A comparative study between existing and proposed works has been presented to show the efficiency of the proposed work. The proposed 8-bit reversible barrel shifter is improved by more than 50% in terms GC,QC and GO than existing designs [1]. Our proposed reversible barrel shifter can be used in reversible arithmetic logic unit which is a heart of a reversible processor. Besides, it can be used in other reversible arithmetic circuits for shifting operation [1], [2].

REFERENCES

[1] S. Gorgin and A. Kaivani, "Reversible barrel shifters," in Computer Systems and Applications, 2007. AICCSA '07. IEEE/ACS International Conference on, May 2007, pp. 479–483.

[2] I. Hashmi and H. M. H. Babu, "An efficient design of a reversible barrel shifter," in VLSI Design, 2010. VLSID'10. 23rd International Conference on. IEEE, 2010, pp. 93–98.

[3] H. V. R. Aradhya, J. Lakshmesha, and K. N. Muralidhara, "Design optimization of reversible logic universal barrel shifter for low power applications," International Journal of Computer Applications, vol. 40, no. 15, pp. 26–34, February 2012.

[4] P. Kerntopf, "A new heuristic algorithm for reversible logic synthesis," in Proceedings of the 41st annual Design Automation Conference. ACM, 2004, pp. 834–837.

[5] R. P. Feynman, "Quantum mechanical computers1," Foundations of Physics, vol. 16, no. 6, p. 986, 1985.

[6] M. S. Al Mamun, I. Mandal, and M. Hasanuzzaman, "Design of universal shift register using reversible logic," International Journal of

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Engineering and Technology, vol. 2, no. 9, pp. 1620–1625, September 2012.

[7] A. Peres, "Reversible logic and quantum computers," Physical review A, vol. 32, no. 6, pp. 3266–3276, 1985.

[8] E. Fredkin and T. Toffoli, Conservative logic. Springer, 2002.

[9] A. N. Nagamani, H. V. Jayashree, and H. R. Bhagyalakshmi, "Novel low power comparator design using reversible logic gates," Indian Journal of Computer Science and Engineering, vol. 2, no. 4, pp. 566–574, AugustSeptember 2011.

[10] D. Maslov and G. W. Dueck, "Garbage in reversible design of multiple output functions," in 6th International Symposium on Representations and Methodology of Future Computing Technologies, 2003, pp. 162– 170.

[11] M. A. Nielsen and I. L. Chuang, Quantum computation and quantum information. Cambridge university press, 2010.

[12] T. Thomson and H. Tam, "Barrel shifter," Jul. 29 1997, uS Patent 5,652,718. [13] R. J. Tocci, Digital Systems: principles and applications. Pearson Education India, 1980.