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Design and Implementation of MMC – HVDC Model



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ABSTRACT:

This project proposes an enhanced control method for a high-voltage direct- current (HVDC) modular multilevel converter (MMC). To control an MMC-HVDC system properly, the ac current, circulating current, and sub module (SM) capacitor voltage are considered.

The ac-side current is a fundamental frequency component, and the circulating current is a double-line frequency component. Existing control methods control the ac current and circulating current by separating each component.

However, the existing methods have a disadvantage in that the ac-side current must be separated into the positive and negative sequences for control under an unbalanced voltage condition. The circulating current consists of not only negative-sequence components but also positive- and zero-sequence components under an unbalanced voltage condition. Therefore, an additional control method is necessary to consider the positive- and zero-sequence components of the circulating current. The proposed control method has the advantage of controlling not only the ac-side current of the MMC but also the circulating current without separating each of the current components to control each arm current of the MMC.

In addition, it can stably control the positive and zero-sequence components of the circulating current under the unbalanced voltage condition.

INTRODUCTION

With extensive research and applications, VSC technology has gradually achieved a high degree of maturity, and there has been numerous projects on VSC-based HVDC applications, including the applications of MTDC and renewable energy integration in recent years. There has been a variety of topologies with the VSC development. Among them, one of these, the MMC, has salient features and shows its strong competitiveness, which has been well recognized by research and applications. Since there are a number of energy capacitors in the SMs of the MMCs, it is important to precharge these capacitors during the startup stage and the system startup control is essential. In, a startup control scheme for the MMC was proposed.

The proposed control scheme was based on the control of an auxiliary voltage source at the MMC dc-side. However, it is generally expected to start a system without auxiliary sources, which saves space and costs. In a startup technique using additional resistors was proposed. The resistors were connected on the converter arms and were inserted/bypassed to limit the arm current. However, the additional resistive losses were not expected. In a startup scheme with a two-stage charging process for MMC was proposed. Although the proposed charging scheme seemed to achieve charging the voltage of each SM capacitor to the rated value without auxiliary dc source, it had two main problems.

First, in the first charging stage, the dc voltage was assumed to be the rated value and the charging of the SM

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A Peer Reviewed Open Access International Journal

capacitors was from the dc side. Under this assumption, the proposed scheme was only valid for the MMC under inverter operations. Second, in the second charging stage, the proposed scheme was that the SM capacitor voltages were charged to the rated value when the SMs were deblocked. However, the main objective of the start-up control of MMC is to pre-charge the SM capacitors to the rated value before they are deblocked.

A start-up scheme for MMC HVDC was proposed in including the calculation of the limiting resistance, the setting of the rising slope of dc voltage and the reference setting of reactive power. In, a calculation method for the minimum limiting resistance was proposed. In, the dynamics of the SMs in the MMC during the pre-charging process were analyzed and an optimized modulation algorithm was proposed for reducing the current surges when deblocking the MMC.

Theoretically, an MMC can be deblocked at zero voltage difference and the current surges under this condition are the smallest. However, the control scheme proposed in did not achieve zero voltage difference when deblocking the MMC. The start-up schemes proposed above were all based on two-terminal MMC HVDC systems. In, a three-terminal MMC HVDC system based on a real application was investigated, and a control procedure of starting the system was proposed in detail. However, these procedures were obtained as a conceptual approach, which was based on the analysis at systematic level. There was no analysis on the dynamics of the SMs in the MMC with no comprehensive simulation results. Different sequential startup control was compared in, while most comparisons were based on simulations and the analysis were not comprehensive with no mathematical derivations. Hence, the startup control including the startup sequence of MMC MTDC systems deserves our study and exploration. This project investigates the start-up process of an OWF integrated MMC MTDC system with the main contributions given as follows.

1. Regarding an MMC MTDC system with active ac networks, the mathematical model before and after the deblocking of the converter is further developed on into a second-order circuit with the consideration of the converter arm inductor. A hierarchical start-up control scheme is proposed. Considering the fact that an OWF is a passive ac network before the completion of its start-up, a start-up control strategy for the converter connecting with the OWF with deblocking the converter at zero voltage difference on SMs is proposed;
2. A four-terminal MMC HVDC system is established on the RTDS with one terminal connecting with an OWF. The effectiveness of the proposed sequential start-up control scheme is verified by the simulation results. The superiority of the proposed scheme, in terms of mitigating the voltage spikes and current surges, than other control schemes is compared, and the easy implementation of the proposed scheme is presented;
3. The proposed start-up control scheme is validated on the MMC MTDC system with master–slave control and droop control, respectively.

HVDC TRANSMISSION SYSTEM

The decision for the installation of HVDC over HVAC involves capital investments and losses. A DC line with two conductors can carry the same amount of power as an AC line with three conductors of the same size and insulation parameters. This results in smaller footprint and simpler design of towers, reduced conductor and insulation costs. Moreover, line investments are reduced by absence of compensation devices, since DC lines do not consume reactive power. Power losses are reduced due to 30% reduction in conduction losses, minimized corona effect and smaller dielectric losses in case of a cable. The breakeven distance, where DC system tends to be more economic than AC for the overhead lines can vary within 400-700 km, while for the cable systems it is around 25-50 km, depending on particular requirements.

The HVDC transmission technology based on high-power electronic devices is widely used nowadays in electrical systems for the transmission of large amounts of power over long distances.

The transformation from AC to DC and vice versa is realized by two converter types:

- Current-Source Converters (CSC);

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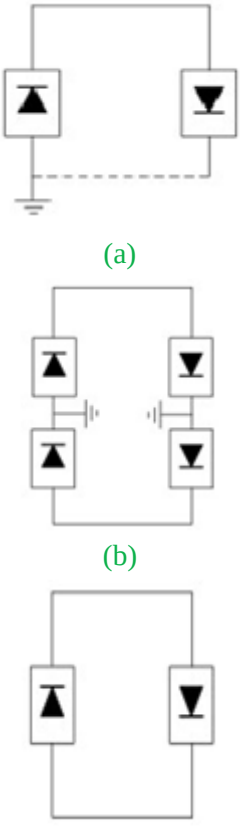
- Voltage-Source Converters (VSC).

CONFIGURATION OF HVDC TRANSMISSON

Depending on functional aspects, three main HVDC configurations shown in Figure 2.1 are used.

Mono polar configuration (a) - interconnects two converter stations via a single line, with the possibility to operate at both DC polarities. Ground, sea or metallic conductor can be used for return path.

Bipolar configuration (b) - involves two conductors, operating at opposite polarities. This results in two independent DC circuits, rated at half capacity each. During outages of one pole, a mono polar operation can be used. This is the most common configuration for modern HVDC transmission.



(a)

(b)

(c)

Fig 2.1 - HVDC system configurations. (a) Mono polar. (b) Bipolar. (c) Back-to-back

In Back-to-Back configuration (c) - the DC sides of two converters are directly connected, having no DC transmission line. This arrangement is used for the interconnection of asynchronous AC systems.

The typical configuration of modern VSC-HVDC transmission system is shown in Figure 2.3. Two DC conductors of opposite polarity interconnect two converter stations. The polarity of the DC-link voltage remains the same while the DC current is reversed when the direction of the power transfer has to be changed

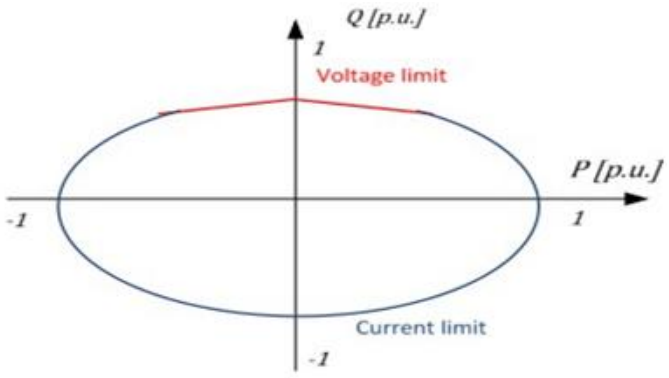


Fig 2.2 - Active-reactive locus diagram of VSC-HVDC transmission

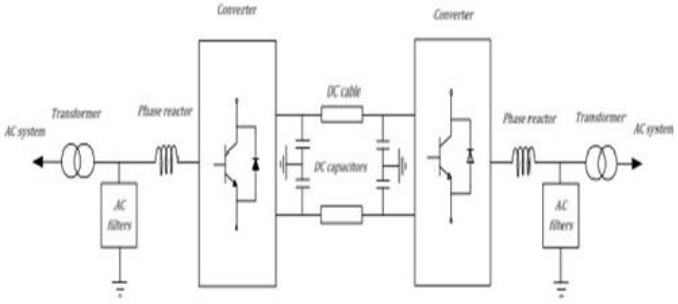


Fig 2.3 - VSC-HVDC system configuration

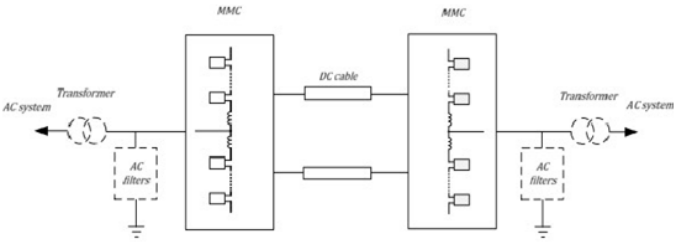


Fig 2.4 - MMC-HVDC system configuration

The DC side capacitors ensure support and filtering of the DC voltage. The converter AC terminals are connected with phase reactors and harmonic filters. The phase reactors ensure control of power exchange between the converter and AC system, the limitation of

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fault currents and blocking of current harmonics appearing due to PWM. The AC filters reduce harmonics content on the AC bus voltage. Power transformers are used to interface the AC system, adapting converter and AC system voltages as well as participate in power regulation by means of tap changers.

MODULATION TECHNIQUES OF MMC

Multilevel modulation methods can be split into two main categories:
Space Vector Modulation (SVM) and Voltage level Based Modulation; i.e. Carrier PWM (CPWM) and Nearest Level Modulation.

Space vector modulation

The Space Vector Modulation theory is well established nowadays. Due to its advantages, such as easy digital implementation and the possibility of optimizing the switching sequences, it is an attractive modulation technique for multilevel converters. The principle applied for the calculation of the voltage vectors in two or three level converters can be extended to multilevel converters. However, the complexity of the algorithms for the calculation of the state vectors and computational costs increase with the number of levels. Recent publications have presented strategies where simpler algorithms are used; accordingly the computational efforts are significantly reduced, comparing with conventional SVM techniques.

Multi carrier modulation

The Carrier-based Pulse-Width Modulation concept is based on comparison of a reference (modulating) signal with a high-frequency triangular waveform (the carrier). The carrier can have a periodic bipolar or unipolar waveform. The switching instants are determined by the intersections of the modulating and carrier signals.

When the reference is sampled through the number of carrier waveforms, the PWM technique is considered as a multicarrier PWM. The multicarrier PWM implementation in multi-cell converter topologies is especially advantageous because each carrier can be assigned to a particular cell which allows independent cell modulation and control.

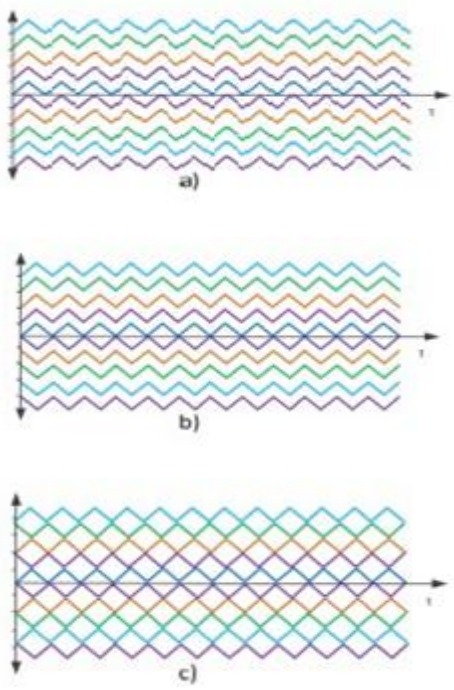

Fig3.4 - Level shifted PMW carriers. (a) Phase Disposition (PD) (b) phase opposition disposition (POD) (c) alternate phase opposition disposition (APOD)

The carriers can be displaced within levels (Level-shifted PWM), have phase shifts (phase-shifted PWM) or have a combination of them. The level-shifted PWM (LS-PWM) has N-1 carrier signals with the same amplitude and frequency, relating each carrier with the possible output voltage level generated.

Depending on the way the carriers are located, they can be in phase disposition (PD-PWM), phase opposition disposition (POD-PWM), or alternate phase opposition disposition (APOD-PWM) as shown in Figure3.4.

The LS-PWM methods produce an unequal duty and power distribution among the sub-modules since the vertical shifts relate each carrier and output level to a particular cell. These can be corrected by implementing carrier rotation and signal distribution techniques. The Carrier phase shifted method (PS-PWM) has N-1 carrier signals with the same amplitude and frequency.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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To achieve a staircase multilevel output waveform, the phase shift between the carriers is calculated as φ = 3605/'N − 1. The multicarrier PS-PWM process is shown in Figure 3.5.

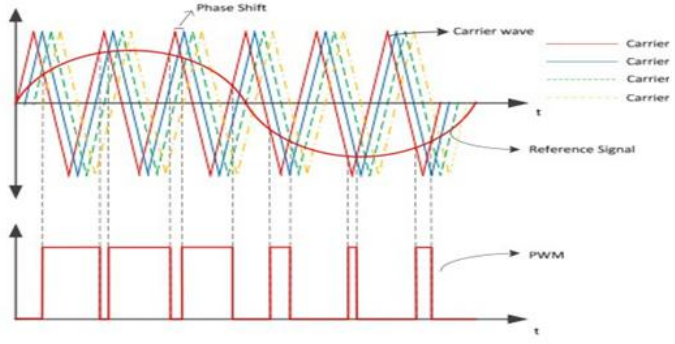

Fig 3.5 - Phase Shifted PWM

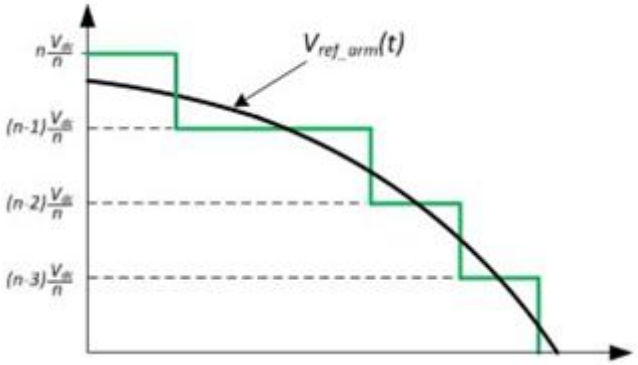

Fig 3.6 -Nearest Level Modulation, arm voltage waveform

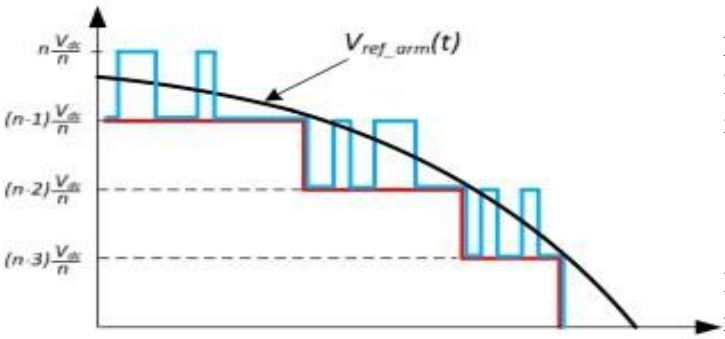

Fig 3.7 - Nearest Level Modulation, arm voltage waveform with SM modulation.

This approach provides equal duty and power distribution between the cells and, by selecting an adequate carrier frequency, capacitor voltage balancing can be achieved. A comprehensive analysis of the Multicarrier PWM techniques was performed in where the mentioned methods were extended and analysed particularly for MMC applications.

MMC – HVDC MODEL DELOPMENT

In this chapter a model of MMC-HVDC transmission system is developed and tested. First, the inner control techniques for the MMC are discussed and proven through simulations. Then, the outer control loops for the VSC-HVDC transmission systems are presented.

In this project, the MMC Inner Control shall be referred to the control of the sub-module capacitor voltages and the circulating current. The outer controls denote the control loops implemented for the regulation of the output parameters of the converter; e.g. current control, DC voltage control and PQ control.

Energy Control

In this method the arm capacitor voltages are kept to a reference through the control of the total stored energy m[in the phase leg and the difference between the energy stored in the upper and lower arms. An open loop approach using the estimation of the stored energy is proposed with the intention of increasing the stability of the system and avoiding the need of a continuous measurement of the capacitors voltage to calculate the converter stored energy.

Distributed control

In this the cell capacitor voltages are controlled independently. The control is implemented in two parts.

- Averaging part, implemented per phase-leg
- Balancing part, implemented in each sub-module

In Figure 4.1 the block diagram of the distributed control method is presented. As it can be observed, the averaging control is implemented in two loops, outer voltage loop and inner current loop. The voltage loop is responsible of controlling the mean value of the capacitor voltages in the leg by influencing each cell individually. The error signal is processed in the controller, resulting in the reference signal for the difference current loop. Under the balanced conditions, the DC component of the difference current is equal to 1/3 of the DC-link current,

ISSN No: 2348-4845
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therefore a feed-forward term is added to increase the response of the controller as highlighted in Figure 4.1.

If the average voltage is lower than the desired value, a positive current reference is obtained. The current reference is subtracted from the measured value, reducing the control command. By this means, the DC component of the difference current is increased, rising the charge in the capacitors.

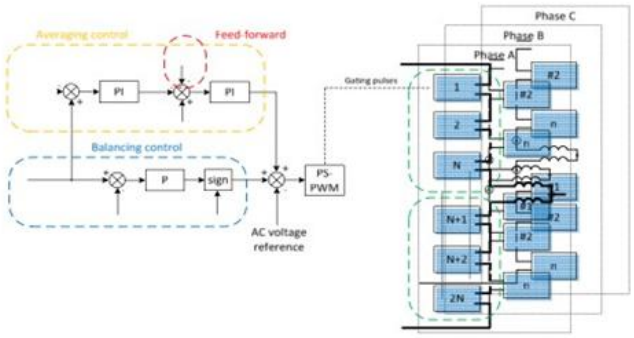

Fig 4.1 - Distributed Control, block diagram

The average charge of the capacitors depends on the DC component of the difference current. If only an integral compensator is used, the DC value of the difference current is controlled, making in no effect on the circulating current. The compensator in the current loop acts on the AC component of the difference current. The Balancing control is implemented in each sub-module individually. The control signal is generated based on the capacitor voltage and the direction of the corresponding arm current. The final sub-module voltage reference is obtained by adding both averaging and balancing control signals to the voltage reference.

HVDC CONTROLS

In HVDC transmission system the outer control regulates the power transfer between the AC and DC systems. The active and reactive power is regulated by the phase and the amplitude of the converter line currents with respect to the PCC voltage. The control structure for conventional VSC-HVDC systems consists of a fast inner current control loop and outer control loops, depending on the application requirements HVDC controls are shown in figure 4.2.

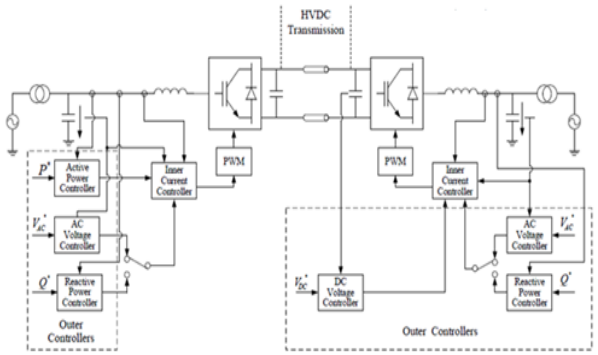

Fig 4.2 Overall control structure of the VSC-HVDC transmission system

The current loop is responsible for fast tracking of references generated in the power controller, DC or AC voltage controllers. When operating in inverter mode, the converter controls the DC-link voltage at predefined value. To achieve this, the DC voltage controller adjusts the active current reference in such a way, that the net imbalance of power exchange between the DC and AC systems is kept to zero .In rectifier mode the converter tracks active power references directly. The reactive power at both sides can be controlled independently. It can be regulated to track a reference, thus regulating power factor at the PCC or to control of the AC grid voltage at the PCC. A phase locked loop (PLL) is used for the synchronisation with the grid voltage. The PLL mechanism is able to detect phase angle and the magnitude of the grid voltage, to be later used in the controls. The grid frequency can also be obtained from PLL.

Phase Locked Loop

The grid synchronization is a very important and necessary feature of grid side converter control. The synchronization algorithm is able to detect the phase angle of grid voltage in order to synchronize the delivered power. Moreover, the phase angle plays an important role in control, being used in different transformation modules, as Park's transformation.

There are several methods capable to detect the phase angle: the zero crossing detection, the filtering of grid

ISSN No: 2348-4845
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voltages and the phase locked loop (PLL) technique.PLL is a phase tracking algorithm, which is able to provide an output synchronized with its reference input in both frequency and phase. The purposed of this method is to synchronize the inverter output current with the grid voltage, in order to obtain a unitary power factor.

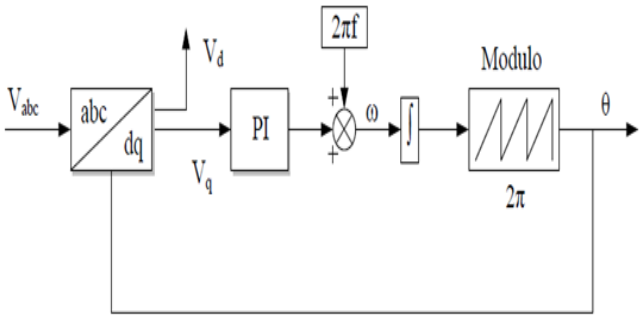

Fig 4.3 Block diagram of PLL

The block diagram of the PLL algorithm implemented in the synchronous reference frame is presented in Figure 4.3. The inputs of the PLL model are the three phase voltages measured on the grid side as well as source side and the output is the tracked phase angle. The PLL model is implemented in d-q synchronous reference frame, which means that a Park transformation is needed. The phase locking of this system is realized by controlling the q-axis voltage to zero. Normally, a PI controller is used for this purpose. By integrating the sum between the PI output and the reference frequency the phase angle is obtained.

Current Control Loop

The inner current controller is implemented in the d-q synchronous reference frame. Usually, the d-q control structures are associated with PI controllers due to their good behavior when regulating DC variables. However the PI current controllers have no satisfactory tracking performances. Therefore, in order to improve the performances of the PI current controllers in such systems, cross-coupling terms and voltage feed forward is usually used

The structure of the inner current controller implemented in the synchronous reference frame is presented in Figure 4.4.

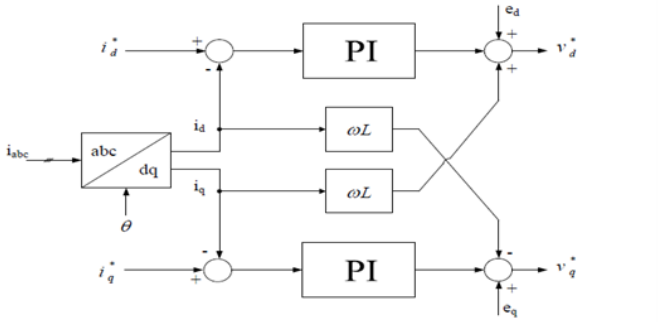

Fig 4.4 The Inner current controller implemented in synchronous reference frame

CONVERTER CURRENT LIMITATION

The described control strategies have shown an increase in the AC currents due to change in grid conditions. Depending on the particular conditions of the grid unbalance, these currents may exceed the limits of the converter devices, thus tripping the over current protection. A current-limiting mechanism should be implemented in order to ensure stable and continuous converter operation during faults.

- Calculation of AC current limits
- Validation of current limitation strategy
- Maximum active power injection
- Maximum reactive power injection

The arm currents fall into the imposed limits within 3 fundamental cycles, because of the ramped change of power references. However, after stabilization, the limits for the arm and AC currents are not exceeded. With the injection of reactive power, the grid voltage is raised. Thus the converter provides grid voltage support with maximum allowed reactive current injection.

BASIC STRUCTURE

Figure.5.1 shows a single-line schematic diagram of an MMC MTDC system with the integration of an OWF. Both the offshore and onshore MMCs connect to the ac power sources, either the OWF or ac utility grids, through a three-phase transformer.

The MTDC network can be in either radial or meshed arrangement. For the sake of simplicity, the MTDC investigated in this project is in radial connection only.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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In Figure.5.1, denotes each terminal of the MTDC system; denotes the AC circuit breaker at each terminal; denotes the common connecting point of the ac network. Fig. 5.2 depicts the structure of one MMC and one SM within the MMC. Each MMC consists of three parallel-connected phase units where each phase unit comprises two arms.

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Each arm is composed of one arm inductor and series-connected, identical half-bridge SMs. The arm inductor is designed to provide current control and limit the circulating current within the arm and to limit fault currents. A SM has three switching states, block (BLK), ON, and OFF. The SM is blocked either in the standby mode or under fault conditions. Under nominal conditions, each SM is either switched ON or OFF. In the ON state, the upper IGBT (S1) is switched on and the lower one (S2) is switched off, the voltage of the SM equals to the capacitor voltage. In the OFF state, S1 is switched off and S2 is switched on, the capacitor is bypassed . At the initial stage before the start-up of the system, the MMC is in standby mode with all SMs being blocked.

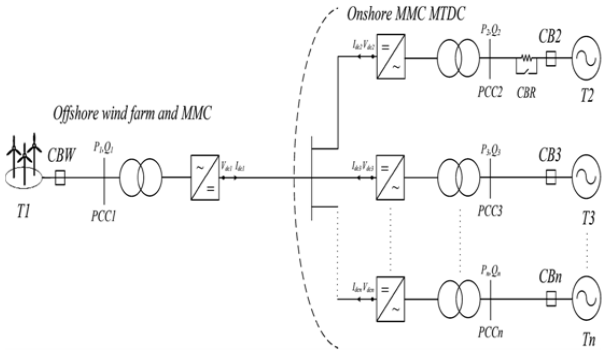

Fig. 5.1. MMC MTDC system with the integration of an OWF.

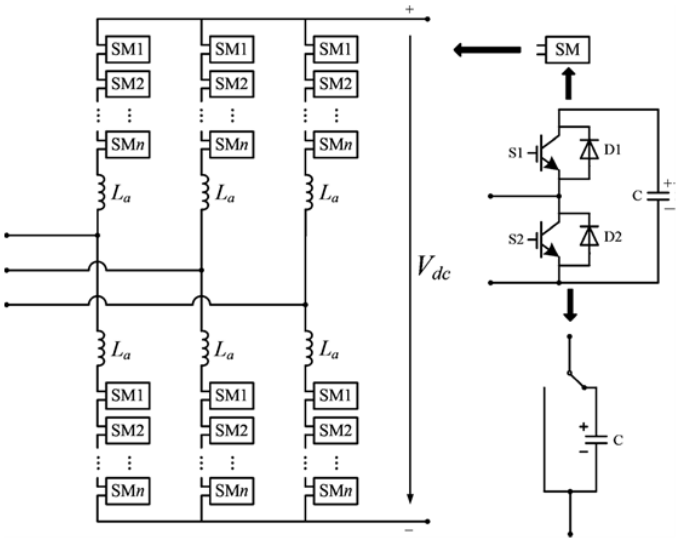

Fig. 5.2. Structure of one MMC and a SM.

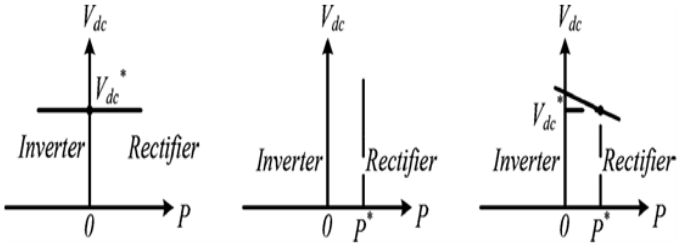

Fig. 5.3. Characteristics of dc voltage versus active power in MTDC. (a) Constant dc voltage control. (b) Constant active power control. (c) Droop control.

CONTROL STRATEGY

The MTDC investigated in this paper is a four-terminal MMC HVDC system. For the offshore terminal, T1, the active power transferred is determined by the control of the DFIG-based OWF.

Hence, MMC-1 applies ac voltage and frequency control to stabilize the voltage magnitude and frequency at PCC1. For the onshore MTDC terminals, the MMCs are connected with active AC networks which can provide stable ac voltage at the PCC and active power to the connected MMC.

The well-known dq decoupled control is applied. For MMC MTDC systems, two main control paradigms, i.e., master–slave control and droop control are generally used.

ISSN No: 2348-4845
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For the master–slave control, one terminal is operated as the master terminal with constant dc voltage control, while the other terminals are operated as slave terminals with constant active power control. For the droop control, active power can be shared among different HVDC terminals.

The characteristics of dc voltage versus active power in an MTDC are illustrated in Figure.5.3. The following analysis on the start-up control will be conducted based on the system with master–slave control in which T2 is operated as the master terminal, while the other three terminals are operated as slave terminals. Reactive power control is applied by T2, T3 and T4 to control the reactive power at 0.

The control strategy of each terminal is shown in Table I. The proposed start-up control will be validated on the system with master-slave control and droop control, respectively, in the case studies. At the initial state, all of the capacitors within the MMCs are not charged and the voltage of the MTDC system is not established. During the period from the initial state to the steady state, in order to realize the start-up of the MTDC with small voltage spikes and current surges, the start-up process is divided into several stages rather than starting all terminals simultaneously.

For T1, the start-up of the OWF necessitates a stable nominal AC voltage at PCC1. The establishment of the AC voltage relies on the inverted control of MMC-1 of the DC voltage. Hence, the start-up of T1 should be initiated after the start-up of T2 with a well-stabilized MTDC voltage.

As for T2, it not only stabilizes the MTDC voltage, but also acts as a dc slack bus to balance the active power of the MTDC system. The active power transferred at T2 should be within its maximum rating.

The control strategy of each terminal is shown in Table I. The proposed start-up control will be validated on the system with master-slave control and droop control, respectively, in the case studies.

At the initial state, all of the capacitors within the MMCs are not charged and the voltage of the MTDC system is not established. During the period from the initial state to the steady state, in order to realize the start-up of the MTDC with small voltage spikes and current surges, the start-up process is divided into several stages rather than starting all terminals simultaneously.

If the active power flow is not well regulated during the start-up period and is significantly over its transfer capability, it may affect the stabilization of the DC voltage controlled at T2 and there will be subsequent impact on the system performance.

In addition, T1 with OWF is a weaker network compared with T3 and T4 with active ac networks. Hence, the coordinated start-up sequence plays a significant role in the start-up of the system and needs to be comprehensively investigated.

MATHEMATICAL MODEL

Before the Deblocking of the MMC

At the initial stage when the wind farm has not been started, the wind farm connected terminal cannot provide stable ac voltage or inertia and is considered as a passive network. Under this condition, the SMs of the wind farm connected MMC can only be charged from the dc side, as the dashed line shown in Fig. 5.4. When the voltage of the MTDC is stabilized by the control of MMC-2, the blocked MMC-1 is also equivalent to a RLC circuit, as shown in Figure.5.8, where Since there are 2n SM capacitors connected in series, each capacitor will be finally charged to V_dc/2n

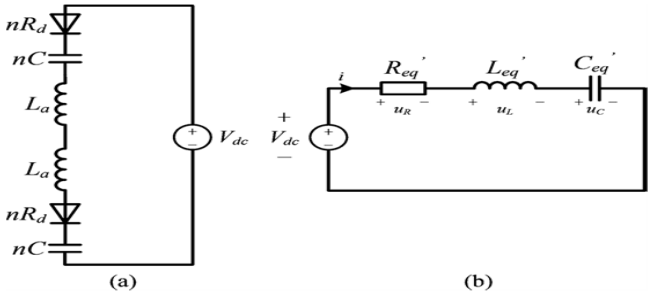

Fig 5.8. Equivalent circuit before the deblocking MMC-1. (a) Equivalent circuit.(b) Simplified circuit.

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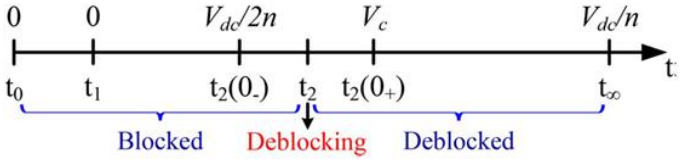


Fig 5.9. Voltage change of a SM from the initial state of the MMC with a passive ac network.

After deblocking of the MMC

The nominal voltage of each SM is 〖V〗_dc/n . The voltage change of a SM from the initial to the steady state is illustrated in Figure.5.9. If the wind farm connected MMC is deblocked directly, there must be a current surge due to the SM voltage difference at the deblocking instant. Therefore, in order to reduce the voltage difference at the deblocking stage, the controlled dc voltage is regulated to a reduced value, which is named as reduced dc voltage control scheme. The SM voltage difference becomes zero when the dc voltage is reduced to half of its rated value. In this paper, the half DC voltage control scheme is applied. Hence, the reference of the dc voltage at T2, after being set at the nominal value, is reduced to V_dc/2n prior to the deblocking of MMC-1.

SIMULATION RESULTS

In order to verify the effectiveness of the proposed scheme, a four-terminal MMC HVDC system with one terminal connected with an OWF is established on the RTDS.

Case A:- In this case, the MTDC is started without starting resistor and without reduced dc voltage control. Simulation results are shown in Fig. 6.1.

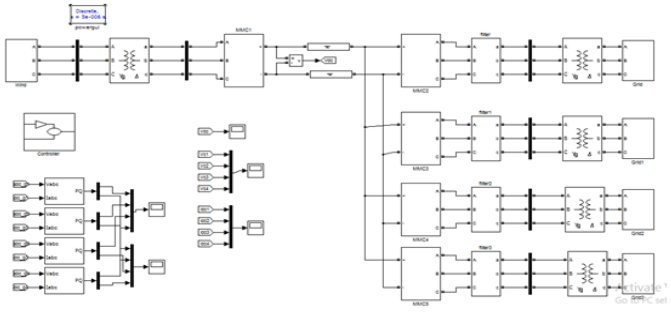
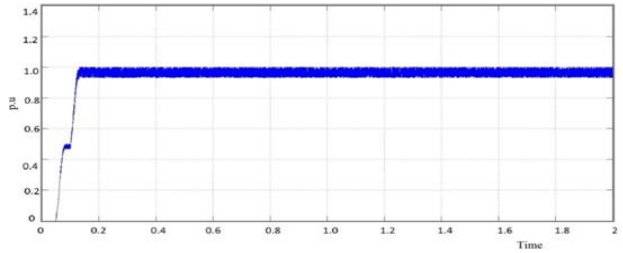
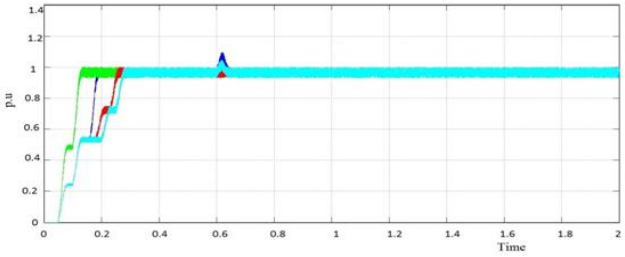


Fig:6.1- MTDC without a starting resistor and without reduced DC voltage control

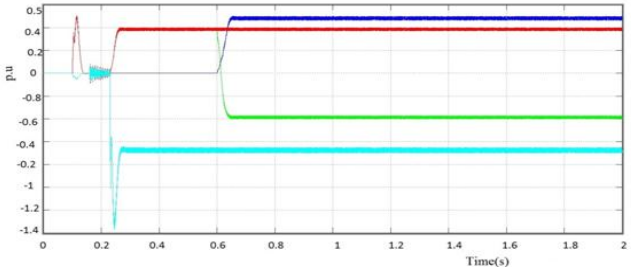
In this case, the MTDC is started without starting resistor and without reduced dc voltage control. Simulation results are shown in Fig. 6.1. Fig. 6.1(a) shows the reference dc voltage 〖(V)〗_dc2ref) and the controlled dc voltage(V_dc2) of MMC-2; Fig. 6.1(b) shows the voltages of the SM capacitors, where 〖CV〗_n (n=1,2…...4) denote the SM capacitor voltage of each MMC; Fig. 6.1(c) shows the dc currents of the MTDC, where I_dcn(n=1,2……4) denote the DC current at each terminal; Fig. 6.1(d) shows the active power of the MTDC, where P_n (n=1,2…..4) denote the active power measured at each terminal; Fig. 6.1(e) shows the reactive power of the MTDC, where Q_n(n=1,2…..4) denote the reactive power measured at each terminal. The measuring points of these quantities are illustrated in Fig. 5.1. Fig. 6.1(c) demonstrates that, due to the absence of starting resistor, the DC current at T2 increases significantly when closing CB2. Since V_dcref is always set atV_dc^* during the start-up process, the voltages



(a)



(b)



(c)

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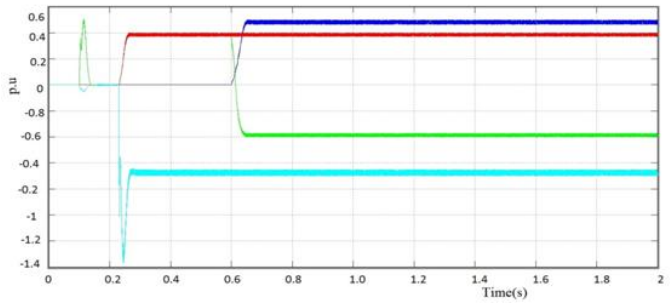
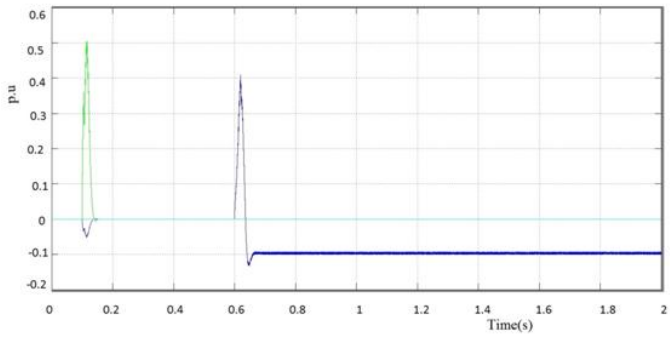


(d)



(e)

Fig6.1MTDC without a starting resistor and without reduced DC voltage control (Case A): (a) MMC-2 DC side voltage, (b) SM capacitor voltages; (c) MTDC currents, (d) active power, and (e) reactive power.

The SM capacitor is not zero between t 〖(0〗 _-) and t(0_+), leading to the step rise of the voltages of the SM capacitors. This will causes large voltage spikes and current surges.

According to Table I, the MMC at each terminal is deblocked at 4 s, 9 s, 12 s, and 13 s, and oscillations of the dc voltage and SM capacitor voltages can be observed in Fig. 6.1(a) and (b). The current surges and power oscillations can be observed at those 4 instants as shown in Fig. 6.1(c) and (d). In addition, since the dc voltage is controlled at V_dc^* at all times, after closing CB3 and CB4, the MMC dc side voltage is much larger than the MMC ac side voltage, leading to the current injection from the MMC DC side to the ac side. According to the current direction and the BLK state of the MMC, this current will charge the SM capacitor, resulting in the voltage rise in the SM capacitor. Table I shows that CB3 and CB4 is closed at t and respectively. Fig. 6.1(b) demonstrates the voltage rise of the SM capacitor in MMC-3 at 10 s and in MMC-4 at 11 s. This also leads to the oscillations on the dc voltage and dc current as shown in Fig. 6.1(a) and (c) at these two instants, as well as the oscillations on the active power as shown in 6.1(d).

CONCLUSION

This project has investigated the start-up control of an OWF integrated MMC MTDC system. After the derivation and analysis of the mathematical models on both the active and passive networks connected MMCs, a hierarchical control scheme for the active network connected MMCs and a reduced dc voltage control scheme for the OWF connected MMC have been proposed. The combination of both schemes forms an overall sequential start-up control scheme. A four-terminal MMC HVDC system with one terminal connected with an OWF has been established on the RTDS. The system with either master-slave control or droop control can be well started using the proposed control scheme with small voltage spikes and current surges. In comparison with the start-up control schemes with/without starting resistor and half dc voltage control, the superiority of the proposed scheme has been observed. This project has also discussed the potential development on the proposed scheme and the importance of the sequential start-up for the MTDC. The proposed sequential start-up control scheme has less complexity and is easy to realize. Although half dc voltage control scheme may not be applicable for every MMC MTDC projects, the reduced dc voltage control scheme can be applied for all of them.

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