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Seven-Level Inverter Integrating Switched Capacitor Techniques

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Abstract

In this paper, a novel cascaded seven-level inverter topology with a single input source integrating switched capacitor techniques is presented. Compared with the traditional cascade multilevel inverter (CMI), the proposed topology replaces all the separate dc sources with capacitors, leaving only one H-bridge cell with a real dc voltage source and only adds two charging switches. The capacitor charging circuit contains only power switches, so that the capacitor charging time is independent of the load. The capacitor voltage can be controlled at a desired level without complex voltage control algorithm and only use the most common carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM) strategy. The operation principle and the charging-discharging characteristic analysis are discussed in detail. A 1kW experimental prototype is built and tested to verify the feasibility and effectiveness of the proposed topology.

Index Terms—Cascaded seven-level inverter, switched capacitor techniques, carrier phase-shifted sinusoidal pulse width modulation, charging and discharging characteristic.

Introduction

In general, multilevel converters are classified into diode-clamped [5], flying capacitor [6], and cascaded multilevel inverter topologies [7]. A particular attention has been given to cascaded multilevel topology because of its modularity, symmetrical structure and simplicity of control. However, the main drawback with the CMI is the large amount of separate isolated sources required to feed each of the H-bridges. It will need n isolated sources for 2n+1 levels of output. Photovoltaic panel, fuel cells, batteries, and ultracapacitors are the most common independent sources. A five-level CMI for distributed energy applications is presented in [8]. The input ports of the CMI are connected to PV modules. However, PV output power depends on weather conditions, such as irradiation and temperature, and it is unavailable at night, which implies that the system cannot work at night. A galvanic isolated charger for the PV port should be installed in the CMI system by connecting to an existing storage unit port.

However, the isolated dc sources in these solutions have to be fed from isolation transformers, which are more expensive and bulky. An alternative option without transformers is to replace all the separate dc sources feeding the H-bridge cells with capacitors, leaving only one H-bridge cell with a real dc voltage source. However, a complex voltage control algorithm is required to keep the capacitor voltage controlled at the desired level. The researchers have proposed various efficient control algorithms. The proposed method in [15]-[16] uses the switching state redundancy for capacitor voltage regulation in

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inductive load. However, the output current of the converter as well as the time duration of the redundant switching states greatly impact the charging and discharging patterns of the replacing capacitors. A simple capacitor voltage regulation constraint is derived which can be used in optimization problems for harmonic minimization or harmonic mitigation to guarantee capacitor voltage regulation in all load condition [17]. A new control method, phase-shift modulation, is used to regulate the voltage of the capacitors replacing the independent dc source. The method is robust and does not incur much computational burden [18]. The proposed dc-voltage-ratio control in [19] is based on a time-domain modulation strategy that avoids the use of inappropriate states to achieve any dc voltage ratio. The following are the three associated problems of this topology: 1) regulating the voltage across the capacitors makes the controller design complex, 2) the charging circuit contains the load. Thus, the charging time and the capacitor voltage are affected by the load variation, and 3) the charging-discharging characteristics and efficiency issues of the capacitor are not fully discussed in the literature.

The efficiency of switched-capacitor in DC-DC converters has been a widely debated issue among researchers [20]-[22]. The equations for the relationship between peak current and circuit's parameters are presented in [23]. With the method, the high pulse current at charging transient can be limited to obtain a higher efficiency. In [24], the efficiency of a RC circuit under different conditions in the charging and discharging operation is analyzed systematically. Based on the analysis, some design rules useful for developing high-efficiency switched-capacitor converters is suggested. Resonant switched capacitor converter using small inductors is also considered as a promising approach to avoid the drawback of the spike current [25].

In this paper, a novel cascaded seven-level inverter topology with a single input source integrating switched capacitor techniques is proposed. The proposed topology consists of a charging circuit and three H-bridge inverter units, as shown in Fig. 1(a). The reliable source port Uin2 can charge capacitor C1 or C3 through the charging switch and H-bridge switches simultaneously and individually.

The charging circuit contains only power switches and capacitors, so that the charging time is independent of the load. The capacitor voltage can be controlled at a desired level with transformerless charging technique and without complex voltage control algorithm.

II. MODULATION STRATEGY

Different multilevel modulation techniques have been presented in the literature. For the CMI, carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM) is the most common strategy [1], with an improved harmonic performance. The CPS-SPWM associates a pair of carriers to each cell of the CMI, and a phase shift among the carriers of the different cells is introduced. In this way, a stepped multilevel waveform is originated. There are some interesting features and advantages: 1) The output voltage has a switching pattern with 2N times the switching frequency (where N is the number of cells). Hence, better total harmonic distortion (THD) is obtained at the output, using 2N times lower frequency carriers. 2) Since all the cells are controlled with the same reference and same carrier frequency, the power is evenly distributed among the cells across the entire modulation index [26]. 3) For the single-supply CMI using capacitors, the advantage is that the capacitors are properly charged without complex voltage balancing control algorithm.

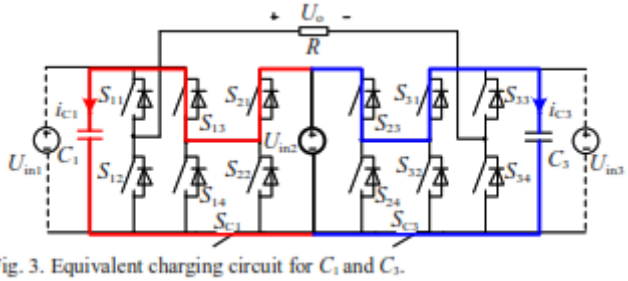

Fig. 3. Equivalent charging circuit for C_1 and C_3.

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The level-shifted SPWM (LS-SPWM) has better output voltage harmonic profile since all the carriers are in phase compared to CPS-PWM. However, this method is not preferred for CMI, since it causes an uneven power distribution among the different cells.

Selective harmonic elimination (SHE) is a low switching frequency (below 1 kHz) PWM method developed to ensure the elimination of undesired low-order harmonics [26]. Space vector modulation (SVM) exhibits features of good dc-link voltage utilization, better fundamental output voltage, better harmonic performance and easier implementation in digital signal processor. However, SVM-based algorithms are not the dominant modulation scheme for n-level (n>5) inverter. The number of the voltage vector is increased to 7^3 in seven-level inverter and the calculation of the duration of the voltage vectors is so complicated.

In this paper, CPS-SPWM is performed to obtain the sinusoidal output voltage in the single-supply cascaded seven-level inverter, and the capacitors are charged by introducing charging-switch pairs every cycle. To some extent, capacitor voltage UC1 and UC3 are regarded as constant, and the three H-bridge inverter cells share balanced power.

Six-way phase-shifted triangular carrier voltages and one-way sinusoidal modulation wave are required for the CPS-SPWM scheme. Z1, Z1, Z2, Z2, Z3, and Z3 are the carrier signals for S11, S13, S21, S23, S31, and S33, respectively and TS is the carrier period.

Substituted for the modulation wave in a carrier cycle, where the carrier frequency is significantly greater than the modulation frequency. The power switches are turned on when the corresponding carrier wave signal is less than the modulation sine wave m. On the contrary, the switches are off when the carrier wave is greater than m. The switches S11/S12, S13/S14, S21/S22, S23/S24, S31/S32, and S33/S34 are operated in a complementary manner. SC1 and SC3 are the charging switches. The gate signal of SC1 can be obtained with S13 and S21 by the AND circuit and that of SC3 can be obtained with S23 and S31 by the same circuit. There are 20 kinds of operating status of each switch, as illustrated in Table I.

And six of them are for the charging process and nine switching status are for the discharging process.

III. CAPACITOR CHARGING AND DISCHARGING CHARACTERISTIC ANALYSIS

A. Capacitor charging state analysis

Through the charging switch and H-bridge switches, C1 and C3 can be charged by the reliable source Uin2. From Status 1, 2 and Status 3 in Table I, we can see that there is only one charging path for C1. In other words, the capacitor charging current iC1 only goes through S21 and S13, as drawn in red color in Fig.3. According to Status 4 to 6, we can see that charging current iC3 flows through S23 and S31. The equivalent charging circuit for C3 is shown in blue color in Fig.3.

B. Capacitor charging time analysis

The capacitor charging time is related to the modulation sine wave value m. For simplicity, the charging time for C1 is taken as an example to have a detailed analysis. When m (0, 2/3), the modulation wave Z1 lags behind Z2 by TS/6, as shown in Fig. 2(a) and 2(b). At this stage, the falling edge of g13 and the rising edge of g21 move forward or backward with the variation in m.

However, the overlapping portions of g13 and g21 remain unchanged; thus, the charging time remains TS/6. The output voltage of the inverter is 0 or Uin2 when m (0, □ 1/3), as illustrated in Fig. 2(a), and Uin2 or 2Uin2 when m (1/3,□ 2/3), as illustrated in Fig. 2(b). When m (2/3, 1), S21 is turned off after S13, as illustrated in Fig. 2(c). The charging time is (1-m)TS/2, and the output voltage of the inverter is 2Uin2 or 3Uin2. And capacitor voltage UC1 would decrease drastically if the modulation wave is increased to 1; however, it would recover in time if the modulation wave is decreased.

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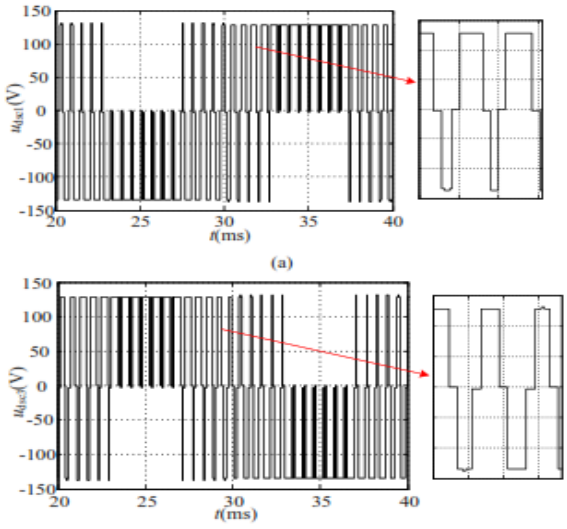
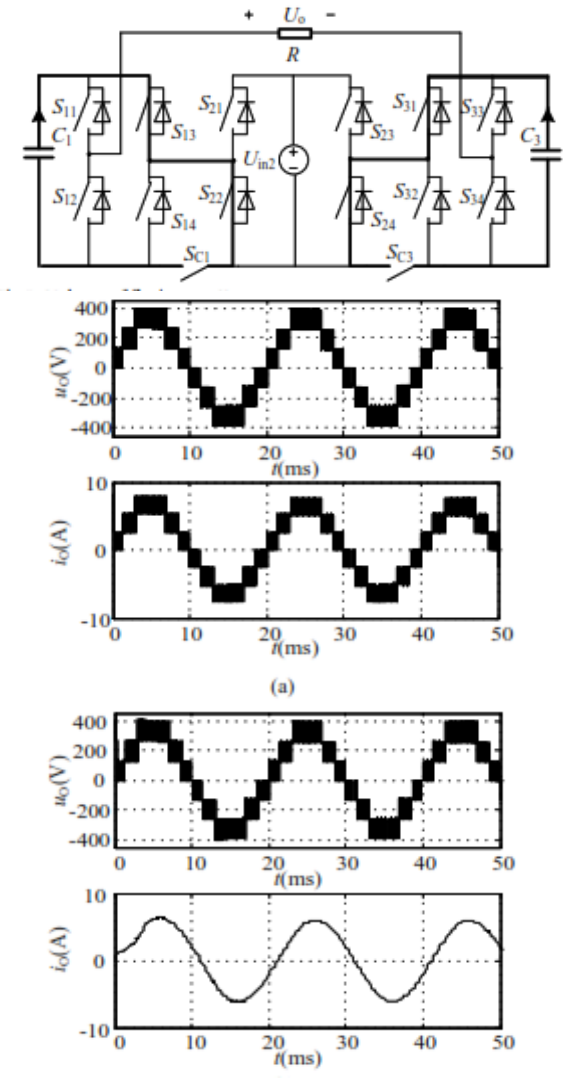


Fig. 11. Voltage waveforms of the charging-switch. (a) S_{C1}. (b) S_{C3}.



Due to the symmetry, the charging time and the output voltage can be easily derived with m < 0. And Table II gives the charging time and the output voltage in different m.

VI. CONCLUSION

A novel single DC source cascaded seven-level inverter integrating switched capacitor techniques is developed in this paper. In the proposed topology, the transformerless charging circuit only contains power switches and capacitors, and the charging time is independent of the load. The operation principle and the charging-discharging characteristic analysis are investigated in depth. With the common CPS-SPWM strategy, the sinusoidal output voltage can be well obtained. Moreover, the capacitors are properly charged without complex voltage balancing control algorithm. The peak charging current and the charging loss can be reduced with appropriate circuit parameters. The proposed topology has the features of modularity, low cost and simplicity of control and makes it attractive in DC-AC power applications. A 1kW experimental prototype verifies the feasibility of the proposed inverter. The proposed inverter is also suitable for photovoltaic-battery multi-input application with high redundancy.

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