ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Monthly Peer Reviewed Open Access International e-Journal

Simulation of Current Source Driver Circuit with PFC for Induction Motor Applications

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Abstract:

Current Source Drivers (CSDs) are investigated for MHz Power Factor Correction (PFC) applications. Due to the fast duty cycle change, the half-bridge (HB) CSD topology can hardly be accepted for high frequency PFC Applications. To solve the problem, the full-bridge (FB) CSD topology is used instead.

It is interesting to note that the FB CSD with the continuous inductor current can actually achieve adaptive drive currents inherently depending on the drain currents in the main power MOSFETs to achieve optimal design. The loss analysis and design procedure are also presented for the FB CSD for the boot PFC converter. To check the performance of induction motor drive connected to proposed converter. The simulation results are obtained using MATLAB/SIMULINK software.

Keywords:

Boost converter, current source driver (CSD), megahertz (MHz) switching frequency, power MOSFET, power factor correction (PFC).

I.INTRODUCTION:

The development of microprocessor and other integrated circuits submits new challenges to power converter. In order to reduce the passive component size, and also to meet the stringent transient response requirement, the switching frequency of the power converter will move into the megahertz range in the next few years. At high-frequency applications, the effect of the gate drive circuit of MOSFETs on the overall performance of the converter becomes quite significant.

As the switching frequency increases, the gate drive loss of the power MOSFET, which is proportional to the switching frequency, increases as well. In addition, as power MOSFET die size is increased to improve the MOSFET on-resistance, the gate-source capacitance of the MOSFET increases proportionally.

Therefore, the gate drive loss becomes more significant, especially in low-voltage, high-current applications. High gate capacitance also increases the switching time and thus the switching loss.

Fig. 1 shows the widely used conventional gate drive scheme, where represents the driven power MOSFET and represents the gate resistor in the driving path. Unfortunately, this conventional gate drive scheme is a voltage source drive approach, and all the drive energy is dissipated on the resistor in the charge and discharge path [1]–[4].

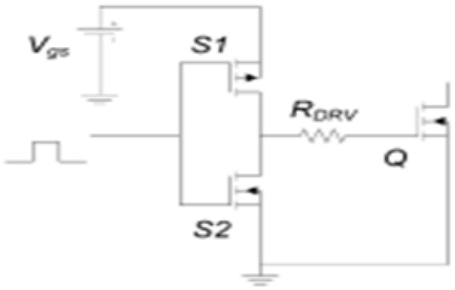

Fig.1 Conventional gate drive scheme

On the other hand, introducing power devices with a low on state voltage/resistance is the only way to reduce the on-state losses. Super junction structures make it possible to decrease the on-state voltage and/or resistance drastically, which has been introduced to MOSFETs and insulated gate bipolar transistors (IGBTs), such as CoolMOS (Infineon), MDmesh (STmicro), CSTBT (Mitsubishi), etc. [7]–[9]. Generally, MOSFETs using a super junction structure have a relatively large input/output capacitance Ciss and Coss, and a large

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reverse recovery charge Qrr in the source-to-drain reverse diode characteristics [10]. Switching losses caused by Coss and Qrr can be minimized by applying the soft switching techniques to the converter circuit. However, the large input capacitance Ciss results in a great increase of the power consumption in the gate-drive circuit especially at a high-frequency operation.

Depending on the current types of the CS inductor, the CSD topologies can be categorized as continuous and discontinuous. A low-side and high-side CSD using a coupled inductor was proposed for a synchronous buck VR in [5] and [6].

To eliminate the coupled inductor, a dual-channel CSD with a continuous CS current using a bootstrap technique was proposed in [7] and [8] to achieve the switching loss reduction and gate energy recovery of the synch FETs.

Its improved version was presented to optimize the performance of the control FET and synch FET independently in [9]. Similar CSD structure is also applied to the interleaving boost converter for PV applications in [10]. In order to reduce the circulating current and the CS inductance value, the CSDs with the discontinuous current and lower inductance were proposed in [11]–[10].

To overcome the current diversion problem, the blocking diode is introduced to the CSDs and the fast switching capability is further improved. However, these CSDs can only provide constant drive current and this may result in lower efficiency when the switching current varies in wide range in PFC applications.

II. ANALYSIS OF CSD CIRCUITS AND THE PROPOSED ADAPTIVE CSD FOR BOOST PFC CONVERTERS:

A. Analysis of the Half-Bridge CSD:

The basic CSD with the continuous inductor current is a half bridge (HB) structure as shown in Fig. 2. It consists of two drives MOSFETsS1andS2.Vc is the drive voltage, Lr is the CS inductor, and Cb is the blocking capacitor. The voltage across the blocking capacitor Cb is vCb=(1–D)•Vc, which varies with the duty cycle.

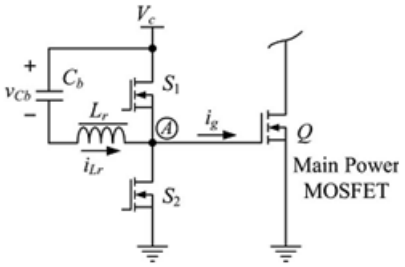

Fig.2. HB CSD topology.

In the boost PFC converter, the duty cycle modulates fast with the input line voltage to shape the input current.

B. Proposed CSD for a Boost PFC Converter:

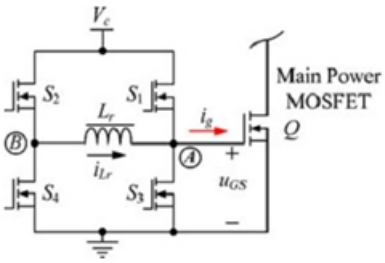

Fig.3. Proposed CSD Solution for PFC applications.

Fig. 3 shows the proposed CSD circuit for the boost PFC converter. Compared to Fig.2, S2 and S4 are used to remove the blocking capacitor Cb, which forms a FB CSD structure.

Since there is no longer any blocking capacitor Cb, the proposed CSD can be suitable for the boost PFC converters with the modulated duty cycle. Fig. 3 shows the key waveforms. Fig. 5 shows the single-phase boost PFC stage with the CSD.

As seen from Fig. 4, S1 and S3, and S2 and S4 are controlled complementarily with dead time. This is similar to the control of the synchronous buck converters, so the commercial-off-shelf buck drivers can be directly used instead of the discrete components in other CSD circuits. This much reduces the complexity of the control circuit and level shift circuits.

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International Journal & Magazine of Engineering, Technology, Management and Research
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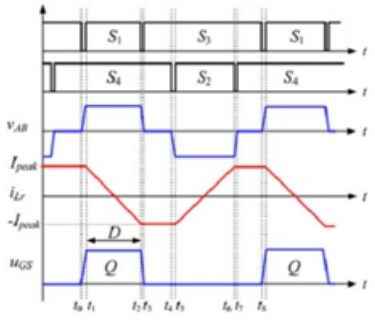

Fig.4. Key waveforms.

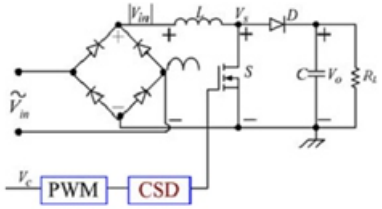

Fig. 5 Proposed CSD solution for the boost PFC converter

C. Principle of Operation:

There are eight switching modes in one switching period. The operation of principle is presented as follows. D1–D4 is the body diodes and C1–C4 is the drain-to-source capacitance of S1–S4, respectively. Cgs is the gate-to-source capacitor of Q.

1) Mode 1 [to,t1] [see Fig. 6]:

Prior to to, S3 is ON and the gate of Q is clamped to ground. At to, S3 turns OFF and the peak value Ipeak of the inductor current iLr charges C3 plus Cgs and discharges C1 simultaneously as a CS. Due to C1 and C3,S3 achieves zero-voltage turnoff. The voltage of C3 rises linearly and the voltage of C1 decays linearly.

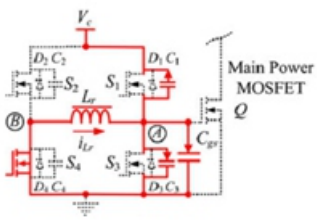

Fig.6. Equivalent circuit of operation in Mode –I [to, t1]

2) Mode2 [t1,t2] [see Fig. 7]:

At t1, the body diode D1conducts and S1turns ON with the zero-voltage condition. The gate-to-source voltage of Q is clamped to Vc throughS1. During this interval, iLr decreases and changes its polarity from Ipeak to -Ipeak..

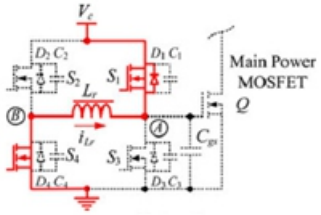

Fig.7. Equivalent circuit of operation in Mode –2 [t1, t2]

3) Mode 3 [t2, t3] [see Fig.8]:

At t2, S1 turns OFF and the negative peak value –Ipeak charges C1 and discharges C3 plus Cgs simultaneously as a CS. Due to C1 and C3, S1 achieves zero-voltage turnoff. The voltage of C1 rises and the voltage of C3 decreases linearly.

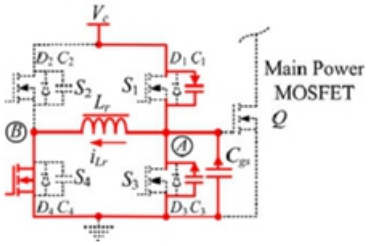

Fig.8. Equivalent circuit of operation in Mode –3 [t2, t3]

4) Mode 4 [t3, t4] [see Fig.9]:

At t3, D3 conducts and S3 turns ON with the zero-voltage condition. The gate to-source voltage of Q is clamped to ground through S3.The current path during this interval is S3–Lr–S4. iLr circulates throughS3and-S4and remains constant in this interval.

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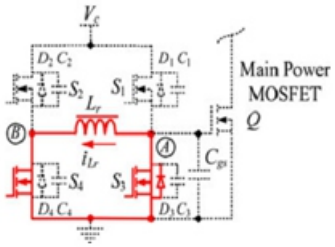

Fig.9. Equivalent circuit of operation in Mode –4 [t3, t4]

5) Mode5 [t4, t5] [see Fig. 10]:

At t4, S4 turns OFF and the negative peak current –Ipeak charges C4and discharges C2 simultaneously. Due to C2 and C4,S4 achieves zero voltage turnoff. The voltage of C4 rises linearly and the voltage of C2 decays linearly.

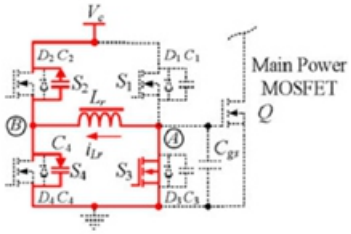

Fig.10. Equivalent circuit of operation in Mode –5 [t4, t5]

6) Mode 6 [t5, t6] [see Fig. 11]:

At t5, D2 conducts and S2 turns ON with the zero-voltage condition. iLr decreases from –Ipeak and changes its polarity to Ipeak.

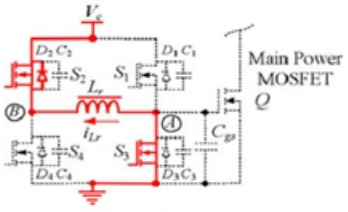

Fig.11. Equivalent circuit of operation in Mode 6 [t5, t6]

7) Mode 7[t6, t7] [see Fig. 12]:

At t6, S2 turns OFF. The peak drive currentI-peakchargesC2 and dischargesC4.The voltage ofC2 rises linearly and the voltage of C4 decays linearly.

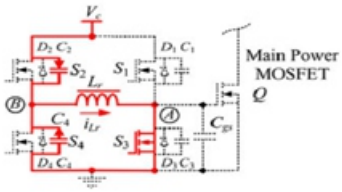

Fig.12. Equivalent circuit of operation in Mode 7[t6, t7]

8) Mode 8 [t7, t8] [see Fig.13]:

At t7, D4 conducts and S4 turns ON with the zero-voltage condition. The current path during this interval isS4–Lr–S3. iLr circulates through S3 andS4and remains constant during this interval.

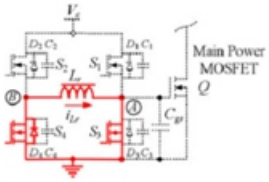

Fig.13. Equivalent circuit of operation in Mode 8 [t7, t8]

D. Adaptive Gate Drive Current of the Power MOSFET:

As seen from Fig. 4, during [t1, t2], the voltage applied to the inductor vAB is the drive voltage Vc. According to the inductance volt-second balance law, the relationship between the inductor value Lr and the peak current Ipeak of the CS inductor is

$$I_{peak} = \frac{V_c \cdot D}{2 \cdot L_r \cdot f_s} \quad D < 0.5 \qquad (1)$$

$$I_{peak} = \frac{V_c \cdot (1-D)}{2 \cdot L_r \cdot f_s} \quad D > 0.5 \qquad (2)$$

For a boost PFC converter with 110 Vac input and 380 V output, the minimum duty cycle is Dmin=1–120 • √2/380 = 0.55.

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When D>0.5, the peak value Ipeak of the inductor current is governed by (2) and is a monotone decreasing function of the duty cycle. Fig. 14 shows the peak current value Ipeak of the CS inductor as the function of the modulated duty cycle during a half-line period. From Fig. 14, as the input current iac in increases following the input voltage vac in, the switching current of the power MOSFET also increase, and the peak value Ipeak of the CS inductor current also increases accordingly, and this leads to a higher driver current, faster switching speed, and thus lower switching loss. On the other hand, as iac in decreases following vac in, the switching current also decreases, which leads to lower circulating loss in the drive circuit? As a conclusion, the peak value Ipeak of the CS inductor (i.e., drive current for the power MOSFET) is able to behave adaptively according to the MOSFET switching current. This property of inherent adaptive drive current of the proposed CSD will benefit the overall efficiency during a wide operation range, without requiring additional auxiliary circuitry and control.

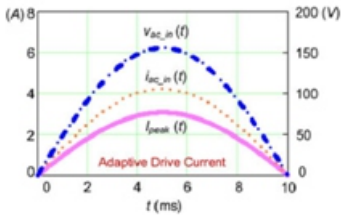

Fig.14 Adaptive drive current with the input line voltage and input current

E. Application Extension:

Moreover, the presented adaptive CSD circuit with one inductor can drive two interleaved boost PFC converters directly as shown in Fig. 15. The advantage is that only single FB CSD is required. It is noted that Q1 and Q2 are turned ON and OFF by the peak current of the CS inductor so that fast switching speed and switching loss reduction can be realized. In addition, S1, S3 and S2, S4 are with complementary control, respectively, and therefore, the commercial buck drivers with two complementary drive signals can be directly used to the CSD circuit. This much reduces the complexity of the CSD circuit implementation with the discrete components. Other benefits of this proposed topology include low current stress of the power MOSFETs, ripple cancellation of input current, and reduced boost inductances.

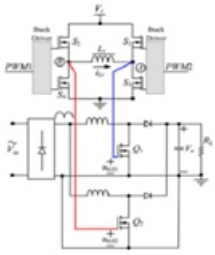

Fig.15 Interleaving boost PFC converters with the proposed adaptive CSD

III. LOSS ANALYSIS OF THE PROPOSED ADAPTIVE CSD FOR A BOOST PFC CONVERTER:

In order to provide the design guideline and optimization, the loss analysis of the proposed adaptive CSD for the boost PFC converter is presented in this section. Basically, the loss of the circuit includes the loss of the PFC power stage and the CSD circuit.

A. Loss Analysis of a Power Stage:

The efficiency of the PFC stage is determined by the losses of the input diode bridge, the boost inductor, the main power MOSFET, and the rectifier diode, and they are analyzed as follows. Because the power MOSFET and boost diode are with a hard switching condition, the switching loss is dominant at high frequency.

1) Loss of the Power MOSFET:

For a single-phase PFC converter, the current waveform of the main power MOSFET is half sinusoidal. The switching loss Psw and conduction loss Pcond are, respectively.

$$P_{sw} = \frac{2\int_0^{\frac{T_{line}}{4}} \frac{1}{2} f_s V_o I_{L\_peak} \sin(\omega_L t)(T_r + T_f)\cdot dt}{T_{line}} + \frac{1}{3} V_o^2 (C_{oss} + C_d) f_s \quad (3)$$

$$P_{cond} = \frac{2\int_0^{\frac{T_{line}}{4}} [I_{L\_peak} \sin(\omega_L t)]^2 R_{ds\_on} D(t)\, dt}{T_{line}} \quad (4)$$

Where ωL=2π.fL, and Tr and Tf are the rising time and the falling time of the MOSFET respectively, ILpeak is the peak current of the boost inductor, Tline is the line period, and fs is the switching frequency. Coss is the MOSFET output capacitance, and Cd is the diode junction capacitance.

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2) Loss of the Boost Diode:

The power losses Pbd of the boost diode including the forward conduction loss and the junction capacitance loss are

$$P_{bd} = \frac{2\int_0^{\frac{T_{line}}{2}} I_{L\_peak}\sin(\omega_L t)\, V_{f\_bd}\,[1-d(t)]\,dt}{T_{line}} + C_{bd}V^2 f_s \quad (5)$$

Where Vf_bd is the forward voltage drop of the diode and Cbd is the junction capacitance of the diode. In the experimental verification, the switching frequency of the boost PFC converter is 1 MHz. In order to minimize the reverse recovery loss, the SiC rectifier CSD06060 from Cree is used. The SiC rectifier has dramatically reduced the reverse recovery charge, so the rectifier's switching loss is not presented in the analysis. However, it should be noted that the diode loss due to the junction capacitance is about 3 W for the CSD06060 at 380 V with 1 MHzswitching frequency.

3) Conduction Loss of the Rectifier Bridge:

The rectifier bridge consists of four rectifier diodes and the conduction loss of the rectifier bridge is

$$P_{rd} = \frac{4}{T_{line}}\int_0^{\frac{T_{line}}{2}} I_{L\_peak}\sin(\omega_L t)\, V_{f\_rd}\, dt \quad (6)$$

Where Vf _rd is the forward voltage drop of the rectifier diodes and IL_peak is the peak current of the boost inductor.

Table I provides the calculated loss breakdown comparison of the 110 Vac input, 380 V output, and 300 W boost PFC converters with 100 kHz and 1 MHz, respectively. The 600 V/11 A CoolMOSTM SPA11N60 from Infineon is used for the power MOSFET and SiC CSD06060 from Cree is used for the diode.

B. Loss Analysis of a CSD:

In order to improve the efficiency, the proposed CSD is employed to reduce the switching loss of the converter. The total power losses of the CSD circuit are listed as follows:

1) The CS inductor loss:

$$P_{copper} = R_{ac}\cdot I_{LRMS}^2 \quad (7)$$

$$P_{ind} = P_{copper} + P_{core} \quad (8)$$

Where ILRMS is the RMS value of the CS inductor current, Rac is the ac resistance of the inductor winding, Pcopper is the copper loss, and Pcore is the core loss;

3)The mesh resistance loss of the power MOSFET:

$$P_{RG} = 2\cdot R_G\cdot I_{peak}^2\cdot t_{sw}\cdot f_s \quad (9)$$

$$t_{sw} = T_{rCSD} + T_{fCSD} \quad (10)$$

Where RG is the internal gate mesh resistance, tsw is the switching time of the power MOSFET, TrCSD and TfCSD are the rising time and the falling time of the power MOSFET, respectively, and Ipeak is the peak value of the CS inductor current;

3) The total conduction loss of S1–S4:

$$P_{cond} = 2\cdot R_{DS(on)}\cdot I_{peak}^2\cdot\frac{4D-1}{3} \quad (11)$$

Where RDS(on)is the on-resistor of the four switches;

4) the total gate drive loss of four switches:

$$P_{gate} = 4\cdot Q_{g\_s}\cdot V_{gs\_s}\cdot f_s \quad (12)$$

Where Qg_s is the total gate charge of switch and Vgss is the drive voltage of the drive switches.

From (8), (9), (11), and (12), the total loss PCSD of the CSD is

IV.MATLAB MODELING AND SIMULATION RESULTS:

$$P_{CSD} = P_{ind} + P_{RG} + P_{cond} + P_{gate} \quad (13)$$

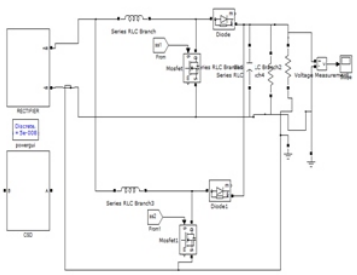

Fig.16 shows the Matlab/simulink model of proposed system

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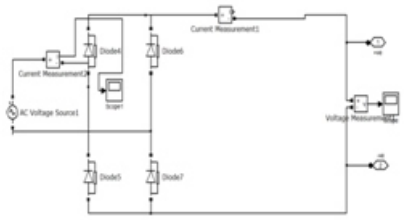

Fig.17 shows the Matlab/simulink model of rectifier.

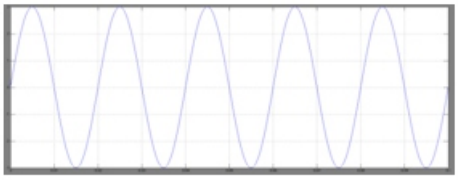

Fig.18 shows the output waveform of inverter input current.

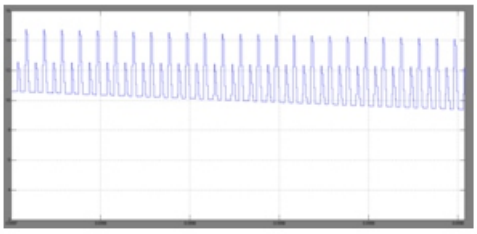

Fig.19 shows the output waveform of inverter output voltage.

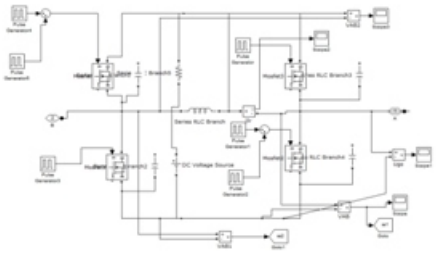

Fig.20 sows the Matlab/simulink model of CSD.

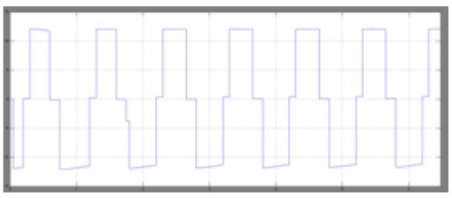

Fig.21 shows the output voltage waveform of inductor.

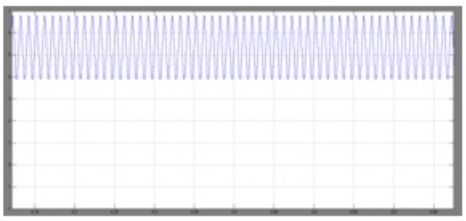

Fig.22 shows the output current waveform of inductor.

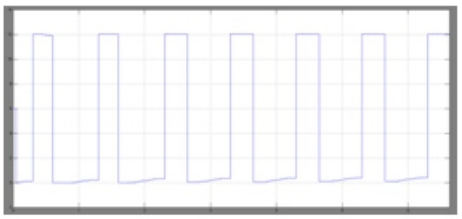

Fig.23 Drive signals of the CSD switches.

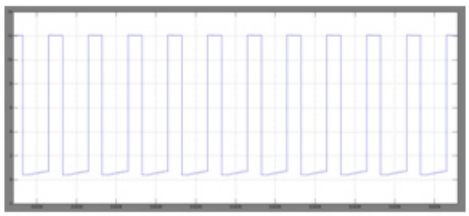

Fig.24 shows the simulated output waveform of gate drive voltage.

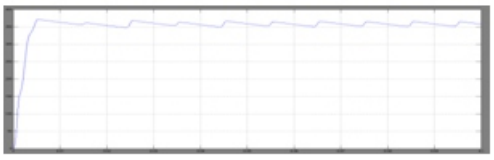

Fig.25 simulated output waveform of output voltage.

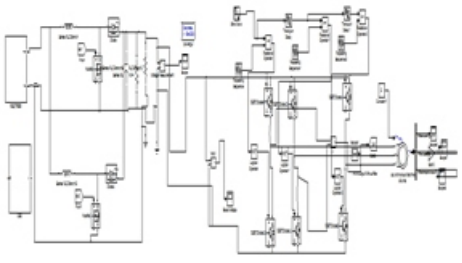

Fig.26 Matlab/simulink model of proposed converter with induction motor drive applications.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Monthly Peer Reviewed Open Access International e-Journal

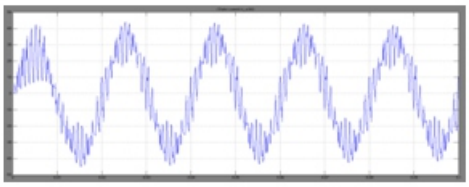

Fig.27 shows the simulated output wave forms of stator current.

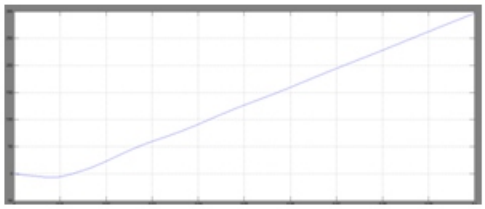

Fig.28 shows the simulated output wave forms of induction motor speed.

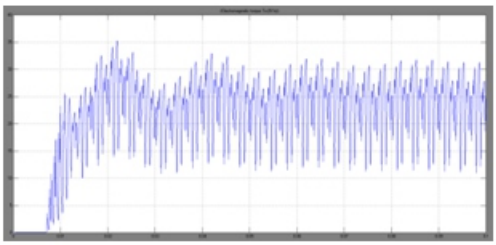

Fig.29 shows the simulated output wave forms of electromagnetic torque of induction motor.

V.CONCLUSION:

In this concept we propose the current source drive system performance with induction motor drive application. An adaptive FB CSD was proposed for boost PFC converters to achieve fast switching speed and significant switching loss reduction.

Compared to other CSDs with the constant drive current, the advantage of the adaptive drive current can achieve further switching loss reduction when the power MOSFET is with a higher witching current while reduce the drive circuit loss when the MOSFET is with a lower switching current. This provides better optimal opportunity with the tradeoff between the switching loss reduction and CSD drive circuit loss during a wide operation range. The simulation results are verified through Matlab/simulink software.

REFERENCES:

[1] H. Fujita, "A resonant gate-drive circuit capable of high-frequency and high-efficiency operation,"IEEE Trans. Power Electron., vol. 25, no. 4, pp. 962–969, Apr. 2010.

[2] B. Wang, A. Monti, and M. Riva, "A high-speed H-bridge circuit based on GaN HFETs and custom resonant gate drivers," inProc. IEEE Energy Convers. Congr. and Expo., Sep. 2009, pp. 973–978.

[3] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault, "New architectures for radio-frequency DC–DC power conversion,"IEEE Trans. Power Electron., vol. 21, no. 2, pp. 380–393, Mar. 2006.

[4] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio frequency power conversion,"IEEE Trans. Power Electron., vol. 22, no. 1, pp. 41–53, Mar. 2007.

[5] K. Yao and F. C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters,"IEEE Trans. Power Electron., vol. 17, no. 2, pp. 180–186, Mar. 2002.

[6] K. Yao and F. C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," IEEE Trans. Power Electron., vol. 17, no. 2, pp.180-186, Mar. 2002.

[7] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching loss,"IEEE Trans. Power Electron., vol. 23, no. 3, pp. 1574–1583, May 2008.

[8] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter,IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1311–1320, Jul. 2007.

[9] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu, and P. C. Sen, "A 1-MHz high efficiency 12 V buck voltage regulator with a new current-source gate driver,"IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2817–2827, Nov. 2008.

[10] Q. Li and P. Wolfs, "The power loss optimization of a current fed ZVS two-inductor boost converter with a resonant transition gate drive,"IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1253–1263, Sep. 2006.