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Simulation and Design of Simplified Single-Phase Multistring five level Inverter Topology for Distributed Energy Resources

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Abstract:

In the micro grid system, the distributed energy resource (DER)-based single-phase inverter is usually adopted. In order to reduce conversion losses, the key is to save costs and size by removing any kind of transformer as well as reducing the power devices. The objective of this letter is to study a novel five-level multistring inverter topology for DERs-based dc/ac conversion system. In this study, a high step-up converter is introduced as a front-end stage to improve the conversion efficiency of conventional boost converters and to stabilize the output dc voltage of various DERs such as photovoltaic and fuel cell modules for use with the simplified multilevel inverter.

The simplified multilevel inverter requires only six active switches instead of the eight required in the conventionalcascadedH-bridge multi-level inverter.Inaddition, two active switches are operated at the line frequency. The studiedmultistring invertertopologyoffersstrongadvantagessuchasimprovedoutput waveforms, smaller filter size, and lower electromagnetic interference and total harmonics distortion. Simulation and experimental results show the effectiveness of the proposed solution.

Index Terms:

DC/AC power conversion, multilevel inverter.

I. INTRODUCTION:

IN LIGHT of public concern about global warming and climate change, much effort has been focused on the development of environmentally friendly distributed energy resources (DERs).

For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic (PV), wind power, microturbines, and fuel cells into the microgrid system has become a critical issue in recent years. In such systems, most DERs usually supply a dc voltage that varies in a wide range according to various load conditions. Thus, a dc/ac power processing interface is required and is compliable with residential, industrial, and utility grid standards.

Various converter topologies have been developed for DERs that demonstrate effective power flow control performance whether in grid-connected or stand-alone operation. Among them, solutions that employ high-frequency transformersormakenouseoftransformersatallhavebeeninvestigatedto reduce size, weight, and expense. For low-medium power applications, international standards allow the use of grid-connected power converters without galvanic isolation, thus allowing so called "transformer less" architectures.

Furthermore, as the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller and less expensive output filters. As a result, various multilevel topologies are usually characterized by a strong reduction in switching voltages across power switches, allowing the reduction of switching power losses and electromagnetic interference (EMI).

A single-phase multistring five-level inverter integrated with an auxiliary circuit was recently proposed for dc/ac power conversion. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics.

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Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the multistring five-level inverter to be approximately 4% less than that of the conventional multistring three-level inverter. In,anovelisolatedsingle-phaseinverter with generalized zero vectors (GZV) modulation scheme was first presented to simplify the configuration. However, this circuit can still only operate in a limited voltage range for practical applications and suffer degradation in the overall efficiency as the duty cycle of the dc-side switch of the front-end conventional boost converter approaches unity. Furthermore, the use of isolated transformer with multiwindings of the GZVbased inverter results in the larger size, weight, and additional expense.

To overcome the aforementioned problem, the objective of this letter is to study a newly constructed transformer lessfive level multistring inverter topology for DERs. In this letter, the aforesaid GZV-based inverter is reduced to a multistring multilevel inverter topology that requires only six active switches instead of the eight required in the conventional cascaded Hbridge (CCHB) multilevel inverter. In addition, among them, two active switches are operated at the line frequency. In order to improve the conversion efficiency of conventional boost converters, a high step-up converter is also introduced as a front-end stage to stabilize the output dc voltage of each DER modules for use with the simplified multilevel.

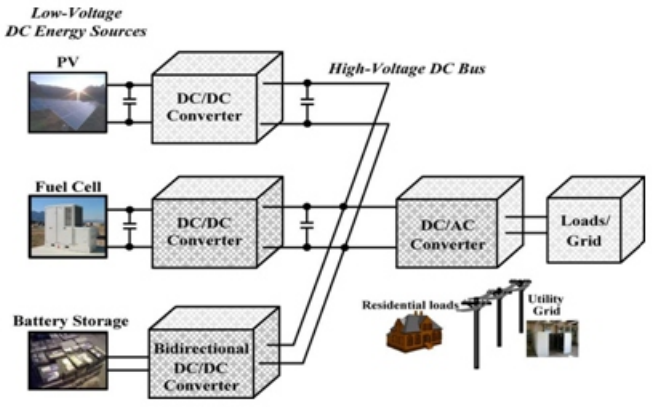

Fig. 1. Configuration of multistring inverter for various DERs application.

Inverter. The newly constructed inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and total harmonics distortion (THD).

In this letter, the operating principle of the developed system is described, and a prototype is constructed for verifying the effectiveness of the topology.

II. SYSTEM CONFIGURATION OF OPERATION PRINCIPLES:

A general overview of different types of PV modules or fuel cell inverters is given. This letter presents a multistring multilevel inverter for DERs application. The multistring inverter shown in Fig. 1 is a further development of the string inverter, whereby several strings are interfaced with their own dc/dc converter to a common inverter. This centralized system is beneficial because each string can be controlled individually. Thus, the operator may start his own PV/fuel cell power plant with a few modules. Further enlargements are easily achieved because a new string with a dc/dc converter can be plugged into the existing platform, enabling a flexible design with high efficiency.

The single-phase multistring multilevel inverter topology used in this study is shown in Fig. 2. This topology configuration consists of two high step-up dc/dc converters connected to their individual dc-bus capacitor and a simplified multilevel inverter. Input sources, DER module 1, and DER module 2 are connected to the inverter followed a linear resistive load through the high step-up dc/dc converters. The studied simplified five-level inverter is used instead of a conventional cascaded pulse width-modulated (PWM) inverter because it offers strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD. It should be noted that, by using the independent voltage regulation control of the individual high step-up converter, voltage balance control for the two bus capacitors C_{bus1}, C_{bus2} can be achieved naturally.

A. High Step-Up Converter Stage:

In this study, high step-up converter topology in is introduced to boost and stabilize the output dc voltage of various DERs such as PV and fuel cell modules for employment of the proposed simplified multilevel inverter. The architecture of a high step-up converter initially introduced from, depicted in Fig. 2, and is composed of different converter topologies: boost, fly back, and a charge-pump circuit.

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The coupled inductor of the high step-up converter in Fig. 2 can be modeled as an ideal transformer, a magnetizing inductor, and a leakage inductor. According to the voltage–seconds balance condition of the magnetizing inductor, the voltage of the primary winding can be derived as

$$v_{\text{pri}} = V_{\text{in}} \cdot \frac{D}{1-D} \qquad (1)$$

Where V_{in} represents each the low-voltage dc energy input sources, and voltage of the secondary winding is

$$v_{\text{sec}} = \frac{N_s}{N_P} \cdot v_{\text{pri}} = \frac{N_s}{N_P} \cdot V_{\text{in}} \cdot \frac{D}{1-D.} \qquad (2)$$

Similar to that of the boost converter, the voltage of the charge pump capacitor C_{pump} and clamp capacitor C_c can be expressed as

$$v_{Cp} = v_{Cc} = V_{\text{in}} \cdot \frac{1}{1-D.} \qquad (3)$$

Hence,the voltage conversion ratio of the high step-up converter, named input voltage to bus voltage ratio, can be derived as [26]

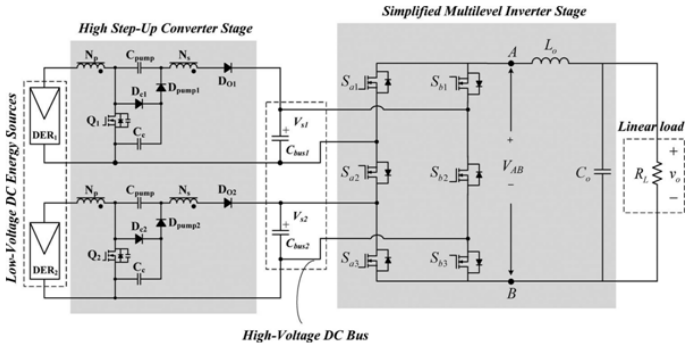
$$\frac{V_{si}}{\text{in}} = \frac{\left(2 + N_s/N_p \cdot D\right)}{V \qquad (1-D)} \Big|_{i} \qquad (4)$$

B. Simplified Multilevel Inverter Stage:

To assist in solving problems caused by cumbersome power stages and complex control circuits for conventional multilevel inverters,thisletterreportsanewsingle-phasemultistringtopology, presented as a new basic circuitry in Fig. 3.

Referring to Fig. 2, it should be assumed that, in this configuration, the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and all switching combinations are activated in an output cycle. The dynamic voltage balance between the two capacitors is automatically controlled by the preceding high step-up converter stage. Then, we can assume $V_{s1} = V_{s2} = V_s$.

This topology includes six power switches—two fewer than the CCHB inverter with eight power switches—which drastically reduces the power circuit complexity and simplifies modulator circuit design and implementation. The phase disposition (PD) PWM control scheme is introduced to generate switching signals and to produce five output-voltage levels: 0, V_s,$2V_s$,$-V_s$, and $-2V_s$.



This inverter topology uses two carrier signals and one reference to generate PWM signals for the switches. The modulation strategy and its implemented logic scheme in Fig. 4(a) and (b) areawidelyusedalternative-forPDmodulation.Withtheexception of an offset value equivalent to the carrier signal amplitude, two comparators are used in this scheme with identical carrier signals V_{tri1} and V_{tri2} to provide high-frequency switching signals for switches S_{a1}, S_{b1}, S_{a3}, and S_{b3}. Another comparator is used for zero-crossing detection to provide line-frequency switching signals for switches S_{a2} and S_{b2}.

Fig. 2.Single-phase multistring five-level inverter topology.

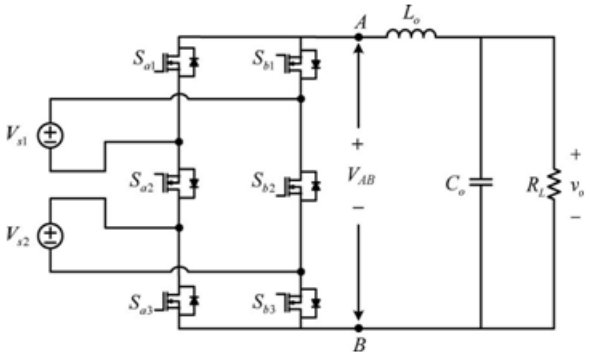


Fig. 3.Basic five-level inverter circuitry.

For convenient illustration, the switching function of the switch in Fig. 3 is defined as follows:

$$S_{aj} = \begin{cases} 1, & S_{aj} \quad \text{ON} \\ 0, & S_{aj} \quad \text{OFF} \end{cases}$$

$$S_{bj} = \begin{cases} 1, & S_{bj} \quad \text{ON} \\ 0, & S_{bj} \quad \text{OFF} \end{cases}$$

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Table I lists switching combinations that generate the required five output levels. The corresponding operation modes of the multilevel inverter stage are described clearly as follows.

1)Maximum positive output, 2VS:

Active switches S_{a2}, S_{b1}, and S_{b3} are ON; the voltage applied to the LC output filter is $2V_S$.

2)Half-level positive output, +Vs:

This output condition can be induced by two different switching combinations. One switching combination is such that active switches S_{a2}, S_{b1}, and S_{a3} are ON; the other is such that active switches Sa2, Sa1, and Sb3 are ON. During this operating stage, the voltage applied to the LC output filter is $+V_s$.

3)Zero output, 0:

This output condition can be formed by either of the two switching structures. Once the left or right switching leg is ON, the load will be short-circuited, and the voltage applied to the load terminals is zero.

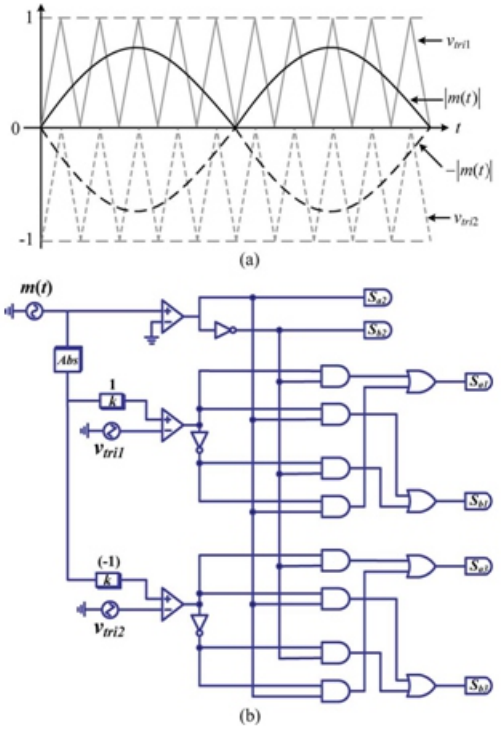

Fig.4.Modulation strategy :(a) carrier/reference signals; (b)modulationlogic.

5)Half-levelnegativeoutput, –Vs:

Thisoutputconditioncan be induced by either of the two different switching combinations. One switching combination is such that active switches S_{a1}, S_{b2}, and S_{b3} are ON; the other is such that active switches S_{a3}, S_{b1}, and S_{b2} are ON.

6)Maximumnegativeoutput, –2Vs:

During this stage, actives witches S_{a1},S_{a3},andS_{b2} areON,and the voltage applied to the LC output filter is $-2V_s$.

TABLE I:SWITCHING COMBINATIONS:

S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	V_{AB}
0	1	0	1	0	1	$2V_S$
0	1	1	1	0	0	V_S
1	1	0	0	0	1	V_S
1	1	1	0	0	0	0
0	0	0	1	1	1	0
1	0	0	0	1	1	$-V_S$
0	0	1	1	1	0	$-V_S$
1	0	1	0	1	0	$-2V_S$

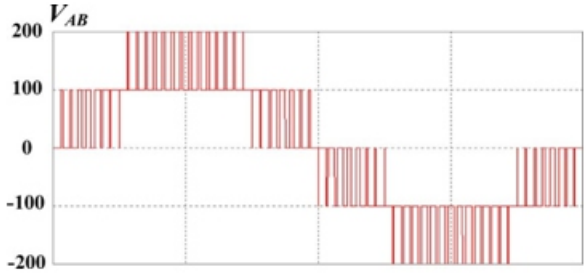

Fig. 5. Simulated waveforms of phase voltage VAB of inverter stage [Scale: 100V/div]

In these operations, it can be observed that the open voltage stress of the active power switches S_{a1}, S_{a3}, S_{b1}, and S_{b3} is equal to input voltage V_s ; moreover, the main active switches S_{a2} andS_{b2} areoperatedattheline-frequency.Hence,theresulting switching losses of the new topology are reduced naturally, and the overall conversion efficiency is improved.

To verify the feasibility of the single-phase five-level inverter, a widely used software program PSIM is applied to simulate the circuit according to the previously mentioned operation principle. The control signal block is shown in Fig. 4; m(t) is the sinusoidal modulation signal. Both V_{tri1} and V_{tri2} are the two triangular carrier signals.

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Thepeakvalueandfrequencyofthesinusoidalmodulation signal are given as mpeak = 0.7 and fm = 60Hz, respectively.

The peak-to-peak value of the triangular modulation signal is equal to 1, and the switching frequency ftri1 and ftri2 are both given as 1.8kHz.

The two input voltage sources feeding from the high stepup converter is controlled at 100V, i.e. $V_{s1} = V_{s2} = 100V$. The simulated waveform of the phase voltage with five levels is shown in Fig. 5.

The switch voltages of S_{a1}, S_{a2}, S_{a3}, S_{b1}, S_{b2}, and S_{b3} are all shown in Fig. 6. It is evident that the voltage stresses of the switches S_{a1}, S_{a3}, S_{b1}, and S_{b3} are all equal to 100V, and only the other two switches S_{a2}, S_{b2} must be 200V voltage stress.

C. Comparison with CCHB Inverter:

The average switching power loss Ps in the switch caused by these transitions can be defined as

$$P_s = 0.5 V_{DS} I_o f_s \left[t_{c(on)} + t_{c(off)}\right] \quad (7)$$

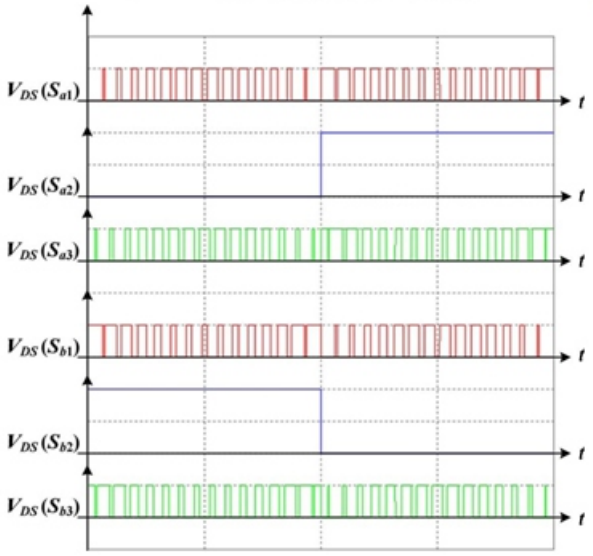

Fig. 6. Simulated waveforms of switch voltage for inverter stage within a line period. [Scale: 100V/div]

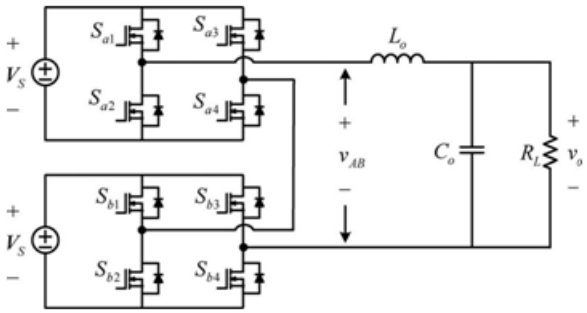

Fig. 7. Five-level inverter topology of CCHB inverter. Wheretc (on) and tc(off) are the turn-on and turn-off crossover intervals, respectively; VDS is the voltage across the switch; and Io is the entire current which flows through the switch.

ComparedwiththeCCHBcircuittopologyasshownin-Fig.7, the voltage stresses of the eight switches of the CCHB inverter are all equal to V_s.

For simplification, both the proposed circuit and CCHB inverter are operated at the same turn-on and turn-off crossover intervals and at the same load Io. Then, the average switching power loss Ps is proportional to VDS and fs as

$$P_s \propto V_{DS} f_s. \quad (8)$$

According to (8)and TableIV,the switching losses of the CCHB inverter from eight switches can be obtained as

$$P_{s,\,H\text{-bridge}} \propto 8 V_s f_s. \quad (9)$$

Similarly, the switching power loss of the proposed singlephase five-level inverter due to six switches can also be obtained as

$$P_{s,\,\text{proposed}} \propto 4 V_s f_s + 2(2V_s) f_m \propto 4V_s (f_s + f_m). \quad (10)$$

Because switches S_{a2}, S_{b2} can only be activated twice in a line period (60Hz) and the switching frequency is larger than the

TABLEII:HARMONICS OF VAB FOR CCHB INVERTER:

h	m_a=0.7	m_a=0.8
Fundamental 1	128.866V	150.984V
3	2.810V	2.780V
5	1.632V	1.604V
7	0.915V	0.981V
9	0.493V	0.573V
11	0.307V	0.301V
%THD V_{AB}	0.433	0.401
%THD v_o	0.020	0.018

Note: m_a is the modulation index; h is the harmonic order.

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TABLE III: HARMONICS OF VAB FOR NEW MULTILEVEL INVERTER:

h	m_a=0.7	m_a=0.8
Fundamental 1	133.491V	155.605V
3	1.193V	1.250V
5	0.400V	0.492V
7	0.029V	0.131V
9	0.193V	0.076V
11	0.278V	0.169V
%THD V_{AB}	0.279	0.169
%THD v_o	0.009	0.008

TABLE IV : COMPARISONS OF TWO MULTI-LEVEL INVERTERS:

Inverter Type	CCHB Inverter	Studied Multilevel Inverter
Switch Numbers	8	6
Voltage Stress	$S_{a1} \sim S_{a4} : V_S$ $S_{b1} \sim S_{b4} : V_S$	$S_{a1}, S_{a3}, S_{b1}, S_{b3} : V_S$ $S_{a2}, S_{b2} : 2V_S$
Switching Loss	$P_{s,H-bridge} \propto 8V_s f_s$	$P_{s,proposed} \propto 4V_s f_s$
NOTES	(1) *CCHB Inverter*: All switches are operated with high frequency. (2) *New Multilevel Inverter*: S_{a2}, S_{b2} are operated under line frequency.	

Line frequency ($f_s \gg f_m$ he switching losses of the proposed circuit is approximated to 4Vsfs.Obviously, the switching power loss is nearly half that of the CCHB inverter.

Considering the harmonics in the inverter output voltage VAB, the amplitude of the fundamental and harmonic components in the output voltage VAB are calculated by PSIM software. The phase-shift PWM technique is adopted for the CCHB Inverter.

Both of the CCHB multilevel inverter and the studied multilevel inverter are operated in the same condition, including the same switching frequency 18kHz, the same modulation index ma, the same input voltage VS = 100V and output LC filter, Lo = 420 µH, Co = 4.7 µF.

Tables II and III show the harmonic components and THD for the CCHB multilevel inverter and the studied-multi-levelinverter,respectively.ItfollowsfromTablesII and III that one can find that the studied multilevel inverter have lower THD than the CCHB multilevel inverter.

It implies that the output waveform is improved and smaller filter size can be used. Finally, for further revealing the potential merits of the studied multistring multilevel inverter, Table IV is provided to summarize comparisons of the switch/diode number, voltage.

TABLE V: COMPONENT PARAMETERS OF THE PROTOTYPE:

High Step DC/DC Converter Stage		
Components	Symbol	Value/Part no.
Coupling inductor	L_m, N_P:N_S	24µH, ETD 39 N_P:N_S = 1.5
Power switches	Q_1, Q_2	FDB3632 (100V, 9mΩ)
Charge-pump diodes	D_{pump1}, D_{pump2}	STPS10AH100 (100V, 10A)
Clamping diodes	D_{c1}, D_{c2}	STPS10AH100 (100V, 10A)
Output diodes	D_{O1}, D_{O2}	15ETH06S (600V, 12A)
Charge-pump caps	C_{pump}	2×4.7µF/630V
Bus capacitors	C_{bus1}, C_{bus2}	2000uF/400V
Simplified Multilevel DC/AC stage		
Power switches	S_{a1}, S_{a2}, S_{a3} S_{b1}, S_{b2}, S_{b3}	FDB2710 (250V, 2.5mΩ)
Output inductor	L_o	1mH
Output capacitor	C_o	4.7µF/630V

Stress, switching losses for the CCHB multilevel inverter, and the simplified single-phase five-level inverter.

III. EXPERIMENTAL RESULTS:

To facilitate understanding of the operating principle and as verification, a prototype system with a high step-up dc/dc converter stage and the simplified multilevel dc/ac stage are built with the corresponding parameters listed in Table V.

The specifications of the two preceding high step-up dc/dc converters are 1) input voltage 30V; 2) controlled output voltage 100V; and 3) switching frequency 85kHz. The corresponding specifications of the simplified multilevel dc/ac inverter stage are 1) output power, Po = 230W; 2) input voltage, Vs = 100V; 3)outputvoltage,vo =110Vrms;4)linefrequency,fm =60Hz; 5) switching frequency, fs = 40kHz; and 6) peak modulation index, mpeak = 0.76.

For better understanding, the guidelines and considerations of the dc-link capacitance and the use of an LC output filter at the output are described as follows.

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A. Sizing DC-link Capacitor:

For the discussed two-stage dc/ac conversion system, the dclink capacitance is sized to keep voltage fluctuations within specified limits to prevent over-voltage on the dc bus. To calculate the relationship between capacitance and voltage limits, the net power flowing into the bus capacitor, i.e., dc-link capacitor, is expressed as

$$P_{bus} = P_{DER} - \frac{V_o I_o}{2}(1 - \cos 2\omega \quad (11)$$

WherePDER is the total output power of the DER modules, and Vo and Io are the peak ac-side quantities.

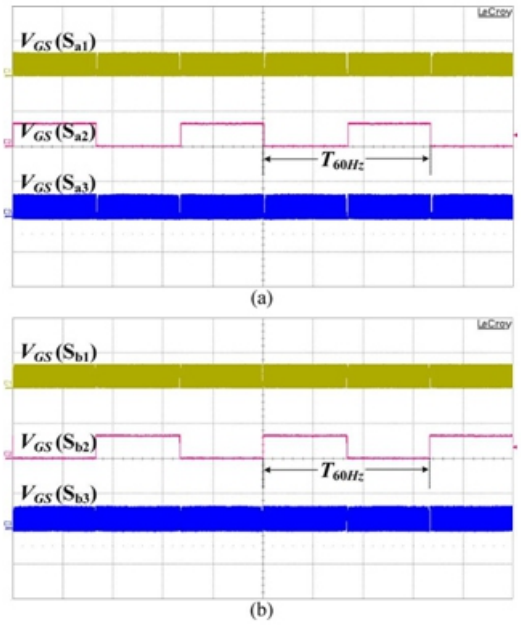

Fig. 8. Measured waveforms of PWM switching signals for inverter stage. [Scale: 10V/div, Time: 5ms/div]

Assuming a steady-state operating condition whereby the net average power flow is zero, the instantaneous power flow into the bus capacitance Cbus is PDER cos2ωt. Integrating this expression provides the energy, and equating the peak change in energy stored in the capacitor with

$$V^2_{bus,min} + \frac{2P_{DER}}{\omega C}$$

$$\Delta E = 0.5C_{bus}(V^2_{bus,max} - V^2_{bus,min}) \text{ yields}$$

$$V_{bus,max} = (12) \text{ bus}$$

Where$V_{bus,max}$ is the peak bus voltage,V_{bus},min istheminimum value of bus voltage, and $C_{bus} = C_{bus1} \times C_{bus2}/(C_{bus1} + C_{bus2})$. The voltage deviation is given by

$$\Delta Vbus = Vbus,max - Vbus,min. \quad (13)$$

For the discussed two-stage conversion system in this study, a design limit of maximum ΔVbus = 10V is chosen to keep the bus voltage well within the voltageratingof the semi conductors, which now is typically 200V, and to minimize the third-order harmonic occurring on the output voltage.

For the aforementioned considerations, thecapacitance C_{bus1} and C_{bus1} are now chosen as 2000 µF, respectively. It should be noted that, for simplification, the bus capacitance for this case is only selected based on voltage deviation specifications.

B. Choice of Output LC Filter:

The output LC filter is tuned to below the switching frequency as follows:

$$\sqrt{L_o C_o} \geq \frac{1}{2\pi f_s} \quad (14)$$

Wherefs is the switching frequency, and Lo and Co are inductance and capacitance of the output LC filter, respectively.

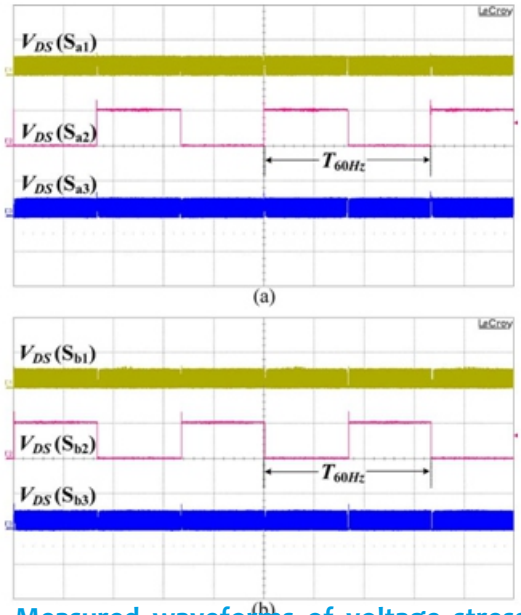

Fig. 9. Measured waveforms of voltage stresses of active switches for inverter stage. [Scale: 200V/div, Time: 5ms/div]

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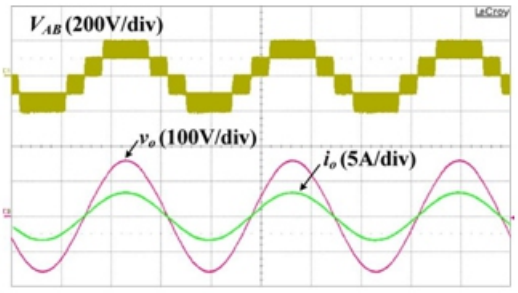

Fig. 10. Measured waveforms of output voltage vo, output current io, and voltage applied to LC filter terminal VAB. [Time: 5ms/div]

The experimental results of the simplified single-phase inverter stage operated at the rated output power are shown in Figs. 8–10.

Figs. 8 and 9 show the PWM signals and voltage stresses of the six power switches for the five-level inverter, respectively.

It is evident that the voltage stresses of the switches S_{a1}, S_{a3}, S_{b1}, and S_{b3} are all equal to 100V, and only the other two switches S_{a2}, S_{b2} must be 200V voltage stress. Fig. 10 shows steadystate waveforms of output voltage vo, output current io, and the voltage applied to LC output filter terminal VAB, respectively, for the inverter with a resistive load of 51 Ω.

As can be seen in Fig. 10, the waveform shows the desired five voltage levels: 200, 100, 0, –100, and –200V. The measured rms value of vo is approximately 110V, while the measured rms value of io is approximately 2.12A. The conversion efficiency of the implemented inverter and THD of the output voltage measured in this case are approximately 96% and 3%, respectively.

IV. CONCLUSION:

This letter reports a newly constructed single-phase multistring multilevel inverter topology that produces a significant reduction in the number of power devices required to implement multilevel output for DERs.

The studied inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD. Simulation and experimental results show the effectiveness of the proposed solution.

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