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Multistage Encoding Methods in Testing Digital VLSI Circuits

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Abstract:

This section shows a multistage encoding method to lessen the test information volume and test control in sweep based test applications. We have proposed a measurable coding procedure called run-length based Huffman coding (RLHC) which is reasonable for multistage encoding to upgrade the test information pressure. This encoding plan together with the nine-coded pressure procedure, called 9C-RLHC upgrade the test information pressure proportion. The proposed multistage pressure likewise indicates huge lessening in normal and pinnacle control in test mode. The decompression design is basic and it requires less territory overhead. Examination of test application time for the proposed multi-arrange pressure is additionally given.

Keywords: RLHC, FSM, MUX.

1. INTRODUCTION:

Factual codes shape the variable-length codeword's for settled length of information squares. Among the accessible factual codes, Huffman code portrayed a decent pressure productivity in light of its most limited normal codeword length. Huffman coding is a measurable information coding strategy that decreases the normal codeword length which speaks to the exceptional example of a set. The proficiency of Huffman code for the most part relies on upon the recurrence of event of all conceivable particular images in the given encoded test set. The short codeword's are allocated to most every now and again happened images and bigger codeword's are appointed to the less oftentimes happened images. The normal codeword length can be minimized along these lines.

Another imperative property of Huffman code is that they give without prefix codeword's, i.e., no codeword is the prefix of another. This disentangles the interpreting prepare. The decoder can momentarily perceive the end of a codeword with no look ahead like in run-length based codes. The settled length input designs limit the abuse of test set elements for pressure. This issue can be understood by the proposed coding plan which permits a productive abuse of test set to accomplish better pressure. The proficiency of Huffman code for the most part relies on upon the recurrence of event of all conceivable unmistakable images in the given encoded test set. The short codeword's are doled out to most regularly happened images and bigger codeword's are doled out to the less much of the time happened images. The normal codeword length can be minimized along these lines.

2. RUN-LENGTH BASED HUFFMAN CODING:

Given a chance to be the test set of the IP center with completely determined bits and the test sets are divided into n unmistakable obstructs each with a length of l. The frequencies (probabilities) of event of n unmistakable squares b1; b2;:::; bn are spoken to as p1; p2;:::; pn separately. The entropy of the test set H(I) indicates the base normal number of bits for each codeword and it can be characterized as minimized. The higher likelihood of event of particular images in the packed test set got from nine-coded pressure method supports the focused on skewing, which can minimize the H(I), and normal codeword length.

$$H|I|\ +-\ \sum_{k=11}^{n} pk\log_2 pk \qquad \textbf{5.2.1}$$

It is assumed that c_1 , c_2 , c_n ...are the codeword length of blocks b_1 b_2 b_n .. respectively. The average codeword length C(I) is

$$|I| = \sum_{k=11}^{n} pk^{C_K} \qquad \textbf{5.2.3}$$

The Huffman code provides closely similar average codeword length of theoretical entropy bound described by Equation 5.2.1. If we skew the occurrence of n distinct blocks in the test sets as much as possible, the entropy value H (I) can be further Minimized.

SYMBOL	PATTERN
L0	1
L1	01
L2	001
L3	0001
L4	0000

Table 1: Representation of Symbols and Patterns for m_h=4

The higher likelihood of event of unmistakable images in the compacted test set acquired from nine-coded pressure system supports the focused on skewing, which can minimize the H(I), and normal codeword length. The arrangement of Huffman tree and Huffman codes are as per the following. Give m_h a chance to be the extent of the gathering. The gathering size speaks to the most extreme adequate number of 0s contained in a keeps running of 0s of length littler than or equivalent to m_h which are alluded as examples. These examples are utilized as contribution to the Huffman coding plan where for every example, the quantity of events are resolved. For gathering sizem_h, there can be most extreme of mh +1 images which is spoken to asL_0, L_1 L_3 …L_{m_h}. and so on. For instance, image and example arrangement with the gathering size m_h= 4 is appeared in Table 1. The Huffman tree is manufactured in view of the examples and the recurrence of events. To build the Huffman tree, the examples are organized in the plummeting request of their events.

At that point the aggregate of the considerable number of events are computed and afterward doled out the foundation of the Huffman tree from which the branches are built. The images which are masterminded in plummeting request, are specifically appointed to the branches which lessen the length of the codeword. The tree development with settled to-variable Huffman and the proposed run-length based Huffman code (RLHC) codes are delineated in Figure 1 (an) and (b) separately. The three test designs with a sum of 48-bits are part into various images and the quantity of events for every image is figured. The Huffman tree is built and all the branches of the tree are set apart with interchange 0_S AND 1_S

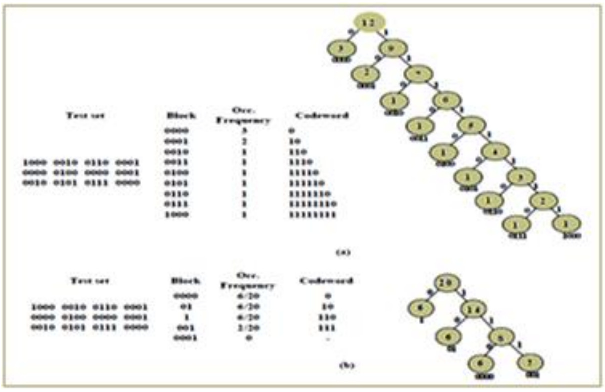

Figure 1: Code formation and its tree construction. (a) Fixed-input Huffman code (b) Run-length based Huffman code

As appeared in Figure 1. The codeword for every example or the image is processed by back following the way along the tree. The branches don't develop both sides of the Huffman tree as portrayed in the ordinary Huffman calculation. We are becoming the branches just in the right sides of tree which brings about shorter codeword for most every now and again happened images and normal codeword. This plan is extremely viable when the quantity of images is constrained. In our RLHC conspire; the most extreme number of images are restricted to mh + 1 for the gathering size of mh. The quantity of images required to develop the Huffman tree are decreased to 5 when contrasted with 9 on account of The tree development with altered to-variable Huffman and the proposed run-length based Huffman code (RLHC) codes are

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shown in Figure 1 (an) and (b) separately. The three test designs with a sum of 48-bits are part into various images and the quantity of events for every image is figured. The Huffman tree is developed and all the branches of the tree are set apart with exchange 1s, Fixed-input Huffman code. As a result, the average codeword length in full Huffman of **(3 × 1) + (2 × 2) + (1 × 3) + (1 × 4) + (1 × 5) + (1 × 6) + (1 × 7) + (1 × 8) + (1 × 8)** =48 bits are reduced to (4 × 1) + (2 × 2) + (1 × 3) + (3 × 3) = 24 bits in the RLHC method. The encoded data is 1111 0 10 110 10 1110 0 010 0 110

1. DECOMPRESSION ARCHITECTURE:

The compacted test information should be decoded utilizing on-chip equipment before being connected to the output chain of the CUT. Figure 5.2 demonstrates the decompression engineering used to decompress the encoded information. It comprises of two limited state machine (FSM) squares, one synchronization obstruct, a counter, a multiplexer (MUX), and the control signals. The decoder works on two tickers - the outside clock ATE CLK and inside clock SOC CLK. The FSM1 speaks to RLHC-FSM and the FSM2 speaks to the 9C-FSM. The FSM1 gets the packed information, DATA IN from the ATE at ATE CLK recurrence. Once the FSM1 identifies the codeword, disentangling starts at the framework clock recurrence (SOC CLK) and the DEC EN is set as 1. At the point when FSM1 deciphers the information, it doesn't get any information from the ATE. The ACK H is set to 1, when the FSM1 decoded the codeword and it is prepared to get the following codeword. The FSM2 get the decoded information from FSM1 at the recurrence of the framework clock. Once FSM2 recognizes the codeword, it will unravel the codeword too. For the codeword's C_1 C_2 C_3 orC_4, the K yield bits contains either 0s or 1s. For codewordsC_5C_6; C_7; C_8 orC_9, either the K=2 or K bits in the yield is relied upon to be gotten specifically from Data in u. A 3 to 1 MUX is utilized to choose 0,1 and Data in u. The two select lines, Sel1 and Sel0 originate from the FSM to the MUX. The counter is utilized to control the exchange of K=2 bits from the yield of MUX to the sweep chain. The number starts when the FSM sends the Cnt en flag and it gets increased when it gets the INC flag.

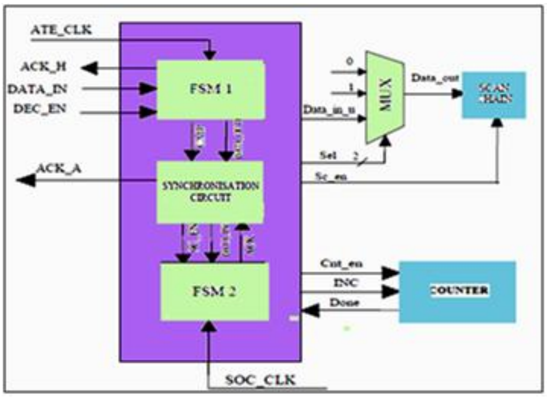

Figure 2: 9C-RLHC encoding: Decompression Architecture

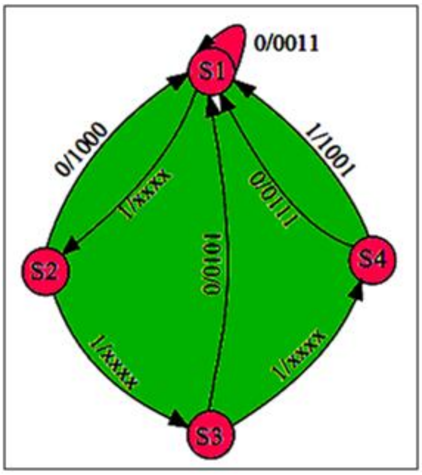

Figure 3: State diagram for RLHC FSM

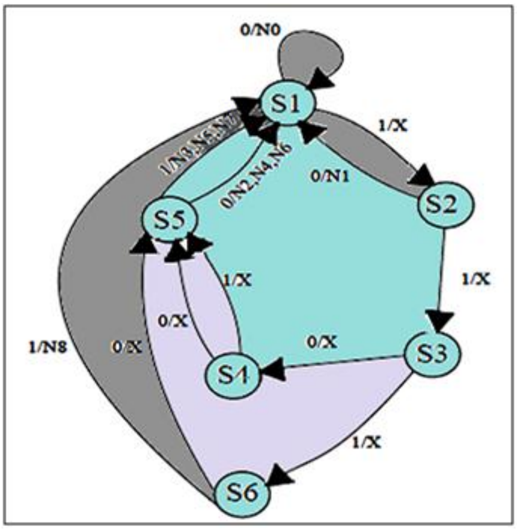

Figure 4: State diagram for 9C FSM

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At the same time, it activates the Sc en signal to enable the scan chain. When the count reaches maximum, the K/2 bits are sent to the scan chain through data out. The counter sends the Done signal to the FSM so as to send the next value to Sel and Cnt _en. After the Done signal is sent for the second time by the counter, the FSM deactivates the Sc en. A synchronization block is used to synchronize both the FSM's.The state diagram used for RLHC decoder with group size m_h = 4 is shown in Figure 5.3. The number of states is equivalent to the total number of branches in the Huffman tree minus one. There are maximum of four states which represent the group size m_h. The FSM starts from state S1, and changes its state based on DATA in bit from ATE. After detecting a codeword, decoding begins at the frequency of system clock and FSM back to its default state i.e. S1 state. For example, when the input data stream to be 01, the decoder changes its state from S1 to S2 and again from S2 to S1 and sets the decoder output to 1000 which indicate the decompressed output 0000. The length of the codeword is equal to the number of ATE clock cycles needed to detect a codeword. This FSM is activated as soon as the DEC EN goes high and it receives input DATA IN.

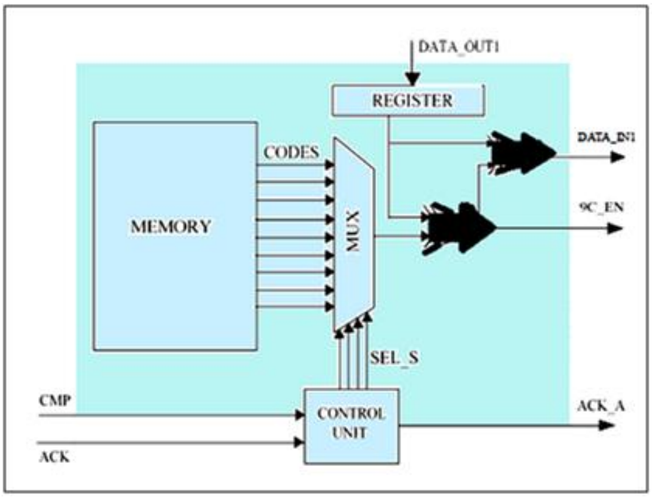


Figure 5: FSM Synchronization circuit

from the ATE. Once the unraveling is done, the CMP flag goes high and the yield Information OUT1, is given to the synchronization piece.

Figure 4 demonstrates the state chart for the 9C decoder FSM utilized as FSM2 which is same as depicted in area 4. Figure 5 is utilized to synchronize the operations amongst FSM1 and FSM2. It comprises of memory, an enlist, a MUX, a control unit and XOR doors. The info information to the enlist is acquired from the FSM1. The control unit does the fundamental controlling of all the components inside the unit. At the point when the CMP flag goes high, the control unit sends select line esteem SEL S to the MUX and the yield of the MUX is then XORed with the yield from the enroll. In the event that the yield of this XOR door is 0, it implies that a 9C codeword is accessible as the yield from the synchronization square which is given as the info DATA IN1 to the FSM2 to be decoded.

4. ANALYIS OF TEST APPLICATION TIME:

We now break down the overall test application time (TAT) when a solitary sweep chain is utilized by the disentangling procedure. One of the primary objectives of any test information pressure technique is to diminish the general test application time notwithstanding lessen the test information volume.

The test application time relies on upon the time required to exchange the encoded test set from the analyzer to the chip and the time required to interpret the encoded information to the output chain. Let the ATE and the on-chip framework are running at various frequencies. It is expected that f_{ATE} and f_{SYS} are the working frequencies of ATE and on-chip framework separately. Additionally, f_{SYS} $=f_{ATE}$ since moderate speed analyzers are utilized to test the fast frameworks. Where $f_{ATE} = f_{SYS} = \phi$, $\phi > 1$. The parameter ϕ is a force of two since it would be simpler to synchronize the analyzer clock and the framework clock. In our plan, the decoder comprises of two-phases. The decoder gets the compacted information from the ATE at a recurrence of f_{ATE}. The RLHC codes and in addition 9C codes are decoded at a recurrence of f_{SYS} The synchronizer is utilized to synchronize the RLHC decoded yield with 9C codeword's.

The proposed decoded plot in this manner decouples the interior sweep chain from the ATE by means of the utilization of a decoder interface. This decoupling infers that the sweep clock recurrence is no longer obliged by the ATE clock recurrence impediment. Therefore, a minimal effort ATE running at a slower recurrence f_{ATE} can be utilized to test a circuit with a higher output test recurrencef_{SYS}. For the proposed conspire, let TAT9C−RLHC be the test application time for the encoded test set. Let Transfer be the time required to exchange the encoded information from ATE to the chip and $T_{decoder}$ be the time required to unravel the encoded test set. In the proposed decoder conspire, $T_{decoder}$ has two sections, TRLHC is the time required to unravel the RLHC encoded test set and T9C be the test time required to decipher the 9C encoded test set. An upper bound on TATE can be gotten by making a skeptical supposition that the disentangling starts after the entire encoded test set is exchanged from the ATE to the chip. This implies that

$$TAT = T_{transfer} + T_{RLHC} + T_{9C} \quad \textbf{4.1}$$

Let $|T_E|$ be the size of encoded test set. Since data is transferred from the ATE to the chip at the tester frequency, the time required to transfer the encoded test set is given by

$$T_{transfer} = |T_E| = f_{ATE}.$$

The time required to decode the encoded test set on-chip in the first stage is equal to $T_{E1} = T_{transfer}$ where T_{E1} is the size of 9C encoded test set. The test application time T_{9C} depends on the frequency of occurrence of each symbol (N_i). The 9C decoder codeword with size $|I_i|$ is entered into FSM at the frequency of $f_{SYS}$and K system clocks are needed for applying K bits into scan chain. The application time for the 9C decoder is given by

$$T_{9C} = \sum_{i=1}^{9} \left\{\frac{k+|I_j|}{f_{SYS}}\right\} . N_i \qquad \textbf{4.2}$$

Let $N=\sum_{i=1}^{9} N_i \; and \; |T_{E1|} = \sum_{i=1}^{9} |I_i| \, |N_i| \qquad \textbf{4.3}$

The time required to decode the data obtained from RLHC decoder is$T_{9C}=\frac{KN+|T_{E2}|}{f_{SYS}}$In our method, both RLHC and 9C decoders are simultaneously decoding the codeword's. Therefore, the overall application time for 9C-RLHC can be given by

$$TAT = \frac{|T_E|}{f_{ATE}} + Max\left\{\frac{|T_{E1|}}{f_{SYS}}, \frac{KN + |T_{E1|}}{f_{SYS}}\right\} \qquad \textbf{4.4}$$

The time required to decode RLHC codes are normally higher than the time required to decode the 9C codes since it output the fixed-length data. So the upper bound on TAT for 9C-RLHC decoder can be

$$TAT = TAT = \frac{|T_E|}{f_{ATE}} + \frac{|T_{E1|}}{f_{SYS}}, \frac{\phi|T_{E|} + |T_{E1|}}{f_{SYS}} \qquad \textbf{4.5}$$

Similarly, we can derive the lower bound on test application time. The lower bound ensures that the ATE never has to wait for the decoder to finish decoding the previous codeword. In other words, the ATE continuously supply the data Entering into its ideal state, to reduce the TAT. The lower bound for 9C-RLHC is limited by the group size, $\mathbf{m_h}$of RLHC scheme. The lower bound on $f_{SYS} = f_{ATE}$ to obtain maximum TAT reduction for 9C-RLHC methods are constrained by $f_{SYS} = f_{ATE}$ K.The overall TAT for the single-stage 9C coding scheme is given by

$$T_{9C} \; \frac{KN + \phi|T_{E2}|}{f_{SYS}} \qquad \textbf{4.6}$$

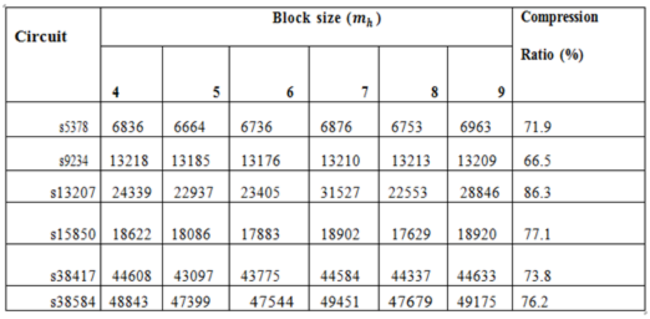
where TE2 is the extent of encoded test set if single-stage pressure is utilized. It can be finished up from Equations 5.4.4 and 5.4.5 that the TAT of our multistage encoding is similar with TAT of single-stage 9C coding, since TE2 > TE1. This diminishment of general TAT is accomplished to the detriment of territory overhead because of synchronization circuit in the decoder.

5.EXPERIMENTAL RESULTS AND ANALYSIS:

Table 2 demonstrates the pressure aftereffects of 9C-RLHC technique for various square sizes of $\mathbf{m_h}$.

The last section demonstrates the best case pressure proportion acquired for every circuit. The 9C-RLHC technique accomplishes a greatest pressure proportion of 85.3% for s13207 circuit. With a specific end goal to demonstrate the adequacy of the proposed 9C-RLHC pressure strategy on lessening of test information volume over different strategies,

Table 2: Compression results for different block sizes in 9C-RLHC technique



Circuit	Block size (m_h)						Compression Ratio (%)
	4	5	6	7	8	9	
s5378	6836	6664	6736	6876	6753	6963	71.9
s9234	13218	13185	13176	13210	13213	13209	66.5
s13207	24339	22937	23405	31527	22553	28846	86.3
s15850	18622	18086	17883	18902	17629	18920	77.1
s38417	44608	43097	43775	44584	44337	44633	73.8
s38584	48843	47399	47544	49451	47679	49175	76.2

6. CONCLUSION:

A multistage encoding plan which misuses the recurrence of event of indistinguishable squares is exhibited. The proposed 9C-RLHC gives better pressure proportion and lesser range overhead. The test application time is likewise decreased as single-stage pressure plot. Exploratory results guarantee that considerable diminishment in test information volume; testing time and test power can be acquired. These methods can be utilized to test SoC with IP centers since the pressure and decompression are plan free. We can expand these plans for multi-filter based installed center by altering the decoder design to improve the test application time. Two multistage encoding plans called 9C-AFDER and 9C-RLHC were proposed to lessen the test data volume and test power. The 9C-AFDER strategy misuses the keeps running of 1s in the main stage pressure and the 9C-RLHC technique abuses the recurrence of event of indistinguishable squares. While both multistage systems upgrade the test data compressions in sweep based test applications, the 9C-RLHC gives better pressure proportion and lesser territory overhead. The test application time is additionally lessened as single-stage pressure conspires.

Exploratory results guarantee that considerable diminishment in test data volume; testing time and test power can be acquired. A strategy which utilize on run-length based coding called exchanging measure up to run-length (AERL) coding to lessen the test data volume and test power consumption is displayed. Another pressure calculation supplanting excess equivalent run-length with shorter codeword and the proposed X-filling strategy builds the quantity of equivalent run-lengths. We have indicated tentatively that the proposed AERL coding method diminishes the test data volume without expanding the pinnacle and normal sweep in test power. Every one of these methods can be utilized to test SoC with IP centers since they require not require the inner structures of the IPs.

7. Future Works:

We can broaden these systems for multi-check based implanted center to upgrade both test data pressure and the test application time. The high rate of X-bit gives a chance to discover filter chain sharing from various centers, so that the relating test sets can be blended and afterward communicated to different chains in parallel testing. By sharing output chain contributions among a few centers it is conceivable to decrease test data volume and abbreviate test application time fundamentally, since centers that share chains are tested simultaneously.

Authors:

- El-Maleh, A. H. (2008b). Test data pressure for framework on-a-chip using developed recurrence coordinated run-length code. IET Comput. what's more, Digital Tech. 2(3), 155–163.
- Li, J., Q. Xu, Y. Hu, and X. Li (2008b). On diminishing both move and catch power for scan-based testing. In Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC, pp. 653–658.
- El-Maleh, A. (2003). A crossover test pressure procedure for effective testing of frameworks on-a-chip. In Proceedings of the IEEE International

Conference on Electronics, Circuits, and Systems, Volume 2, pp. 599–602.

- El-Maleh, A. what's more, R. Al-Abaji (2002). Developed recurrence coordinated run-length code with enhanced application to framework on-a-chip test data pressure. In Electronics, Circuits and Systems, 2002. ninth International Conference on, Volume 2, pp. 449 – 452 Chun, S., Y. J. Kim, J. . Im, and S. Kang (2006). Smaller scale: another half and half test data pressure/decompression conspire. IEEE Trans. Large Scale Integr, (VLSI) Syst. 14(6), 649–654.

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