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Reduction of Power Consumption Using Multi Bit Flip-Flops

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Abstract:

As technology advances, a systems-on-a-chip (SOC) design can contain more and more components that lead to a higher power density. This makes power dissipation reach the limits of what packaging, cooling or other infrastructure can support. Reducing the power consumption not only can enhance battery life but also can avoid the overheating problem, which would increase the difficulty of packaging or cooling. Power has become a burning issue in VLSI design. In modern integrated circuits, the power consumed by clocking gradually takes a dominant part.

Given a design, its power consumption can be reduced by replacing some flip-flops with fewer multi bit flip-flops. However, this procedure may affect the performance of the original circuit. Hence, the flip-flop replacement without timing and placement capacity constraints violation becomes a quite complex problem.

Deal with the difficulty efficiently, several techniques are proposed. In this paper a co-ordinate transformation is performed to identify those flip flops that can be merged and their legal regions.

Besides, building up a combination table to enumerate possible combinations of flip-flops provided by a library is shown. Finally, a hierarchical way to merge flip-flops is used. Besides power reduction, the objective of minimizing the total wire length is also considered. This algorithm significantly reduces clock power and the running time is very short.

Index Terms:

Clock power reduction, merging, multi-bit flip-flop, replacement.

I.INTRODUCTION:

Due to the rapid growth of the chip density and the increasing of clock frequency in the modern high performance designs, power consumption is an important issue in chip manufacturing. A large portion of total power dissipation in synchronous systems is due to the operation of flip-flops in clock network. In conventional synchronous designs, all one-bit flip-flops are considered as independent components. In the recent years, as the process technology advances, feature size of IC is shrank, the minimum size of clock drivers can trigger more than one flip-flop. As a result, merging 1-bit flip-flops into one multi-bit flip-flop by sharing the inverters in the flip-flops can reduce the total clock dynamic power consumption, and the total area contributed by flip-flops.

II.CONVENTIONAL SYSTEM :

A flip-flop is a single bit memory storage element, which is very similar to a latch in that it is a bistable multivibrator, having two states and a feedback path that allows it to store a single bit of information. The difference between a latch and a flip-flop is that a latch is level triggered and the flip-flop is edge triggered. There are several different types of flip-flop each with its own uses and peculiarities.

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The four main types of flip-flop are: SR, JK, D, and T. In conventional type each flip-flop requires a separate clock source which increase the clocking power considerably also the chip area.

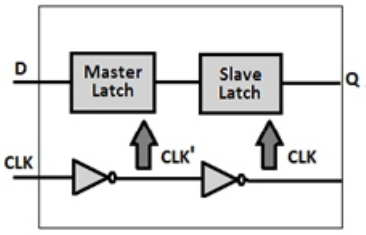

Fig1. Single-Bit Flip-Flop

Fig: 1 shows a single-bit flip-flop, that has two latches (Master latch and slave latch). The latches need "Clk" and "Clk' " signal to perform the operations. In order to have better delay from Clk-> Q, we will regenerate "Clk" from "Clk' ". Hence we will have two inverters in the clock path. In this section we consider a status register with four bit storage.

For this storage we need four 1- bit flip flops with separate four clock signals. Figure 2 shows the output of the 4 bit status register for the input 0100. Table 1 shows the power summary of 4 bit status register with four 1 bit flip flops with separate clock signals for each flip flop. Then for this storage 259m W of power was consumed.

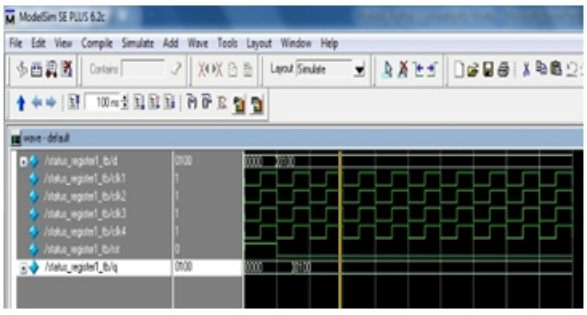

Figure 2: Output of the 4 bit status register with four 1 - bit flip flops.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		259
Vccint 2.50V:	100	250
Vcco33 3.30V:	3	9
Clocks:	86	214
Inputs:	6	15
Logic:	0	0
Outputs:		
Vcco33	1	3
Signals:	0	0
Quiescent Vccint 2.50V:	8	20

Table 1: Power summary of 4 bit register with four 1 - bit flip flops

III.PROPOSED SYSTEM:

In this section, we will introduce multi-bit flip-flop conception. Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplicate inverters, and lower the total clock dynamic power consumption. The total area contributing to flip-flops can be reduced as well. By using multi-bit.

Flip-flop to implement ASIC design, users can enjoy the following benefits:

» Lower power consumption by the clock in sequential banked components.

» Smaller area and delay, due to shared transistors and optimized transistor-level layout.

» Reduced clock skew in sequential gates.

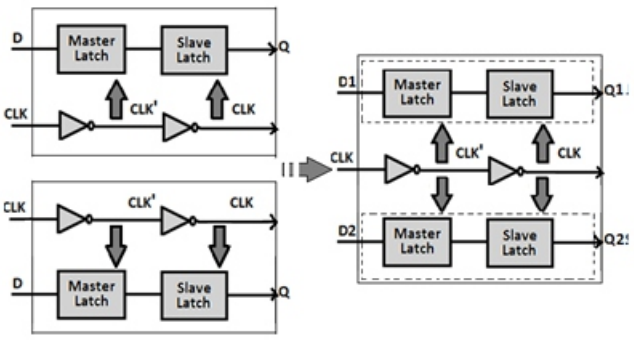

Figure 3: Merging two 1-bit flip-flops into one 2-bit flip-flop

Figure 3 shows an example of merging two 1-bit flip-flops into one 2-bit flip-flop.

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Each 1- bit flip-flop contains two inverters, master-latch and slave-latch.

Figure 4: A dual-bit flip-flop cell.

Figure 4 shows an example of dual-bit flip-flop cell. It has two data input pins, two data output pins, one clock pin and reset pin. Use dual-bit flip-flop can get the benefits of lower power consumption then single-bit, and almost no other additional costs to pay.

CK	D1	Q1	D2	Q2
↑	L	L	L	L
↑	L	L	H	H
↑	H	H	L	L
↑	H	H	H	H
↓	X	D1	X	D2

Figure 5: The true table of dual-bit flip-flop cell.

Figure 5 shows the true table of dual-bit flip-flop cell. We could find that when CK is positive edge, the value of Q1 will pass to D1, and the value of Q2 will pass to D2. Or Q1 and Q2 will keep original value. Multi-bit flip-flop cells are capable of decreasing the power consumption because they have shared inverter inside the flip-flop. Meanwhile, they can minimize clock skew at the same time. In this proposed system we are considering a four bit status register with 3 bit multi bit flip flop and one 1- bit flip flop with two clock signals.

IV.RESULTS & ANALYSIS:

In the conventional system we consider a four bit status register with four 1 bit flip flops with separate clock signals for each flip flop. Then we need four clock signals. Then we have a 259 m W of power consumption.

In our proposed algorithm we consider the same four bit status register three bit multi bit flip flop with one clock signal and separate 1 bit flip flop with another clock signal. In this algorithm totally we are using two clock signals only. Figure 6 shows the output of the 4 bit status register with three bit multi bit flip flop and one separate 1 bit flip flop with two clock signals only. Here we get 0100 output for the input given as 0100. Due to the usage of mergable multi bit flip flops we can reduce the number of clock signals. In this algorithm we can have only two clock signals.

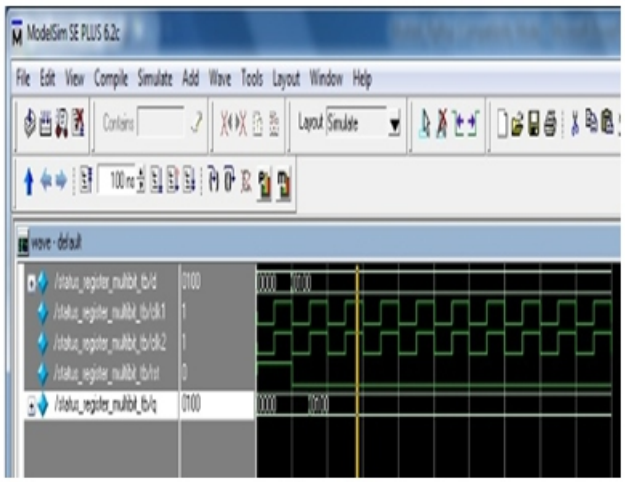

Figure 6: output of the 4 bit status register with three bit multi bit flip flop.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		145
Vccint 2.50V:	54	136
Vcco33 3.30V:	3	9
Clocks:	43	108
Inputs:	3	8
Logic:	0	0
Outputs:		
Vcco33	1	3
Signals:	0	0
Quiescent Vccint 2.50V:	8	20
Quiescent Vcco33 3.30V:	2	7

Table 2: Power summary of the 4 bit status register with three bit multi bit flip flop

Table 2 shows the power summary of 4 bit status register with three bit multi bit flip flop and one 1 bit flip flop with two clock signals only. So by using mergable multi bit flip flops we can have only 145 m W of power consumption.

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From this analysis we can say that we can reduce the power consumption by using mergable Multibit flip flops.

V.CONCLUSION:

Using Multi-Bit Flip-flop is an effective and efficient implementation methodology to reduce the power consumption by merging single-bit flip-flop. In this paper, we have implemented design with XILINX Design Compiler with multi-bit flip-flop. Experimental results indicate that multi-bit flip-flop is very effective and efficient method in lower-power designs. We will use this methodology to implement real ASIC project in the future.

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