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# A low power single phase clock distribution using VLSI technology

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## ABSTRACT:

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodal's 32/33/47/48 prescaler. Since the multimodal's 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S counters can actually be programmed to divide over the whole range of frequencies. However, the P and S zounters are programmed accordingly.

The proposed multiband flexible divider also uses an proved loadable bit-cell for Swallow - counter and consumes a power of 0.96 and 2.2 mW, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

## Keywords:
prescaler, nor gates, multiplexers.

## I.INTRODUCTION:

WIRELESS LAN (WLAN) in the multigigahertz bands, such as Hiper LAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in and consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.

The best published frequency synthesizer at 5 GHz consumes 9.7 mWat 1-V supply, where its complete divider consumes power around 6 mW where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The frequency synthesizer reported in uses a prescaler as the first-stage divider, but the divider consumes Power.

Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage , while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler. The divider also uses an improved low-power loadable bit-cell for the Swallow S counter. The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the voltage-controlled oscillator.

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The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider. The integer-N frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer. It is usually formed by a prescaler, a program counter (P counter) and a swallow counter( S counter). Such a topology can provide a programmable division ratio of N X P + S, where N, P and S are the division ratios of three blocks respectively.

The prescaler provides a dual-modulus of N=N +1. The P counter provides a fixed division ratio according to the requirement of the overall division ratio, while the continuous division ratios from 3 to 2n is achieved through the S counter by periodically reloading the divide-by-2 stages, where n is the number of stages of the S counter. The continuous division ratio is used to select the desired channels. Much research has been focused on the prescaler design for its highest operating frequency .

However, in the modern communication system, there is an increasing demand for multi-standards applications. The requirement for wide band and high resolution operations continue to be the problems. To satisfy these requirements, different reference frequencies, and different arrangement for N, P and S counters are selected for different applications. For example, only the UNII bands are covered. In this paper, a new wideband high resolution programmable frequency divider is proposed.

The wide band and high resolution are obtained by using the all-stage programmable topology in both counters, The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency.

A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit.

The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

## II. LITERATURE SURVEY:

A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider- S.; Levantino, S.; Samori, C.; Lacaita, A.L.-Feb. 2004.

## DESCRIPTION:

The adoption of dynamic dividers in CMOS phase-locked loops for multigigahertz applications allows to reduce the power consumption substantially without impairing the phase noise and the power supply sensitivity of the phase-locked loop (PLL). A 5-GHz frequency synthesizer integrated in a 0.25-µm CMOS technology demonstrates a total power consumption of 13.5 mW. The frequency divider combines the conventional and the extended true-single-phase-clock logics.

The oscillator employs a rail-to-rail topology in order to ensure a proper divider function. This PLL intended for wireless LAN applications can synthesize frequencies between 5.14 and 5.70 GHz in steps of 20 MHz. A low-power 5-GHz CMOS frequency synthesizer for wireless LAN transceivers has been presented. The PLL integrated in a 0.25- m CMOS technology consumes only 13.5 mW, thanks to a dynamic TSPC divider.

This class of dividers is demonstrated to be suitable for multigigahertz synthesizers, since it does not impair the power supply rejection or the phase noise performance. WIRELESS LAN systems in the 5–6-GHz band, such as HiperLAN II and IEEE 802.11a, are recognized as the leading standards for high-rate data transmissions.
Being intended for mobile operations, the radio transceiver has a limited power budget. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the most critical blocks in terms of average current dissipation since it operates extensively for both receiving and transmitting.

The best published integrated synthesizers around 5 GHz suitable for wireless LAN receivers consume up to 25mWin both CMOS and bipolar realizations.

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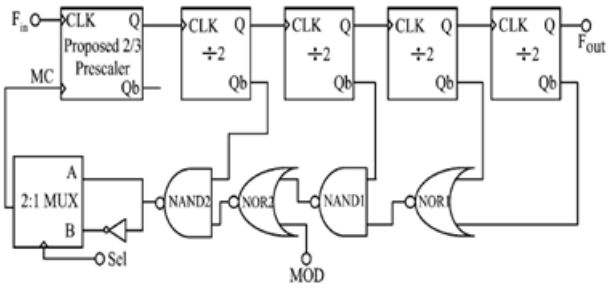
Other synthesizers embedded in 802.11a-compliant transceivers can consume up to 200 mW.The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer.

The integrated synthesizers for WLAN applications at 5 GHz reported in and consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. Frequency synthesizer at 5 GHz consumes 9.7 mW 1-V supply, where its complete divider consumes power around 6 mW where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power.

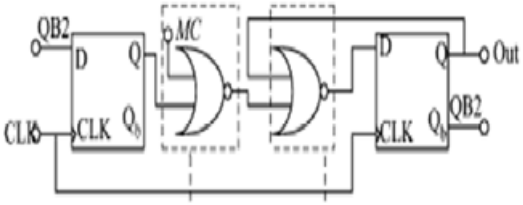



## IV. ROPOSED SYSTEM:

The proposed wideband multimodulusprescaler which can divide the input frequency by 32, 33, 47, and 48 . It is similar to the 32/33 prescaler, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V.

The multimodulusprescaler consists of the wideband 2/3 (N1/(N1+1)) prescale, four aysnchronous TSPC divide-by-2 circuits (AD=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling (N/N+1) divisions, the additional control signal sel is used to switch the prescaler between 32/33 and 47/48 modes.

When MC switches from "0" to "1," transistors M2, M4 and M8 in DFF1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3.




switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2. Where CLi is the load capacitance at the output node of the i th stage of DFF2, and Psc1 and Psc2 are the short-circuit power in the second and third stages of DFF2. When logic signal MC switches from "1" to "0," the logic value at the input of DFF1 is transfered to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1.

Thus, the wideband 2/3 prescaler has benifit of saving more than 50% of power during the divide-by-2 operation. The proposed wideband multimodulusprescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V. The multimodulusprescaler consists of the wideband 2/3 (N1/(N+1))prescaler [10], four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios.

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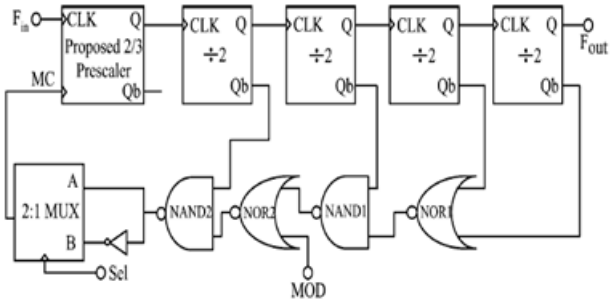
Besidethe usual MOD signal for controlling N(N+1) divisions, the additional control signal Scl is used to switch the prescaler between 32/33 and 47/48 modes.




## PROPOSED MULTIMODULUS 32/33/47/48 PRESCALER:

### Case 1: Sel='0'

When Sel=0 , the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulusprescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC , the 2/3 prescaler operates in the divide-by-3 mode.

If MOD =1, the NAND2 gate output switches to logic "1"(MC=1)and the wideband prescaler operates in the divide- by-2 mode for entire operation. The division ratio N performed by the multimodulusprescaler is

$N = (AD*N1)+(0*(N1+1)) = 32$ …… 4

Where N=2 and AD=16 is fixed for the entire design. If MOD=0 , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N+1 performed by the multimodulusprescaler is

$N + 1 = ((AD - 1)*N1)+(1*(N1+1)) = 33$ …… 5

### Case 2: Sel = 1

When Sel = 1, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulusprescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC = 1, the 2/3 prescaler operates in divide-by-3 mode and when MC=0, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when Sel=0.

If MOD = 1, the division ratio N+1 performed by the multimodulus prescaler is same as except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$N + 1 = ((AD*(N1+1))+(0*N1)) = 48$ …… 6

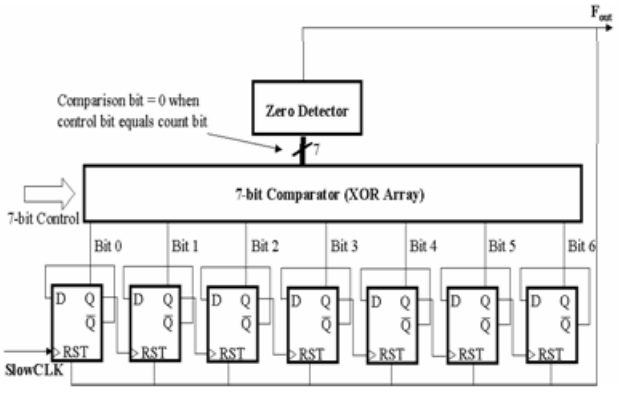
If MOD = 1, the division ratio N performed by the multimodulus prescaler is

$N = ((AD - 1) * (N1+1)) + (1*N1) = 47$

## V. SWALLOW COUNTER:

The swallow counter, as indicated in Figure 8, is used to count S pulses of SlowCLKbefore asserting the modulus control signal and changing the modulus of the DMP to N. A block diagram of the swallow counter is provided in Figure 15. By looking at Figure 15, the similarities between the swallow counter and the program counter are apparent. Once again, the count (6-bits in this case) is maintained using a ripple counter comprised of cascaded flip-flops clocked with SlowCLK. In addition, a comparator compares each count bit with its corresponding bit in the control signal, and a zero-detector asserts modulus control when all bits are equal.

However, the swallow counter does not reset when the count is reached, but masks the input clock using an AND gate connected to the inverse of modulus control. As a result, the ripple counter stops counting when the count is reached, and the state of the circuit is maintained until a reset signal (SwallowRST) is received from the program counter. Since the swallow counter contains 6 bits, it is capable of any count from 0 to 64. Once again, the control signal must be set to S-1, since the zero-state is included in the count.



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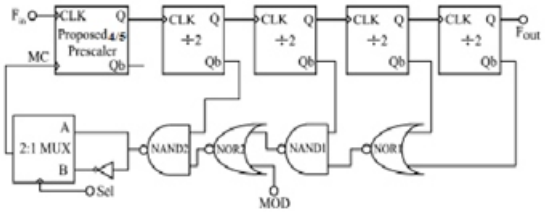
## BLOCK DIAGRAM OF A 6-BIT SWALLOW COUNTER

## S-COUNTER IMPLEMENTATION:

The 6-bit ripple counter implemented as an array of flip-flops, and clocked with the gated clock provided by the AND of SlowCLKand modulus control. In addition, the comparator is implemented as an array

## MULTIPRESCALER_4BY5:




Our proposed multiband flexible divider is Combined by 2/3Prescaler and 4/5 Prescaler in multi modulus Prescaler. By using mux we can operate either 2/3 Prescaler and 4/5 Prescaler. It will operate 2/33/47/48 or 64/65/78/79 bandwidth.

## Simulating with ModelSim

To simulate, first the entity design has to be loaded into the simulator. Do this by selecting fromthe menu:
Simulate > Simulate

A new window will appear listing all the entities (not filenames) that are in the work library. SelectFA entity for simulation and click OK.

Often times it will be necessary to create entities with multiple architectures. In this case the architecture has to be specified for the simulation. Expand the tree for the entity and select the architecture to be simulated and then click OK.

Creating test files for the simulator After the design is loaded, clear up any previous data and restart the timer by typing in the Prompt:

View > Signals
A new window will be displayed listing the design entity's signals and their initial value (shown
below).

Items in waveform and listing are ordered in the same order in which they are declared in the code. To display the waveform, select the signals for the waveform to display (hold CTLand click to select multiple signals) and from the signal list window menu select:
Add > Wave > Selected signals

## VI. SIMULATION IMPLEMENTATION:

Since the early 1980s, when schematic capture was introduced as an efficient way to design very large-scale integration (VLSI) circuits, it has been the design method of choice for designers in the world of VLSI design. However, the use of this method reached its limits in the early 1990s, as more and more logic functionality and features were integrated onto a single chip. Today, most application-specific integrated circuit (ASIC) chips consist of no fewer than one million transistors. Designing circuits this large using the method of schematic capture is time consuming and is no longer efficient. Therefore, a more efficient manner of design was required. This new method had to increase the designers' efficiency and allow ease of design, even when dealing with large circuits. From this requirement arose the wide acceptance of HDL (hardware description language). HDL allows a designer to describe the functionality of a required logic circuit in a language that is easy to understand. The description is then simulated using test benches. After the HDL description is verified for logic functionality, it is synthesized to logic gates by using synthesis tools.

This method helps a designer to design a circuit in a shorter timeframe. The savings in design time is achieved because the designer need not be concerned with the intricate complexities that exist in a particular circuit, but instead is focused on the functionality that is required. This new method of design has been widely adopted today in the field of ASIC design. It allows designers to design large numbers of logic gates to implement logic features and functionality that are required on an ASIC chipAs the size and complexity of digital systems increase, more computer aided design (CAD) tools are introduced into the hardware design process. Early simulation and primitive hardware generation tools have given way to sophisticated design entry, verification, high-level synthesis, formal verification, and automatic hardware generation and device programming tools.

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Growth of design automation tools is largely due to hardware description languages (HDLs) and design methodologies that are based on these languages. Based on HDLs, new digital system CAD tools have been developed and are now widely used by hardware designers. At the same time research for finding better and more abstract hardware languages continues. One of the most widely used HDLs is the Verilog HDL. Because of its wide acceptance in digital design industry, Verilog has become a must-know for design engineers and students in computer-hardware-related fields. This chapter presents tools and environments that are based on Verilog and are available to a hardware designer for automating his or her design process, and hence improving the final product's time to market. We discuss steps involved in taking a hierarchical, high-level design from a Verilog description of the design to its implementation in hardware. Processes and terminologies are illustrated here. We discuss available electronic design automation (EDA) tools that are based on Verilog, and talk about their role in an automated design environment. The last section of this chapter discusses some of the properties of Verilog that make this language a good choice for designers and modelers of hardware.

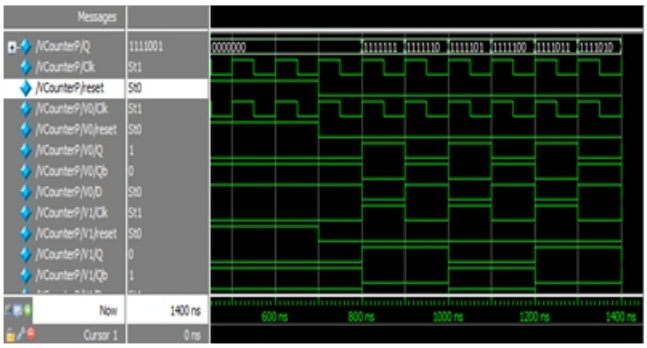

Fig S-COUNTER IMPLEMENTATION

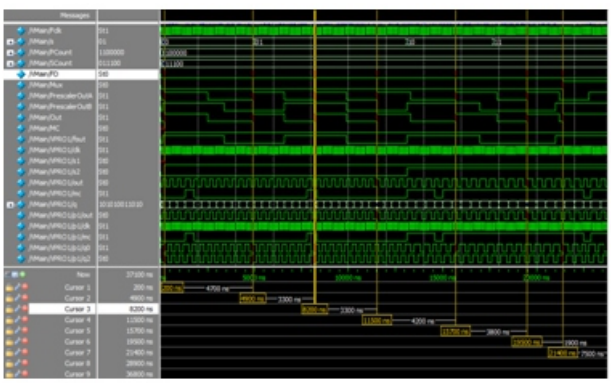

Fig Top module

## VII. CONCLUSION:

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18µm CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

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