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A Low-Power Phase Locked Loop Using Self Healing Pre-Scaler/VCO

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ABSTRACT:

This paper deals with different approaches to design low power Phase Locked Loop (PLL) using self healing Pre-scaler/VCO. The performance of PLL frequency synthesizer is improved by using different Voltage controlled Oscillator (VCO) and their varactor or magnetic tuning scheme. The self healing VCO is implemented in this paper. A 5-stage pre-scaler operating up to 84GHz is presented.

The pre-scaler requirements, design considerations, simulations, and performance measurements are presented. The first divide-by-2 stage consumes 17.7mW at 1.8V, or 26.4fJ power-delay product per gate. The pre-scaler's phase noise gain degeneration at the sensitivity curve boundary is reported for the first time.

It is generally desired to design low Phase noise, wide tuning, low power consumption, high quality factor and independent to Process, Voltage, and Temperature (PVT) variation. However, here various improvements in technology from µm to nm, supply voltage from 0.7 to 1.8V, frequency generated from 2 to 78 GHz and tuning range from 10 to 23% are discussed.

I.INTRODUCTION:

The CMOS –technology approaches to a nanometer scale, the non-idealities such as variability and leakage current may significantly affect the circuit performance. The process variability leads to the large variations to degrade the device matching and performances. It may result in only a few design a wafer to meet the target performance specifications.

The undesired leakage currents also degrade the accuracy and resolution of analog circuits and make digital dynamic circuits not to work properly. For a PMOS transistor with W/L=8Um in 65-nm process, its source and gate are connected to the supply voltage of12v. The drain current leakage current is 68.7na, 0.12ua and 21ua for the typical slow-slow and fast corners respectively and 40c.The leakage current is highly dependent upon the process variation. The current under different corners and temperatures' with a constant VSD=1.22v the leakage current grows very fast in a high temperature environment.

A phase locked loop (PLL) is widely employed in wire -line and wire-less communication systems .The poor device matching and leakage current vary the common mode voltage of a ring-based voltage-controlled oscillator. It may limit the oscillation frequency range of a VCO and causes a VCO not to oscillator in a worst case. the leakage current and leakage mismatch charge will be degrade the reference spur and jitter significantly. To mitigate the above problems a self healing divided by pre-scalar and a self healing VCO are presented.

II.CIRCUIT DESCRIPTION:

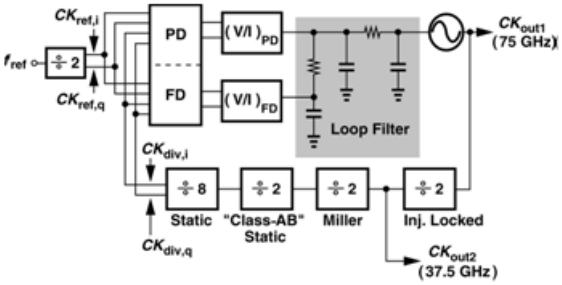

Fig1 PLL Architecture

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The PLL circuit consists of a differential VCO, a divider chain with total modulus of 64, a phase and frequency detector, and a third-order loop filter.

The phase locking and frequency acquisition loops are decomposed to achieve low jitter and wide operation range simultaneously. The phase and frequency detector is implemented with SSB mixers and low-pass filters to suppress the reference feed through.

An extra divider-by-2 circuit is incorporated to provide quadrature reference inputs. Similar to that in [3], the frequency detector along with its V/I converter are automatically turned off upon lock to minimize the disturbance to the VCO.

The loop filter is realized on chip to minimize the noise coupling through bonding wires. The 9-layer interconnect metals in 90-nm process provide high density fringe capacitor2 [4], making the loop filter occupy only m .

To accommodate the severe tradeoffs between the input frequency and operation range, different types of dividers need To be employed here. Generally speaking, the injection-locked dividers [5] achieve the highest operation frequency due to the narrowest locking the simplest structure, but usually with Divider arrangement.

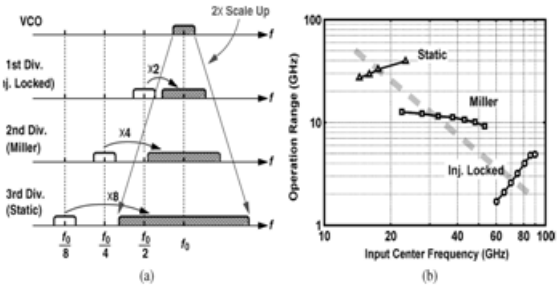

Fig2. (a) Locking range normalization with presumed 2 scale-up requirement. (b) Simulated locking ranges for each divider.

III.PROPOSED ARCHITECTURE:

IN THAT MOSTLY composed of a 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler. The division Ratio is from 4 to 131. The parameters of this PLL are listed in

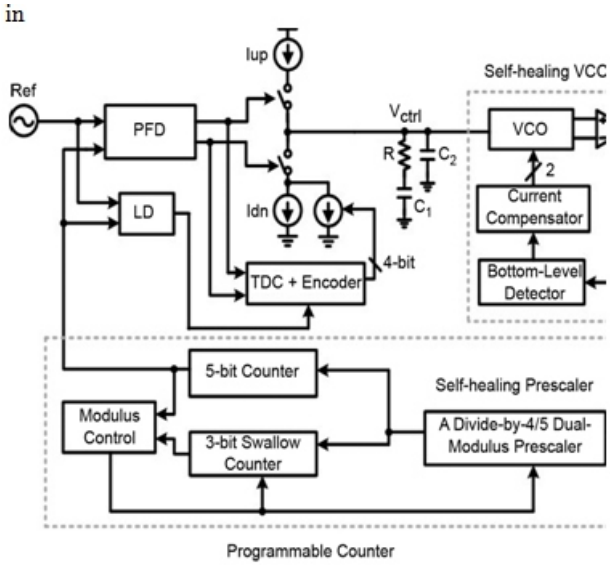

Fig3. Proposed PLL architecture.

Since the phase error of a PLL is highly dependent upon the current mismatch of a CP. The static phase error of a PFD is given as
Δ=Δicp.ton/icp

VCO gain	K_{VCO}	1.5GHz/V
Reference frequency	f_{ref}	15MHz
Charge pump current	I_P	200uA
Passive components	R	180Ohm
	C_1	16.4nF
	C_2	1.3nF

Where is ICP the current IUP &IDN, TON difference between the pull-up and Pull-down currents, and, is the turn-on time of a PFD, ICP is the averaging current of the pull-up and pull-down currents. When this PLL locks, the LD is enabled to turn on the TDC and an encoder.

a. 4-Bit Controller in PLL:

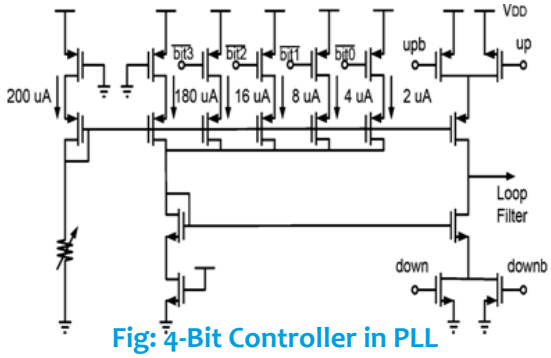

Fig: 4-Bit Controller in PLL

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A 4-bit TDC digitizes this static phase Error to reflect the amount of the current mismatching. Then, the digital code of this TDC is used to calibrate the charge pump. The simulated power of this TDC is 0.24 mW. Its timing resolution is 0.3 ns and the dynamic range is 4.8 ns. A 4-bit digitally-controlled CP is shown in fig4. The up current has a nominal value of 200A and the down current digitally controlled within 180 and 210 A.

The minimum current step is chosen as 2 A to relieve the worst-case current mismatch to 1% in this digitally-controlled CP. The traditional replica-biased CP needs an operational amplifier which needs a High gain and its stability must be concerned. In addition, this operational amplifier may consume a static power. The CP calibration can be finished quickly due to this digital calibration. Once the calibration is completed, the digital code is fixed and the TDC is power-downed to save a power.

b.Self-healing system:

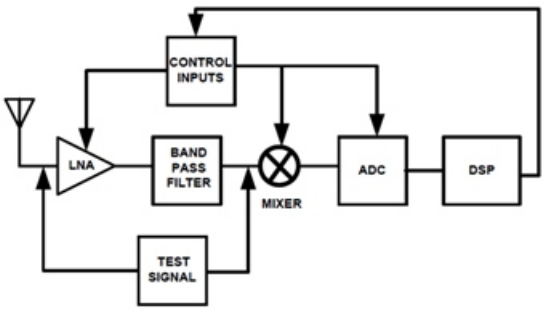


Fig5 self -Healing System.

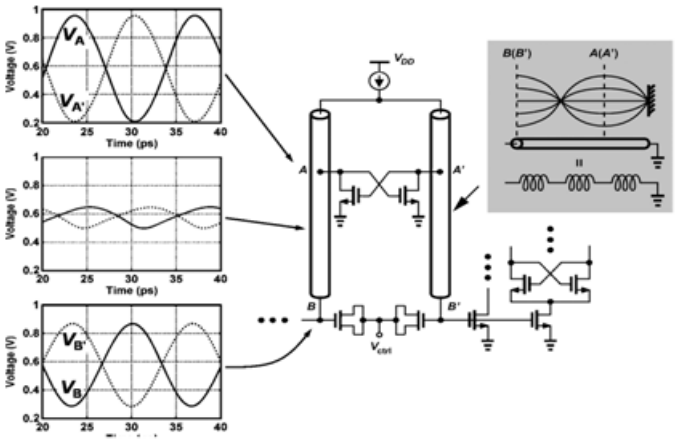
Healing goes beyond simple BIST by adding a layer of hardware and software intelligence to the system that enables autonomous calibration. The present work seeks to show case two wideband test signal source for on-die self healing of an 8-18 GHz (X to Ku band) receiver chain intended for use in radar applications.

In order to exhibit healing, the second test signal source is integrated on die with a 6-20 GHz image-reject mixer. Automated IRR healing is performed on die as a demonstration of local block-level self-healing. VCO of whether the oscillating "tube" is indeed a transmission line.4 Fig. 4(a) introduces a typical high-speed VCO design with a simple buffer, an injection locked divider and a MOS varactor.

The circuit oscillates at a frequency such that the corresponding wavelength is 4 times as large as the equivalent length, leaving the ends (node and) as maximum swings.

However, as the resonance Frequency increases, the loading of the varactors, the buffers, and the dividers becomes significant as compared with that of the cross-coupled pair itself. These indispensable capacitances burden the VCO substantially.

Note that none of these devices can be made arbitrarily small: pair must provide sufficient negative resistance; transistor needs to inject large signal current, and has to provide enough frequency tuning. With the device dimension listed in Fig. 4(a), the circuit oscillates at only 46 GHz. Note that the device sizes have approached the required minimum and further shrinking may cause significant swing degradation.



c.Vector First Stage:

The first two stages the frequency is brought down to below 20GHZ, allowing static implementation on the sub sequent dividers, to extend the band width without using inductors we realize the 3-dividers stage as class-AB structure.

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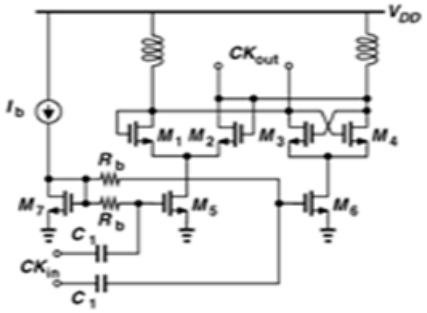
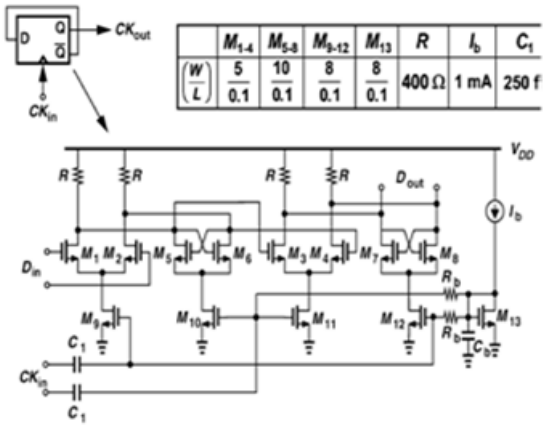
The large in stantaneous currents crease high gain in the signal path and therefore high speed. Beyond this point the divider design becomes much more relaxed. The succeeding stages are implemented as stand static dividers with the power and bandwidth optimized.

	$M_{1,2}$	$M_{3,4}$	$M_{5\text{-}6}$	M_7	I_b	C_1
$\left(\frac{W}{L}\right)$	8/0.1	16/0.1	8/0.1	8/0.1	1.6 mA	200 fF



(a)

	$M_{1\text{-}4}$	$M_{5\text{-}8}$	$M_{9\text{-}12}$	M_{13}	R	I_b	C_1
$\left(\frac{W}{L}\right)$	5/0.1	10/0.1	8/0.1	8/0.1	400 Ω	1 mA	250 f

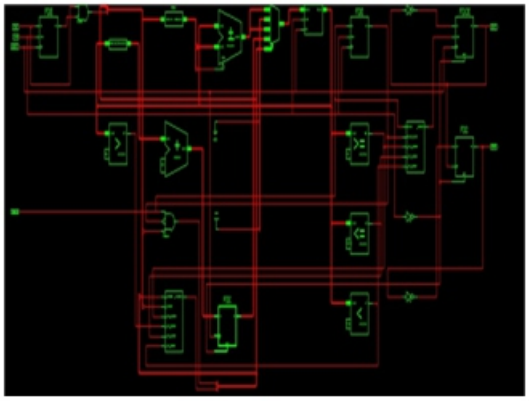


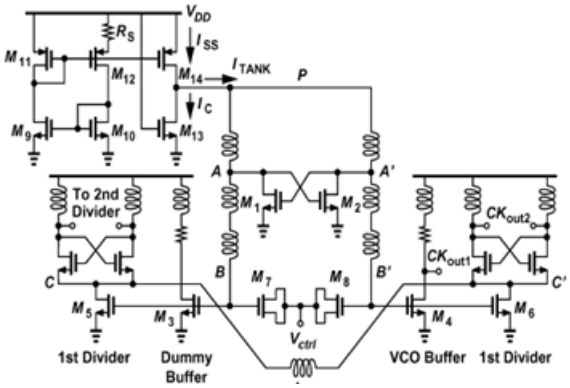
(b)

Fig (a) Second Stage (b) Third Divider Stage

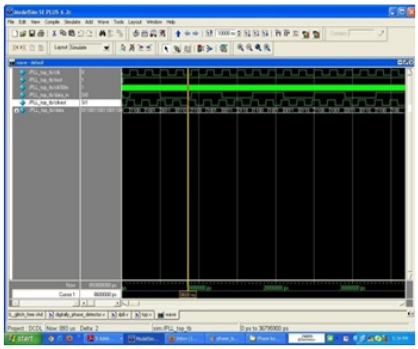
Δ win represents the frequency difference between ck ref and ck div. obviously wither V1 is leading in log in v2 depends on the sign of win, and it can be easily obtained by using a flip-flop output.

the VI converter designed to the frequency detection loop. Injects positive or negative current to the loop filter. This current is 3-times larger than the peak current of (V/I) PD to ensure a smooth frequency acquisition.

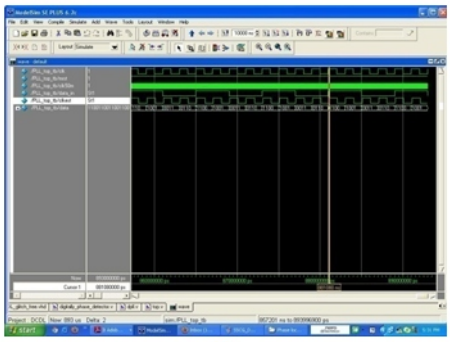




IV.SIMMULATION AND SYNTHESIS:



(a)



(b)

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The Figures are measured through the jitter at 855mhz (A) without and (B) with the self healing rescaler/vco and tdc/encoder to avoid the mal functionδv1 leakage show be lower the vthrosld voltage vthrosld or the subsequent stage asΔvleakage<threshold. The lowest clock frequency of this "TSPCDEF" is Fclock, low≥Ileakage/2. ctot.vthreshol. For example Ileakage~400na at25c ctotal~15fF, and v threshold=0.6v the calculated lowest frequency is 2202MHz that the leakage current is proportional to the temperature. When the temperature increases the lowest frequency is also increases.

The highest frequency of the Tspc is more than 10GHZ. Measured spectrum and jitter (a) 120HZ and 100c and (b) then measured spectrum and jitter. Where Γ2=RMBZ.CH, RMBZ is the equivalent resistance of the transistor Mb2, and v2 is the initial voltage during the discharging interval the voltages vbl changes from the voltage V0~0v to the reference voltages Vsw assume Γ2<<Γ1, the required time track is approximated as Track-~T1Ln (VDD/VDD-vsw) Then required capacitor CH~TRACK/ln (VDD/VDD-VSW).RMB1 In this work the minimum frequency step Δfmin of this PLL is equal to the reference frequency fref

Δ vctrl=Δfmin/kvco=fref/kvco

Required time for this PLL to reach

ΔT = (c1+c2)/IP .Δvctrl

The output is obtained by a self biased buffer. A common-mode detector can be used to detect the common-mode voltage.

	This work		[5]	[6]	[9]	[10]
CMOS	65nm		130nm	130nm	130nm	65nm
Supply	1.2V		1V	1.5V	1V	1.2V
Measured VCO frequency	w/o self-healing	w/i self-healing	10 ~ 700 MHz	30~650 MHz	200 ~ 950 MHz	470 ~ 1130 MHz
	105 ~ 950MHz	60MHz ~ 1489MHz				
Divider Ratio	4 ~ 131		N.A.	1~4096	4 ~ 160	16 ~ 63
Jitter [ps]	w/o calibration*		w/o calibration			
	rms 43.62	pk-pk 284.4	N.A.	N.A.	rms 70.9 / pk-pk 420 @640MHz	Does not lock
	@855MHz					
Jitter [ps]	w/i calibration*		w/i calibration			
	rms 8.03	pk-pk 55.6	rms 24.3 / pk-pk 155 @360MHz	rms 4.9 / pk-pk 44.6 @240MHz	rms 8 / pk-pk 62.6 @640MHz	rms 5.13 / pk-pk 46.2 @800MHz
	@855MHz					
Ref. Spur	w/o calibration*	w/i calibration*	N.A	-35 dBc @240MHz	N.A.	N.A.
	-33.42dBc @855MHz	-52.89dBc @855MHz				
Area [mm²]	0.0182**		0.1681	0.18	0.063	0.065
Power	4.3@855MHz		7@200MHz	7@240MHz	3@640MHz	3.6@800MHz

V.CONCLUSION:

A wide-range PLL is fabricated in a 65-nm CMOS process. To deal with the process variability and leakage current in nano-scale CMOS process.

A self-healing pre-scaler a self-healing, VCO, and a calibrated CP are presented experimental results are given to demonstrate the feasibility.

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